# AUDIO, RADIO AND TV CIRCUITS
# 1st EDITION
# ISSUED NOVEMBER 1983

## INTRODUCTION

This book contains datasheets for SGS integrated circuits and discrete semiconductors commoly used in Audio, Radio and TV applications.

SGS also manufactures a wide range of bipolar, MOS and CMOS ICs for other applications, discrete semiconductors and computer systems.

For details of other databooks contact your SGS sales office or distributor.

# SGS-ATES GROUP OF COMPANIES

**INTERNATIONAL HEADQUARTERS**
SGS-ATES Componenti Elettronici SpA
Via C. Olivetti 2 - 20041 Agrate Brianza - Italy
Tel.: 39 - 65551
Telex: 330131-330141 SGSAGR

**BENELUX**
SGS-ATES Componenti Elettronici SpA
Benelux Sales Office
**B- 1180 Bruxelles**
Winston Churchill Avenue, 122
Tel.: 2 - 3432439
Telex: 24149 B

**BRAZIL**
Sales Office:
**05413 Sao Paulo**
Av. Henrique Schaumann 286-CJ33
Tel.: 11 - 853-5062
Telex: 37988 UMBR BR

**DENMARK**
SGS-ATES Scandinavia AB
Sales Office
**2730 Herlev**
Herlev Torv, 4
Tel.: 2 - 948533
Telex: 35411

**EASTERN EUROPE**
SGS-ATES Componenti Elettronici SpA
Export Sales Office
**20090 Assago (MI)**
V.le Milanofiori - Strada 4 - Palazzo A/4/A
Tel.: 2 - 8244131 (10 linee)
Telex: 330131-330141 SGSAGR

**FRANCE**
Société Générale de Semiconducteurs S.A.
**75643 Paris Cedex 13**
Résidence "Le Palatino"
17, Avenue de Choisy
Tel.: 1 - 5842730
Telex: 042 - 250938

**HONG KONG**
SGS-ATES Singapore (Pte) Ltd.
9th Floor, Block N,
Kaiser Estate, Phase III,
11 Hok Yuen St.,
**Hung Hom, Kowloon**
Tel.: 3-644251/5
Telex: 33906 ESGIE HX

**ITALY**
SGS-ATES Componenti Elettronici SpA
Direzione Italia e Sud Europa
**20090 Assago (MI)**
V.le Milanofiori - Strada 4 - Palazzo A/4/A
Tel.: 2 - 8244131 (10 linee)
Telex: 330131-330141 SGSAGR

Sales Offices:
**40128 Bologna**
Via Corticella, 231
Tel.: 51 - 324486
**00199 Roma**
Piazza Gondar, 11
Tel.: 6 - 8392848/8312777

**SINGAPORE**
SGS-ATES Singapore (Pte) Ltd.
**Singapore 1231**
Lorong 4 & 6 - Toa Payoh
Tel.: 2531411
Telex: ESGIES RS 21412

**SWEDEN**
SGS-ATES Scandinavia AB
**19500 Märsta**
Bristagatan 16
Tel.: 760 - 40120
Telex: 042 - 10932

**SWITZERLAND**
SGS-ATES AG
Swiss Sales Offices
**6340 Baar**
Oberneuhofstrasse, 2
Tel.: 42 - 315955
Telex: 864915
**1218 Grand-Saconnex** (Geneve)
Chemin François-Lehmann 22
Tel.: 22 - 986462/3
Telex: 28895

**UNITED KINGDOM**
SGS-ATES (United Kingdom) Ltd.
**Aylesbury, Bucks**
Planar House, Walton Street
Tel.: 296 - 5977
Telex: 041 - 83245

**U.S.A.**
SGS-Semiconductor Corporation
**Phoenix, AZ 85022**
1000 East Bell Road
Tel.: (602) 867-6100
Telex: 249976 SGSPH UR

Sales Offices:
**Bloomington, MN 55438**
6100 Green Valley Drive
Suite 120
Tel.: (612) 835-1347
**Dallas, TX 75248**
16970 Dallas North Parkway
Suite 401
Tel.: (214) 733-1515
Telex: 203997 SGSDA UR
**Hauppauge, NY 11788**
330 Motor Parkway
Suite 100
Tel.: (516) 435-1050
Telex: 221275 SGSHA UR
**Indianapolis, IN 46241**
2346 S. Lynhurst Drive
Suite E-207
Tel.: (317) 241-1116
Telex: 209144 SGSIN UR
**Irvine, CA 92714**
18271 W. McDurmott Drive
Suite J.
Tel. (714) 863-1222
Telex: 277793
**Norcross, GA 30071**
3040-D1 Holcomb Bridge Road
Tel.: (404) 446-8686
Telex: 261395 SGSAT UR
**Santa Clara, CA 95051**
2700 Augustine Drive
Suite 209
Tel.: (408) 727 - 3404
Telex: 278833 SGSSA UR
**Schaumburg, IL 60169**
600 North Meacham Road
Tel.: (312) 490-1890
Telex: 210159 SGSCH UR
**Waltham, MA 02154**
240 Bear Hill Road
Tel.: (617) 890-6688
Telex: 200297 SGSWH UR
**Woodland Hills, CA 91367**
6355 Topanga Canyon Boulevard
Suite 220
Tel.: (213) 716-6600
Telex: 215258 SGSWD UR

**WEST GERMANY**
SGS-ATES Deutschland Halbleiter
Bauelemente GmbH
**8018 Grafing bei München**
Haidling, 17
Tel.: 8092-690
Telex: 05 27378
Sales Offices:
**3012 Langenhagen**
Hubertusstrasse, 7
Tel.: 511 - 772075/7
Telex: 09 23195
**8500 Nürnberg 30**
Ostendstr., 204
Tel.: 911 - 572977/78/79
Telex: 0626243
**8023 Pullach bei München**
Seitnerstrasse, 42
Tel.: 89 - 793 0662
Telex: 5215784
**7000 Stuttgart 80**
Kalifenweg, 45
Tel.: 711 - 713091/2
Telex: 07 255545

# TABLE OF CONTENTS


GENERAL INFORMATION Page 4

ALPHANUMERICAL INDEX 8

INDEX BY APPLICATION 11

POWER TRANSISTOR SELECTION GUIDE 15

APPLICATION GUIDE 19

DATASHEETS 25

# IDENTITY

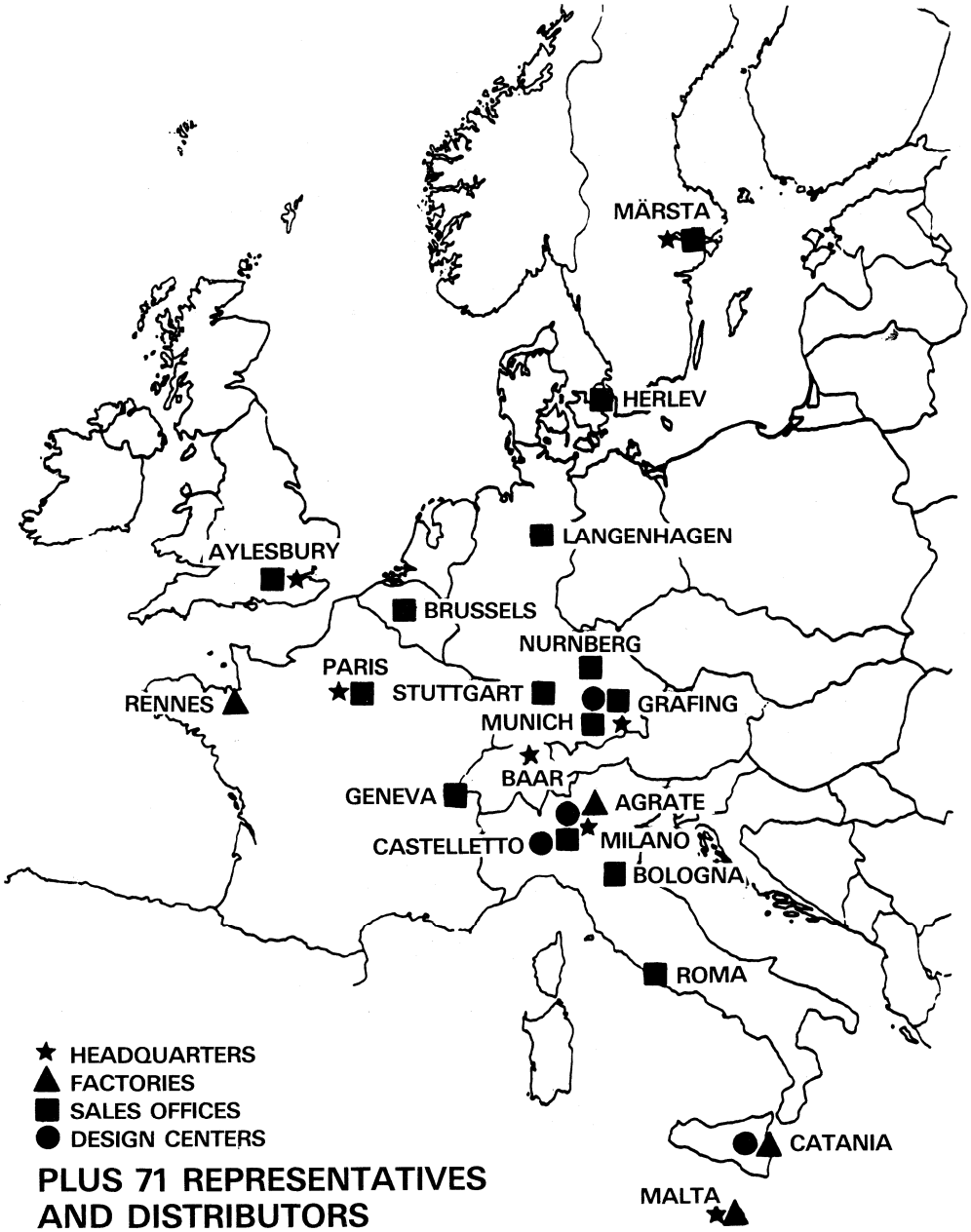
25 years ago, late in 1957, SGS was founded around a team of researchers who were already carrying out pioneer work in the field of semiconductors. From that small nucleus, the company has evolved into a Group of Companies, operating on a worldwide basis as a broad range semiconductor producer, with billings in the quarter billion dollar range and employing about 7500 people.

The company is fully owned by STET, the Italian Financial Company for Telecommunications and Electronics, a 7,5 billion dollar holding which, through its subsidiaries, operates the Italian telecommunications network and manufactures electronic equipment for applications such as telecommunications, space, defense, robotics, telematics, computers, etc. SGS is the subsidiary manufacturing active electronic components.

The SGS Group of Companies has now reached a total of 10 subsidiaries, located in France, Germany, Italy, Malta, Malaysia, Singapore, Sweden, Switzerland, United Kingdom and the USA.

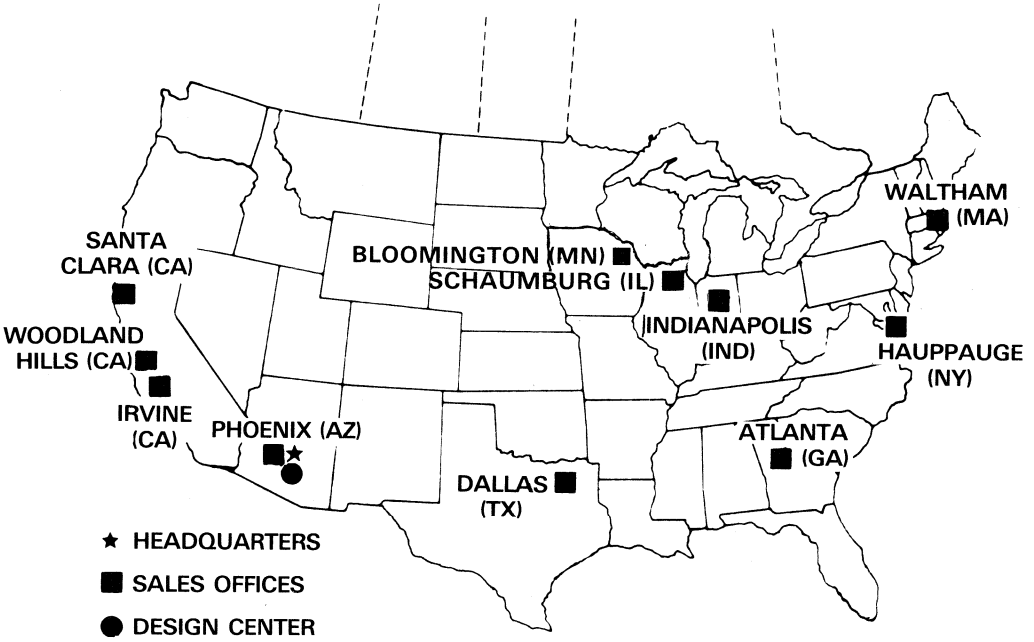
To go with its logo, the company has chosen the motto "Technology and Service", underlining the accent given to the development of state-of-the-art technologies and the corporate commitment to offer customers the best quality and service in the industry.

# SGS-ATES LOCATIONS - EUROPE



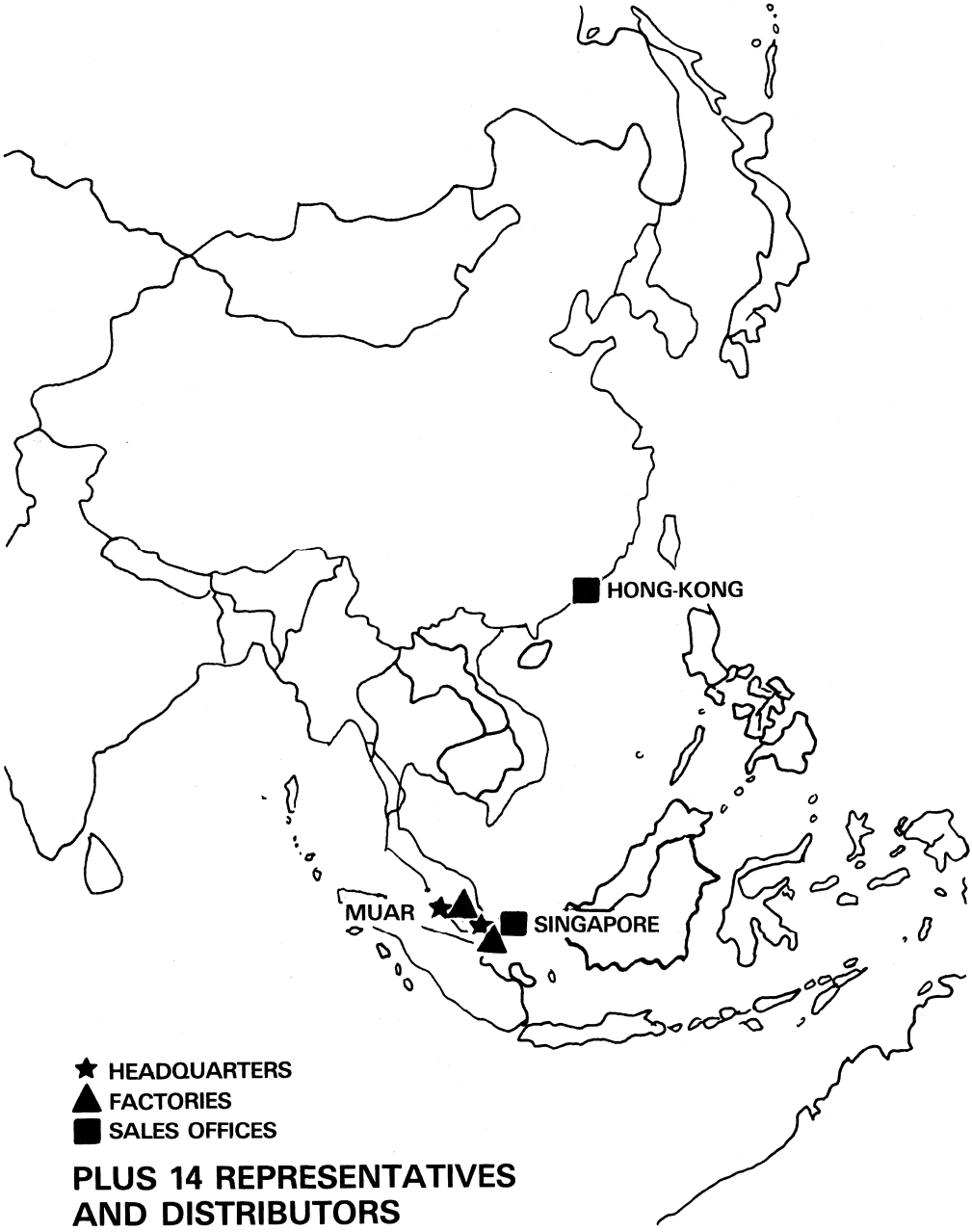

**PLUS 71 REPRESENTATIVES AND DISTRIBUTORS**

# SGS-ATES LOCATIONS
# NORTH AMERICA




## PLUS 108 REPRESENTATIVES AND DISTRIBUTORS

# SGS-ATES LOCATIONS - ASIA/PACIFIC




★ HEADQUARTERS
▲ FACTORIES
■ SALES OFFICES

**PLUS 14 REPRESENTATIVES AND DISTRIBUTORS**

# ALPHANUMERICAL INDEX


| Type | Function | Page |
|---|---|---|
| BD905 | Power linear and switching application | 26 |
| BD906 | Power linear and switching application | 30 |
| BD907 | Power linear and switching application | 26 |
| BD908 | Power linear and switching application | 30 |
| BD909 | Power linear and switching application | 26 |
| BD910 | Power linear and switching application | 30 |
| BD911 | Power linear and switching application | 26 |
| BD912 | Power linear and switching application | 30 |
| BU326 | High voltage power switch | 34 |
| BU326A | High voltage power switch | 39 |
| BU326S | High voltage power switch | 44 |
| BU406 | Horizontal TV deflector | 48 |
| BU406D | Horizontal TV deflector | 54 |
| BU406H | Horizontal TV deflector | 48 |
| BU407 | Horizontal TV deflector | 60 |
| BU407D | Horizontal TV deflector | 54 |
| BU407H | Horizontal TV deflector | 60 |
| BU408 | Horizontal TV deflector | 48 |
| BU408D | Horizontal TV deflector | 54 |
| BU426 | High voltage power switch | 66 |
| BU426A | High voltage power switch | 66 |
| BU806 | Fast switching darlington transistor | 69 |
| BU807 | Fast switching darlington transistor | 69 |
| BUX84 | High voltage switch | 75 |
| L200 | Adjustable voltage and current regulator | 77 |
| L272 | Dual power operational amplifier | 86 |
| L272M | Dual power operational amplifier | 91 |
| L296 | High current switching regulator | 95 |
| L387 | Very low drop 5V voltage regulator | 107 |
| L4705 | Very low drop voltage regulator | 110 |
| L4785 | Very low drop voltage regulator | 110 |
| L4710 | Very low drop voltage regulator | 110 |
| L4805 | Very low drop voltage regulator | 113 |
| L4885 | Very low drop voltage regulator | 113 |
| L4810 | Very low drop voltage regulator | 113 |
| M091 | ON-screen timing scale and band display | 117 |
| M104 | PCM remote control receiver | 125 |
| M105 | PCM remote control receiver | 135 |
| M190 | 16 Key keyboard encoder and latch | 144 |
| M191 | ON-screen timing scale and band display | 117 |
| M192 | 4-Bit binary 7-segment decoder driver | 150 |
| M193A | EPM 16-Electronic program memory (16 station) | 154 |

# ALPHANUMERICAL INDEX


| Type | Function | Page |
|---|---|---|
| M193C | EPM 16-Electronic program memory (16 station) | 154 |
| M193D | EPM 16-Electronic program memory (16 station) | 154 |
| M206 | PLL TV Microcomputer interface | 168 |
| M293 | EPM 16-Electronic program memory for 32 stations | 182 |
| M490 | Single chip non volatile station memory, PCM remote control receiver and display driver | 197 |
| M491 | Single chip non volatile station memory, PCM remote control receiver and display driver | 197 |
| M705 | 15/16 Divider for TV PLL frequency synthesizer | 220 |
| M708 | PCM remote control transmitter | 224 |
| M708A | PCM remote control transmitter | 224 |
| M709 | PCM remote control transmitter | 231 |
| M709A | PCM remote control transmitter | 231 |
| M710 | PCM remote control transmitter | 231 |
| M710A | PCM remote control transmitter | 231 |
| M5450 | Led display driver | 240 |
| M5451 | Led display driver | 240 |
| M5480 | Led display driver | 247 |
| M5481 | Led display driver | 253 |
| M5482 | Led display driver | 259 |
| M5486 | Led display driver | 265 |
| MJE13004 | High voltage power switch | 272 |
| MJE13005 | High voltage power switch | 272 |
| TBA331 | General purpose transistor array | 277 |
| TBA810CB | Fully protected 7W audio amplifier for CB radio | 283 |
| TBA810P | 7W Audio amplifier | 288 |
| TBA810S | 7W Audio amplifier | 292 |
| TBA820M | Minidip 1.2W audio amplifier | 295 |
| TCA3089 | FM if radio system | 302 |
| TCA3189 | FM if high quality radio system | 308 |
| TDA440S | TV vision if system | 313 |
| TDA1054M | Preamplifier with ALC for cassette recorders | 322 |
| TDA1151 | Motor speed regulator | 332 |
| TDA1170D | Low noise TV vertical deflection system | 338 |
| TDA1170N | Low noise TV vertical deflection system | 346 |
| TDA1170S | TV vertical deflection system | 353 |
| TDA1180P | TV horizontal processor | 365 |
| TDA1190Z | Complete TV sound channel | 377 |
| TDA1220A | AM-FM radio | 385 |
| TDA1220B | AM-FM quality radio | 395 |
| TDA1220L | Low voltage AM-FM radio | 411 |
| TDA1670A | Vertical deflection circuit | 420 |

# ALPHANUMERICAL INDEX


| Type | Function | Page |
|---|---|---|
| TDA1770A | Vertical deflection circuit | 433 |
| TDA1904 | 4W Audio amplifier | 446 |
| TDA1905 | 5W Audio amplifier with muting | 452 |
| TDA1908 | 8W Audio amplifier | 465 |
| TDA1910 | 10W Audio amplifier with muting | 476 |
| TDA2002 | 8W Car radio audio amplifier | 489 |
| TDA2003 | 10W Car radio audio amplifier | 496 |
| TDA2004 | 10 + 10W Stereo amplifier for car radio | 505 |
| TDA2005 | 20W Bridge amplifier for car radio | 515 |
| TDA2006 | 10W Audio amplifier | 529 |
| TDA2008 | 12W Audio amplifier ($V_s = 22V$, $R_L = 4\Omega$) | 539 |
| TDA2009 | 10 + 10W High quality stereo amplifier | 544 |
| TDA2010 | 12W Hi-Fi audio amplifier | 554 |
| TDA2020 | 20W Hi-Fi audio amplifier | 559 |
| TDA2020D | 40W Audio driver | 566 |
| TDA2030 | 14W Hi-Fi audio amplifier | 573 |
| TDA2030A | 18W Hi-Fi audio amplifier and 30W driver | 583 |
| TDA2040 | 20W Hi-Fi audio power amplifier | 597 |
| TDA2040A | 20W Hi-Fi audio power amplifier | 604 |
| TDA2054M | Preamplifier with ALC for $C_r$ $O_2$ cassette recorders | 607 |
| TDA2170 | TV vertical deflection output circuit | 614 |
| TDA2220 | High performance AM/FM radio | 622 |
| TDA2270 | TV vertical deflection output circuit | 632 |
| TDA2320 | Preamplifier for infrared remote control systems | 640 |
| TDA2320A | Minidip stereo preamplifier | 645 |
| TDA2822 | Dual power amplifier | 655 |
| TDA2822M | Dual low-voltage power amplifier | 661 |
| TDA3190 | Complete TV sound channel | 669 |
| TDA3410 | Dual low noise tape preamplifier with autoreverse | 678 |
| TDA3420 | Dual very low noise preamplifier | 686 |
| TDA4092 | 5 Bit binary to 7-segment decoder driver | 693 |
| TDA4190 | Complete TV sound channel with DC volume and tone controls | 699 |
| TDA4420 | Vision if system with AFC | 710 |
| TDA4431 | TV signal identification circuit and AFC interface | 717 |
| TDA4433 | TV signal identification circuit and AFC interface | 717 |
| TDA4950 | TV east/west correction circuit | 725 |
| TDA7220 | Very low voltage AM-FM radio | 730 |
| TDA7270S | Multifunction system for tape players | 736 |
| TDA8170 | TV vertical deflection output circuit | 747 |
| TDA8180 | Deflection processor | 756 |
| TDA8190 | TV sound channel with DC controls | 771 |
| TEA1330 | FM stereo decoder | 781 |

# INDEX BY APPLICATIONS

## AUDIO


| Function | Type | Page |
|---|---|---|
| Preamplifiers | TDA2320A | 645 |
| | TDA3410 | 678 |
| | TDA3420 | 686 |
| Power amplifiers | BD905/07/09/11 | 26 |
| | BD906/08/10/12 | 30 |
| | TBA810CB | 283 |
| | TBA810P | 288 |
| | TBA810S | 292 |
| | TBA820M | 295 |
| | TDA1904 | 446 |
| | TDA1905 | 452 |
| | TDA1908 | 465 |
| | TDA1910 | 476 |
| | TDA2002 | 489 |
| | TDA2003 | 496 |
| | TDA2004 | 505 |
| | TDA2005 | 515 |
| | TDA2006 | 529 |
| | TDA2008 | 539 |
| | TDA2009 | 544 |
| | TDA2010 | 554 |
| | TDA2020 | 559 |
| | TDA2020D | 566 |
| | TDA2030 | 573 |
| | TDA2030A | 583 |
| | TDA2040 | 597 |
| | TDA2040A | 604 |
| | TDA2822 | 655 |
| | TDA2822M | 661 |


## RADIO


| Function | Type | Page |
|---|---|---|
| FM IF systems | TCA3089 | 302 |
| | TCA3189 | 308 |
| AM/FM radio | TDA1220A | 385 |
| | TDA1220B | 395 |
| | TDA1220L | 411 |
| | TDA2220 | 622 |
| | TDA7220 | 730 |
| Stereo decoder | TEA1330 | 781 |

# INDEX BY APPLICATIONS

## TV


| Function | Type | Page |
|---|---|---|
| Deflection | BU406 | 48 |
| | BU406D | 54 |
| | BU406H | 48 |
| | BU407 | 60 |
| | BU407D | 54 |
| | BU407H | 60 |
| | BU408 | 48 |
| | BU408D | 54 |
| | BU806 | 69 |
| | BU807 | 69 |
| | TDA1170D | 338 |
| | TDA1170N | 346 |
| | TDA1170S | 353 |
| | TDA1180P | 365 |
| | TDA1670A | 420 |
| | TDA1770A | 433 |
| | TDA2170 | 614 |
| | TDA2270 | 632 |
| | TDA8170 | 747 |
| | TDA8180 | 756 |
| Sound | TDA1190Z | 377 |
| | TDA3190 | 669 |
| | TDA4190 | 699 |
| | TDA8190 | 771 |
| Other TV functions | TDA440S | 313 |
| | TDA4420 | 710 |
| | TDA4950 | 725 |
| Tuning & remote control | M091 | 117 |
| | M104 | 125 |
| | M105 | 135 |
| | M190 | 144 |
| | M191 | 117 |
| | M192 | 150 |
| | M193A/C/D | 154 |
| | M206 | 168 |
| | M293 | 182 |
| | M490 | 197 |
| | M491 | 197 |
| | M705 | 220 |
| | M708/A | 224 |
| | M709/A | 231 |
| | M710/A | 231 |
| | M5450 | 240 |

# INDEX BY APPLICATIONS

## TV

| Function | Type | Page |
|---|---|---|
| Tuning & remote control | M5451 | 240 |
| | M5480 | 247 |
| | M5481 | 253 |
| | M5482 | 259 |
| | M5486 | 265 |
| | TDA2320 | 640 |
| | TDA4092 | 693 |
| | TDA4431 | 717 |
| | TDA4433 | 717 |
| Switch mode power supply | BU326 | 34 |
| | BU326A | 39 |
| | BU326S | 44 |
| | BU426 | 66 |
| | BU426A | 66 |
| | BUX84 | 75 |
| | MJE13004 | 272 |
| | MJE13005 | 272 |

## MISCELLANEOUS

| Function | Type | Page |
|---|---|---|
| Motor speed regulators | TDA1151 | 332 |
| | TDA7270S | 736 |
| Tape preamplifiers | TDA1054M | 322 |
| | TDA2054M | 607 |
| Dual power OP. AMPS. for motor driving | L272 | 86 |
| | L272M | 91 |

## REGULATORS

| Function | Type | Page |
|---|---|---|
| Variable regulators | L200 | 77 |
| | L296 | 95 |
| Low drop regulators | L387 | 107 |
| | L4705 | 110 |
| | L4785 | 110 |
| | L4710 | 110 |
| | L4805 | 113 |
| | L4885 | 113 |
| | L4810 | 113 |

# SELECTION GUIDE

# SELECTION GUIDE

## NPN TRANSISTORS & DARLINGTONS FOR APPLICATION IN HORIZONTAL DEFLECTION STAGE OF TV RECEIVERS

| Type | $I_C$ (A) | $V_{CBO}$ (V) | $V_{CEO}$ (V) | $P_{tot}$ (W) | $h_{FE}$ min | @ $I_C/V_{CE}$ (A/V) | $V_{CEsat}$ max (V) | @ $I_C/I_B$ (A/mA) | Package | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| BU407D | 7 | 330 | – | 60 | 8 | 5/1 | 1 | 5/650 | TO-220 | 54 |
| BU407H | 7 | 330 | 150 | 60 | 6 | 5/1 | 1 | 5/800 | TO-220 | 60 |
| BU407 | 7 | 330 | 150 | 60 | 10 | 5/1 | 1 | 5/500 | TO-220 | 60 |
| BU408D | 7 | 400 | – | 60 | 5 | 6/1 | 1 | 6/1200 | TO-220 | 54 |
| BU408 | 7 | 400 | 200 | 60 | 5 | 6/1 | 1 | 6/1200 | TO-220 | 48 |
| BU406D | 7 | 400 | – | 60 | 8 | 5/1 | 1 | 5/650 | TO-220 | 54 |
| BU406H | 7 | 400 | 200 | 60 | 6 | 5/1 | 1 | 5/800 | TO-220 | 48 |
| BU406 | 7 | 400 | 200 | 60 | 10 | 5/1 | 1 | 5/500 | TO-220 | 48 |
| BU807* | 8 | 330 | 150 | 60 | 100 | 5/2 | 1.5 | 5/50 | TO-220 | 69 |
| BU806* | 8 | 400 | 200 | 60 | 100 | 5/2 | 1.5 | 5/50 | TO-220 | 69 |

* Darlington types.

## NPN TRANSISTORS FOR APPLICATION IN SWITCH-MODE POWER SUPPLY SYSTEM FOR TV RECEIVERS

| Type | $I_C$ (A) | $V_{CBO}$ (V) | $V_{CEO}$ (V) | $P_{tot}$ (W) | $h_{FE}$ min. | @ $I_C/V_{CE}$ (A/V) | $V_{CE\ sat}$ max (V) | @ $I_C/I_B$ (A/mA) | Package | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| BUX84 | 2 | 800 | 400 | 40 | 50 | 0.1/5 | 3 | 1/200 | TO-220 | 75 |
| MJE13004 | 4 | 600 | 300 | 75 | 8 | 2/5 | 0.6 | 2/500 | TO-220 | 272 |
| MJE13005 | 4 | 700 | 400 | 75 | 8 | 2/5 | 0.6 | 2/500 | TO-220 | 272 |
| BU326 | 6 | 800 | 375 | 75 | 25• | 1/5 | 1.5 | 2.5/500 | TO-3 | 34 |
| BU426 | 6 | 800 | 375 | 113 | 25• | 0.6/5 | 1.5 | 2.5/500 | SOT-93 | 66 |
| BU326S | 6 | 800 | 400 | 90 | 3.5 | 4/5 | 1.5 | 2.5/500 | TO-3 | 44 |
| BU326A | 6 | 900 | 400 | 75 | 25• | 1/5 | 1.5 | 2.5/500 | TO-3 | 39 |
| BU426A | 6 | 900 | 400 | 113 | 25• | 0.6/5 | 1.5 | 2.5/500 | SOT-93 | 66 |

• Typical.

## POWER TRANSISTORS FOR AUDIO APPLICATIONS

| $V_{CEO}$(V) / $I_C$ (A) | 22 | | 32 | | 40 | | 45 | | 60 | | 80 | | 100 | | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | NPN | PNP | NPN | PNP | NPN | PNP | NPN | PNP | NPN | PNP | NPN | PNP | NPN | PNP | |
| 1 | | | | | TIP29 | TIP30 | BD135 | BD136 | BD137<br>TIP29A | BD138<br>TIP30A | BD139<br>TIP29B | BD140<br>TIP30B | TIP29C | TIP30C | TO-126<br>TO-220 |
| 2 | | | | | | | BD233<br>BD239 | BD234<br>BD240 | BD235<br>BD239A<br>TIP110 | BD236<br>BD240A<br>TIP115 | BD237<br>BD239B<br>TIP111 | BD238<br>BD240B<br>TIP116 | BD239C<br>TIP112 | BD240C<br>TIP117 | TO-126<br>TO-220<br>TO-220 |
| 3 | | | | | TIP31 | TIP32 | BD175<br>BD241 | BD176<br>BD242 | BD177<br>BD241A<br>TIP31A | BD178<br>BD242A<br>TIP32A | BD179<br>BD241B<br>TIP31B | BD180<br>BD242B<br>TIP32B | BD241C<br>TIP31C | BD242C<br>TIP32C | TO-126<br>TO-220<br>TO-220 |
| 4 | BD433 | BD434 | BD435 | BD436 | 2N5190 | 2N5193 | BD437<br>BD533 | BD438<br>BD534 | BD439<br>2N5191<br>BD535 | BD440<br>2N5194<br>BD536 | BD441<br>2N5192<br>BD537 | BD442<br>2N5195<br>BD538 | | | TO-126<br>TO-126<br>TO-220 |
| 6 | | | | | TIP41 | TIP42 | BD243 | BD244 | BD243A<br>TIP41A | BD244A<br>TIP42A | BD243B<br>TIP41B | BD244B<br>TIP42B | BD243C<br>TIP41C | BD244C<br>TIP42C | TO-220<br>TO-220 |
| 10 | | | | | | | | | MJE3055T<br>2N3715<br>2N5877 | MJE2955T<br>2N3791<br>2N5875 | 2N3716<br>2N5878 | 2N3792<br>2N5876 | | | TO-220<br>TO-3<br>TO-3 |
| 12 | | | | | | | BD705 | BD706 | BD707 | BD708 | BD709 | BD710 | BD711 | BD712 | TO-220 |
| 15 | | | | | 2N3771 | | BD905<br>BDW51 | BD906<br>BDW52 | BD907<br>2N3055E<br>2N3772<br>BDW51A | BD908<br>MJ2955<br>BDW52A | BD909<br>BDW51B | BD910<br>BDW52B | BD911<br>BDW51C | BD912<br>BDW52C | TO-220<br>TO-3<br>TO-3<br>TO-3 |
| 25 | | | | | TIP35 | TIP36 | BD249 | BD250 | BD249A<br>TIP35A<br>2N5885 | BD250A<br>TIP36A<br>2N5883 | BD249B<br>TIP35B<br>2N5886 | BD250B<br>TIP36B<br>2N5884 | BD249C<br>TIP35C | BD250C<br>TIP36C | SOT-93<br>SOT-93<br>TO-3 |
| 30 | | | | | 2N5301 | 2N4398 | | | 2N5302 | 2N4399 | 2N5303 | 2N5745 | | | TO-3 |

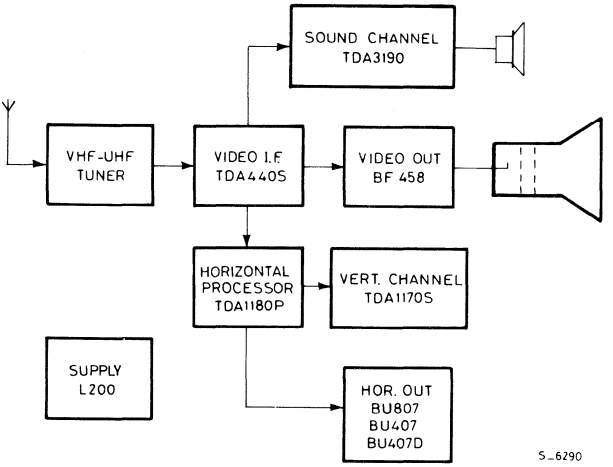
## DARLINGTONS FOR AUDIO APPLICATIONS

| $V_{CEO}$(V) / $I_C$ (A) | 40 | | 45 | | 60 | | 80 | | 90 | | 100 | | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | NPN | PNP | NPN | PNP | NPN | PNP | NPN | PNP | NPN | PNP | NPN | PNP | |
| 4 | | | BD675A | BD676A | BD677<br>BD677A | BD678<br>BD678A | BD679<br>BD679A | BD680<br>BD680A | | | BD681 | BD682 | TO-126 |
| 5 | | | | | TIP120 | TIP125 | TIP121 | TIP126 | | | TIP122 | TIP127 | TO-220 |
| 6 | | | BDW23 | BDW24 | BDW23A | BDW24A | BDW23B | BDW23C | | | BDW23C | BDW24C | TO-220 |
| 8 | <br><br>2N6386 | | BDX53 | BDX54 | BDX53A<br>TIP130<br><br>MJ1000 | BDX54A<br>TIP135<br><br>MJ900 | BDX53B<br>TIP131<br><br>MJ1001 | BDX54B<br>TIP136<br><br>MJ901 | | | BDX53C<br>TIP132 | BDX54C<br>TIP137 | TO-220<br>TO-220<br>TO-220<br>TO-3 |
| 10 | | | BDX33<br><br><br>BDX85 | BDX34<br><br><br>BDX86 | BDX33A<br>2N6387<br>TIP140<br>BDX85A<br>MJ3000 | BDX34A<br><br>TIP145<br>BDX86A<br>MJ2500 | BDX33B<br>2N6388<br>TIP141<br>BDX85B<br>MJ3001 | BDX34B<br><br>TIP146<br>BDX86B<br>MJ2501 | | | BDX33C<br><br>TIP142<br>BDX85C | BDX34C<br><br>TIP147<br>BDX86C | TO-220<br>TO-220<br>SOT-93<br>TO-3<br>TO-3 |
| 12 | | | BDW93<br><br>BDX87 | BDW94<br><br>BDX88 | BDW93A<br>BDV65<br>BDX87A | BDW94A<br>BDV64<br>BDX88A | BDW93B<br>BDV65A<br>BDX87B | BDW94B<br>BDV64A<br>BDX88B | | | BDW93C<br>BDV65B<br>BDX87C | BDW94C<br>BDV64B<br>BDX88C | TO-220<br>SOT-93<br>TO-3 |
| 16 | | | | | MJ4033 | MJ4030 | MJ4034 | MJ4031 | | | MJ4035 | MJ4032 | TO-3 |
| 20 | | | | | 2N6282 | 2N6285 | 2N6283 | 2N6286 | | | 2N6284 | 2N6287 | TO-3 |
| 30 | | | | | MJ11012 | MJ11011 | | | MJ11014 | MJ11013 | MJ11016 | MJ11015 | TO-3 |

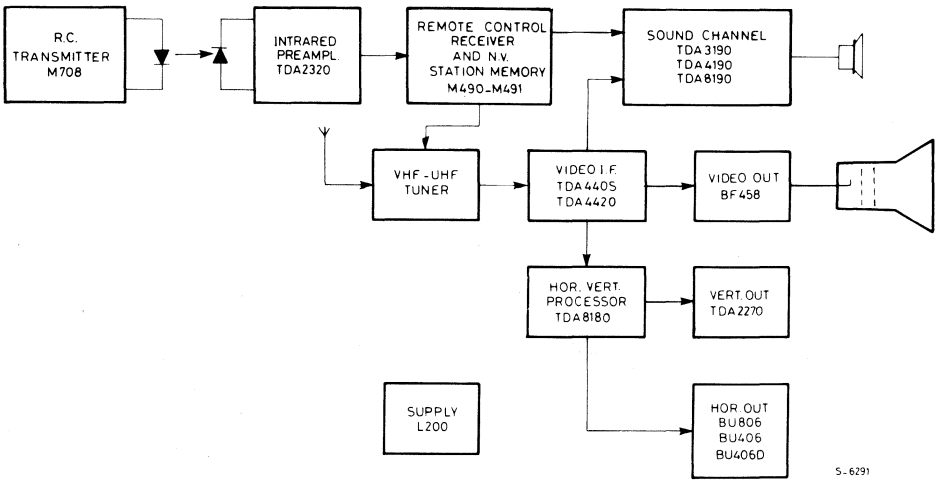
# APPLICATION GUIDE

# APPLICATION GUIDE

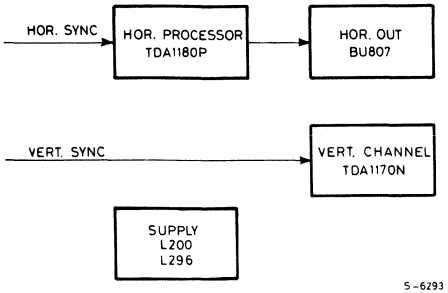
## LOW-COST B & W TV



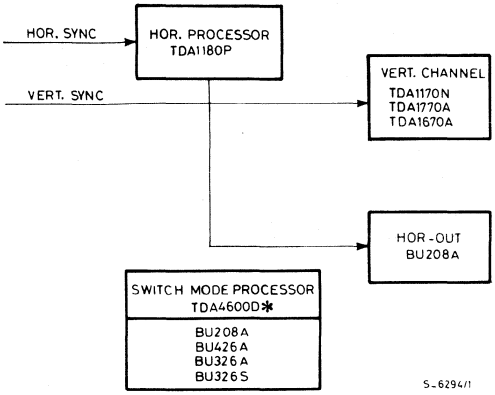

## LARGE SCREEN B & W TV



## B & W DISPLAY AND MONITOR

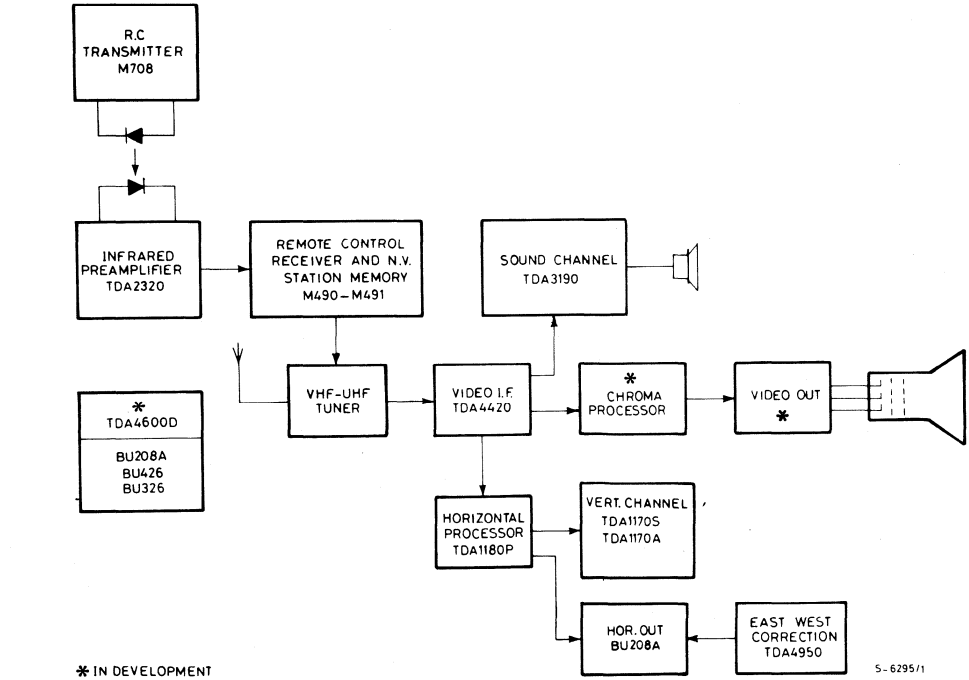



## COLOR DISPLAY AND MONITOR




*IN DEVELOPMENT

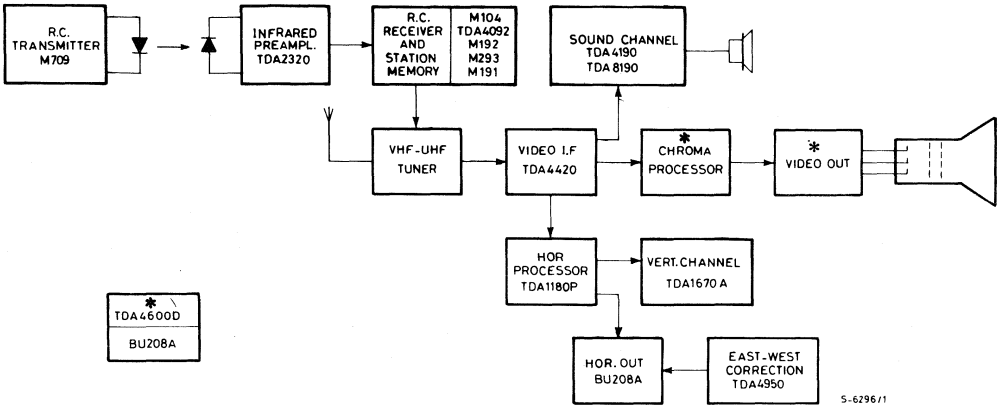
## LOW-COST SMALL SCREEN COLOR TV




*IN DEVELOPMENT

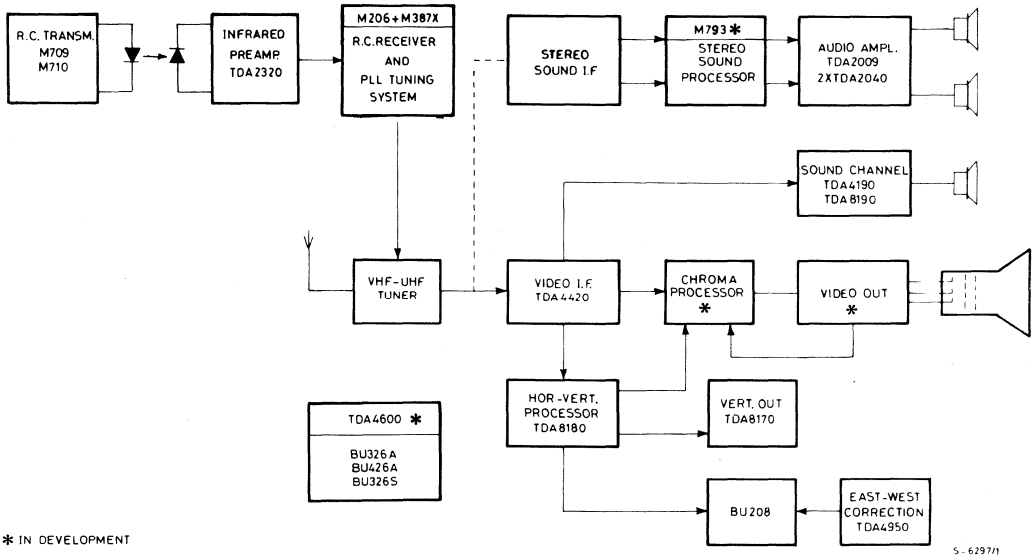
# APPLICATION GUIDE

## LARGE SCREEN COLOR TV



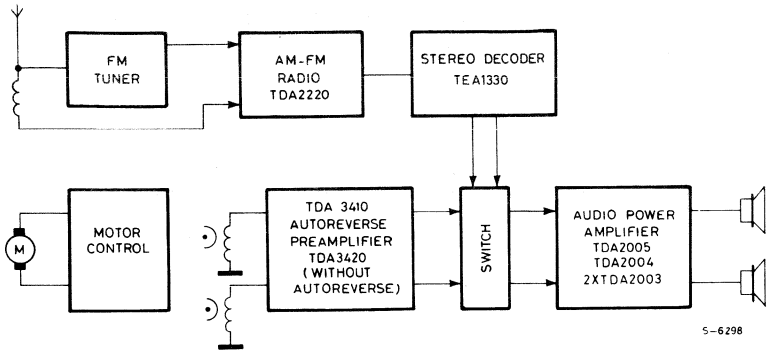

*IN DEVELOPMENT

## HIGH QUALITY COLOR TV

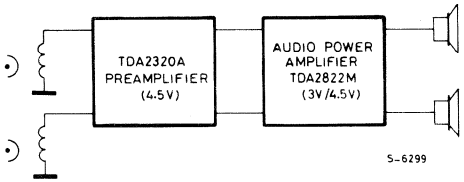



* IN DEVELOPMENT

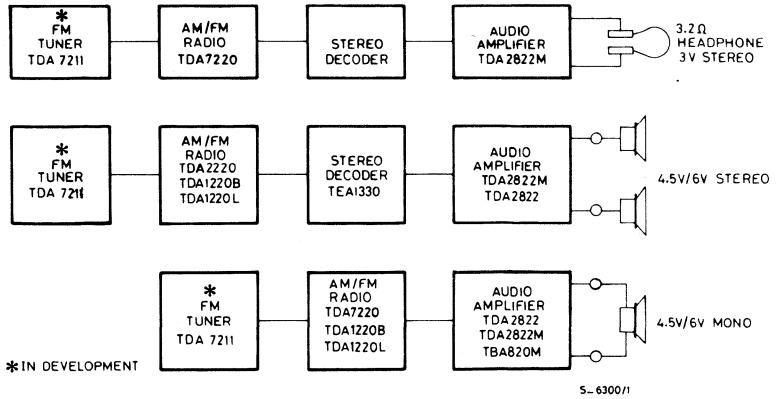
## CAR RADIO (WITH CASSETTE PLAYER)




## PORTABLE CASSETTE PLAYERS

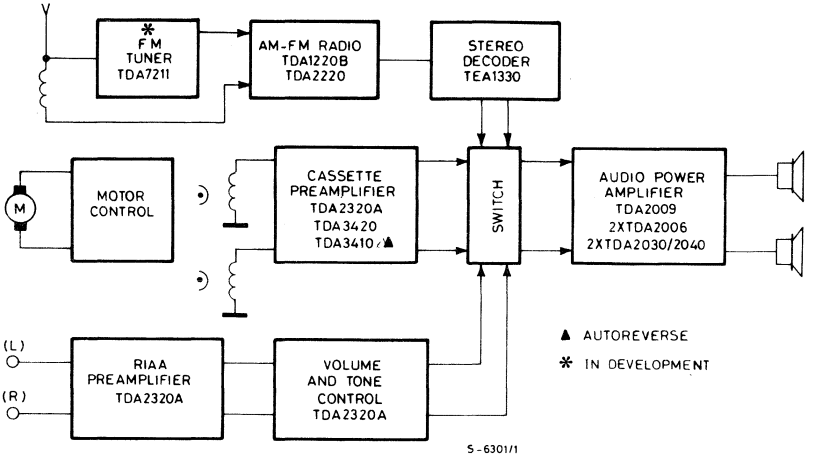



## PORTABLE RADIOS



# APPLICATION GUIDE

## MUSIC CENTERS



# DATASHEETS

BD905
BD907
BD909
BD911

# EPITAXIAL-BASE NPN

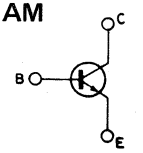
## POWER LINEAR AND SWITCHING APPLICATIONS

The BD 905, BD 907, BD 909, BD 911 are silicon epitaxial-base NPN power transistors in Jedec TO-220 plastic package. They are intended for use in power linear and switching applications.
The complementary PNP types are the BD 906, BD 908, BD 910 and BD 912 respectively.

## ABSOLUTE MAXIMUM RATINGS

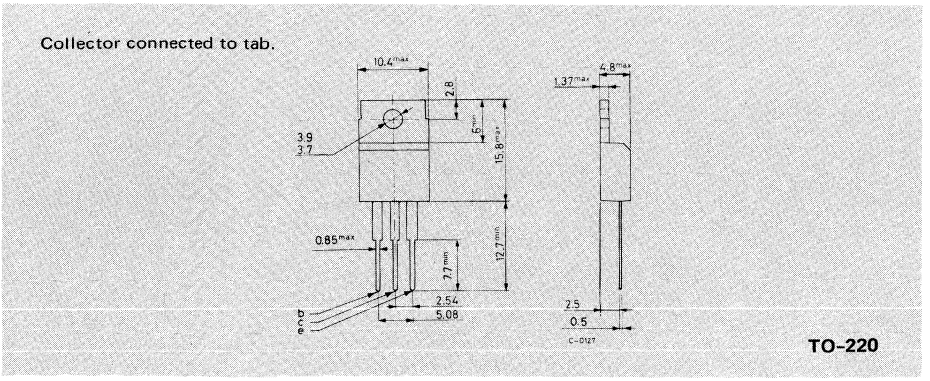
| | | BD905 | BD907 | BD909 | BD911 |
|---|---|---|---|---|---|
| $V_{CBO}$ | Collector-base voltage ($I_E = 0$) | 45V | 60V | 80V | 100V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B = 0$) | 45V | 60V | 80V | 100V |
| $V_{EBO}$ | Emitter-base voltage ($I_C = 0$) | 5V | | | |
| $I_E$, $I_C$ | Emitter and collector current | 15A | | | |
| $I_B$ | Base current | 5A | | | |
| $P_{tot}$ | Total power dissipation at $T_{case} \leqslant 25°C$ | 90W | | | |
| $T_{stg}$ | Storage temperature | -65 to 150°C | | | |
| $T_j$ | Junction temperature | 150°C | | | |

## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm




TO-220

## THERMAL DATA

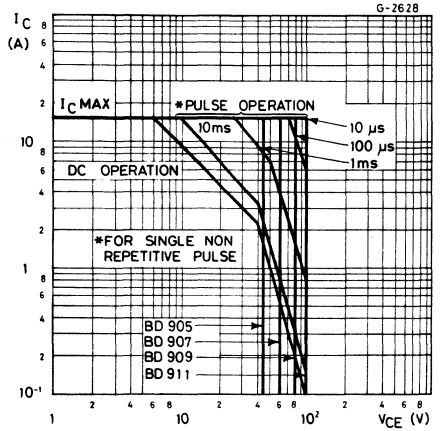
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 1.4 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless otherwise specified)

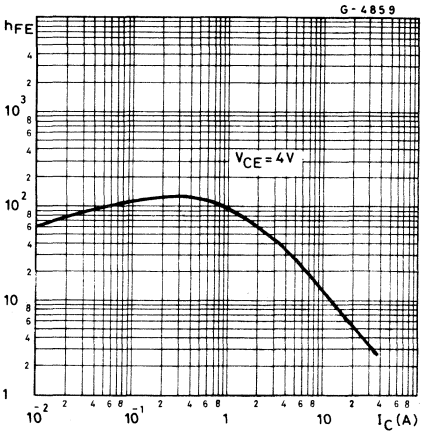
| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CBO}$ | Collector cutoff current ($I_E = 0$) | for **BD905** | $V_{CB}$ = 45V | | | 500 | μA |
| | | for **BD907** | $V_{CB}$ = 60V | | | 500 | μA |
| | | for **BD909** | $V_{CB}$ = 80V | | | 500 | μA |
| | | for **BD911** | $V_{CB}$ = 100V | | | 500 | μA |
| | | $T_{case}$ = 150°C | | | | | |
| | | for **BD905** | $V_{CB}$ = 45V | | | 5 | mA |
| | | for **BD907** | $V_{CB}$ = 60V | | | 5 | mA |
| | | for **BD909** | $V_{CB}$ = 80V | | | 5 | mA |
| | | for **BD911** | $V_{CB}$ = 100V | | | 5 | mA |
| $I_{CEO}$ | Collector cutoff current ($I_B = 0$) | for **BD905** | $V_{CE}$ = 30V | | | 1 | mA |
| | | for **BD907** | $V_{CE}$ = 30V | | | 1 | mA |
| | | for **BD909** | $V_{CE}$ = 40V | | | 1 | mA |
| | | for **BD911** | $V_{CE}$ = 50V | | | 1 | mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C = 0$) | $V_{EB}$ = 5V | | | | 1 | mA |
| $V_{CEO\ (sus)}$* | Collector-emitter sustaining voltage ($I_B = 0$) | $I_C$ = 100mA | | | | | |
| | | | for **BD905** | 45 | | | V |
| | | | for **BD907** | 60 | | | V |
| | | | for **BD909** | 80 | | | V |
| | | | for **BD911** | 100 | | | V |
| $V_{CE\ (sat)}$* | Collector-emitter saturation voltage | $I_C$ = 5A | $I_B$ = 0.5A | | | 1 | V |
| | | $I_C$ = 10A | $I_B$ = 2.5A | | | 3 | V |
| $V_{BE\ (sat)}$* | Base-emitter saturation voltage | $I_C$ = 10A | $I_B$ = 2.5A | | | 2.5 | V |
| $V_{BE}$* | Base-emitter voltage | $I_C$ = 5A | $V_{CE}$ = 4V | | | 1.5 | V |
| $h_{FE}$* | DC current gain | $I_C$ = 0.5A | $V_{CE}$ = 4V | 40 | | 250 | — |
| | | $I_C$ = 5A | $V_{CE}$ = 4V | 15 | | 150 | — |
| | | $I_C$ = 10A | $V_{CE}$ = 4V | 5 | | | — |
| $f_T$ | Transition frequency | $I_C$ = 0.5A | $V_{CE}$ = 4V | 3 | | | MHz |

* Pulsed: pulse duration = 300 μs, duty cycle = 1.5%

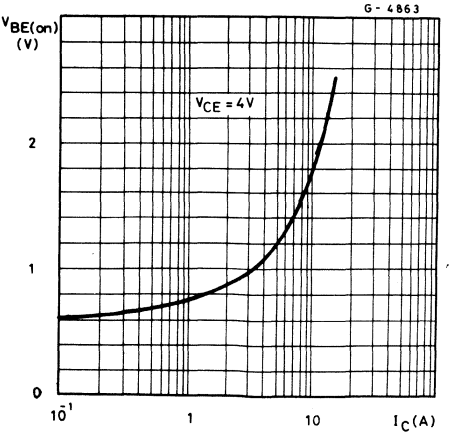
## Safe operating areas



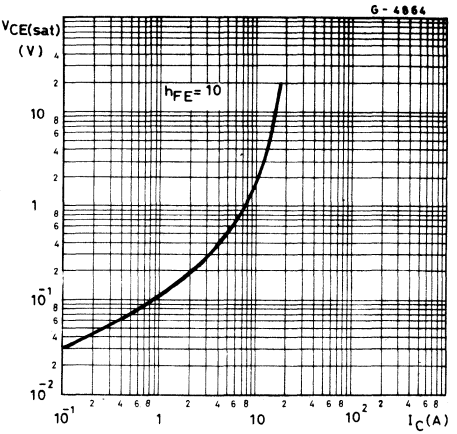

## DC current gain



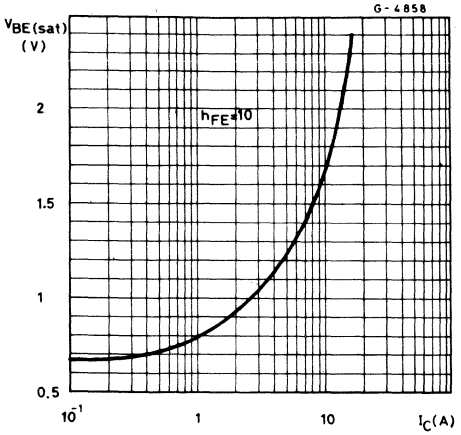

## DC transconductance



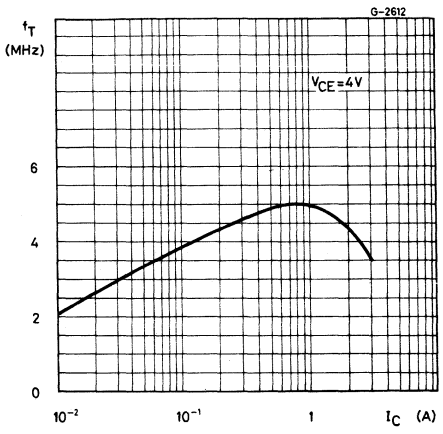

## Collector-emitter saturation voltage



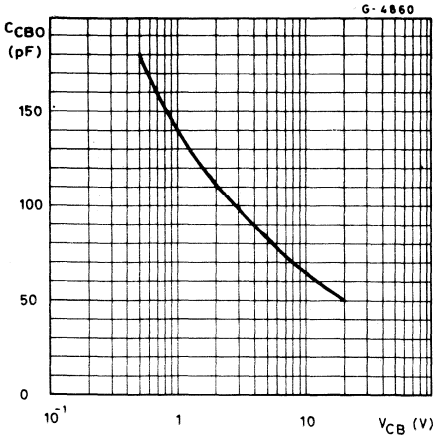
Base-emitter saturation voltage



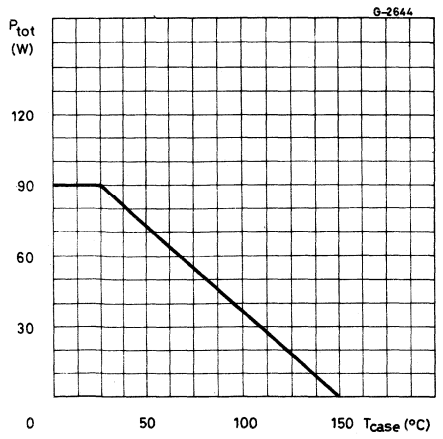

Transition frequency




Collector-base capacitance




Power rating chart



BD906
BD908
BD910
BD912

# EPITAXIAL-BASE PNP

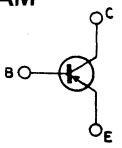
## POWER LINEAR AND SWITCHING APPLICATIONS

The BD 906, BD 908, BD 910 and BD 912 are silicon epitaxial-base PNP power transistors in Jedec TO-220 plastic package.
They are intended for use in power linear and switching applications.
The complementary NPN types are the BD 905, BD 907, BD 909 and BD 911 respectively.

## ABSOLUTE MAXIMUM RATINGS

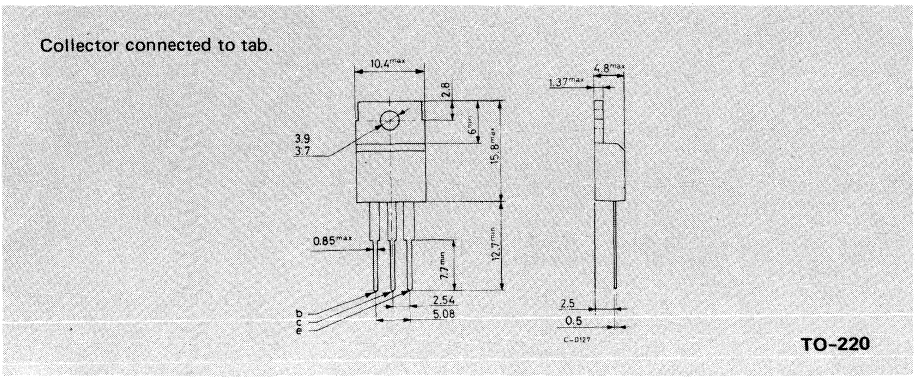
| | | BD906 | BD908 | BD910 | BD912 |
|---|---|---|---|---|---|
| $V_{CBO}$ | Collector-base voltage ($I_E = 0$) | -45V | -60V | -80V | -100V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B = 0$) | -45V | -60V | -80V | -100V |
| $V_{EBO}$ | Emitter-base voltage ($I_C = 0$) | -5V | | | |
| $I_E$, $I_C$ | Emitter and collector current | -15A | | | |
| $I_B$ | Base current | -5A | | | |
| $P_{tot}$ | Total power dissipation at $T_{case} \leq 25°C$ | 90W | | | |
| $T_{stg}$ | Storage temperature | -65 to 150°C | | | |
| $T_j$ | Junction temperature | 150°C | | | |

## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm



## THERMAL DATA

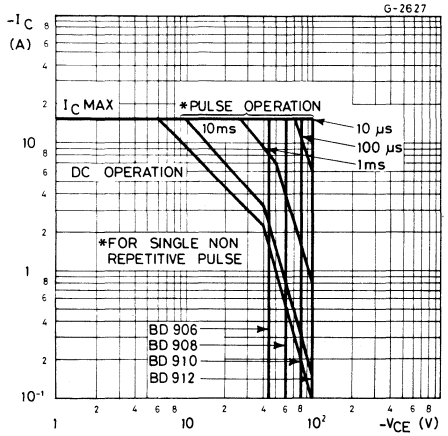
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 1.4 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless otherwise specified)

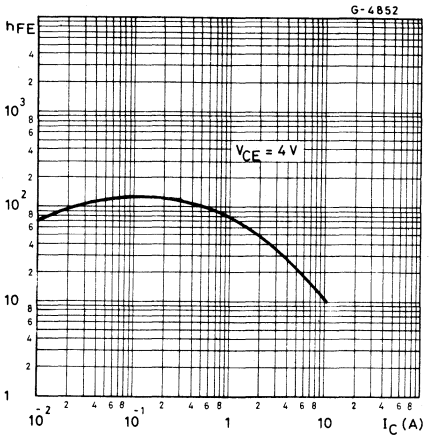
| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CBO}$ | Collector cutoff current ($I_E = 0$) | for **BD906** | $V_{CB}$ = -45V | | | -500 | μA |
| | | for **BD908** | $V_{CB}$ = -60V | | | -500 | μA |
| | | for **BD910** | $V_{CB}$ = -80V | | | -500 | μA |
| | | for **BD912** | $V_{CB}$ = -100V | | | -500 | μA |
| | | $T_{case}$ = 150°C | | | | | |
| | | for **BD906** | $V_{CB}$ = -45V | | | -5 | mA |
| | | for **BD908** | $V_{CB}$ = -60V | | | -5 | mA |
| | | for **BD910** | $V_{CB}$ = -80V | | | -5 | mA |
| | | for **BD912** | $V_{CB}$ = -100V | | | -5 | mA |
| $I_{CEO}$ | Collector cutoff current ($I_B = 0$) | for **BD906** | $V_{CE}$ = -30V | | | -1 | mA |
| | | for **BD908** | $V_{CE}$ = -30V | | | -1 | mA |
| | | for **BD910** | $V_{CE}$ = -40V | | | -1 | mA |
| | | for **BD912** | $V_{CE}$ = -50V | | | -1 | mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C = 0$) | $V_{EB}$ = -5V | | | | -1 | mA |
| $V_{CEO\ (sus)}$* | Collector-emitter sustaining voltage ($I_B = 0$) | $I_C$ = -100mA | | | | | |
| | | | for **BD906** | -45 | | | V |
| | | | for **BD908** | -60 | | | V |
| | | | for **BD910** | -80 | | | V |
| | | | for **BD912** | -100 | | | V |
| $V_{CE\ (sat)}$* | Collector-emitter saturation voltage | $I_C$ = -5A | $I_B$ = -0.5A | | | -1 | V |
| | | $I_C$ = -10A | $I_B$ = -2.5A | | | -3 | V |
| $V_{BE\ (sat)}$* | Base-emitter saturation voltage | $I_C$ = -10A | $I_B$ = -2.5A | | | -2.5 | V |
| $V_{BE}$* | Base-emitter voltage | $I_C$ = -5A | $V_{CE}$ = -4V | | | -1.5 | V |
| $h_{FE}$* | DC current gain | $I_C$ = -0.5A | $V_{CE}$ = -4V | 40 | | 250 | — |
| | | $I_C$ = -5A | $V_{CE}$ = -4V | 15 | | 150 | — |
| | | $I_C$ = -10A | $V_{CE}$ = -4V | 5 | | | — |
| $f_T$ | Transition frequency | $I_C$ = -0.5A | $V_{CE}$ = -4V | 3 | | | MHz |

* Pulsed: pulse duration = 300 μs, duty cycle = 1.5%

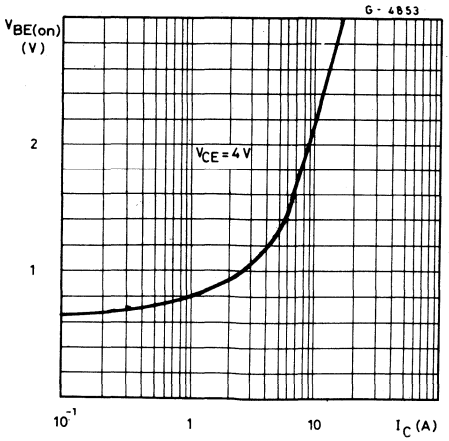
## Safe operating areas



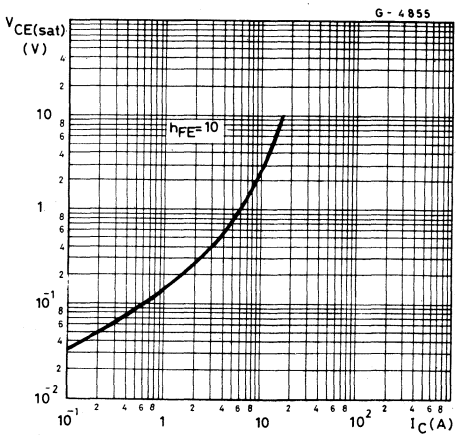

## DC current gain



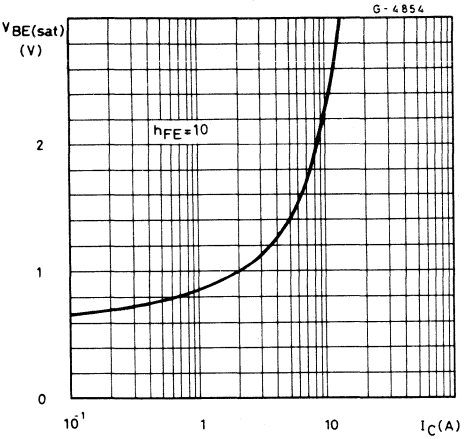

## DC transconductance



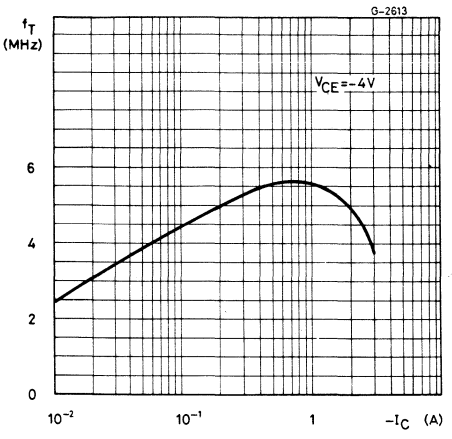

## Collector-emitter saturation voltage



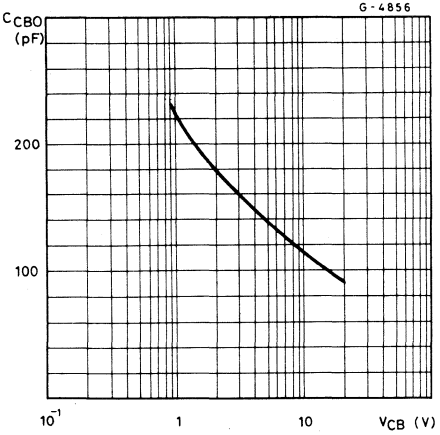
## Base-emitter saturation voltage



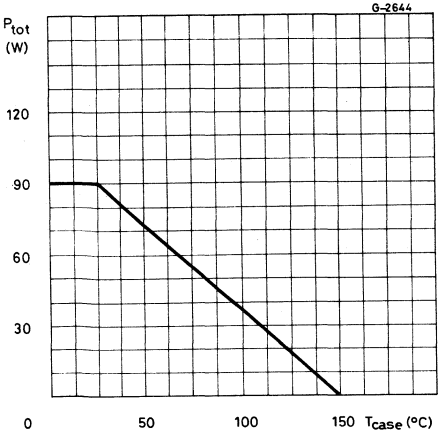

## Transition frequency




## Collector-base capacitance




## Power rating chart



# BU326

# MULTIEPITAXIAL MESA NPN

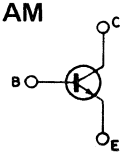
## HIGH VOLTAGE POWER SWITCH

The BU 326 is a silicon multiepitaxial mesa NPN transistor in a Jedec TO-3 metal case particularly intended for switch-mode CTV supply system.

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{CES}$ | Collector-emitter voltage ($V_{BE}=0$) | 800 | V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B=0$) | 375 | V |
| $V_{EBO}$ | Base-emitter voltage ($I_C=0$) | 10 | V |
| $I_C$ | Collector current | 6 | A |
| $I_{CM}$ | Collector peak current | 8 | A |
| $I_B$ | Base current | 3 | A |
| $P_{tot}$ | Total power dissipation at $T_{case} \leq 25$ °C | 75 | W |
| $T_{stg}$ | Storage temperature | -65 to 200 | °C |
| $T_j$ | Junction temperature | 200 | °C |

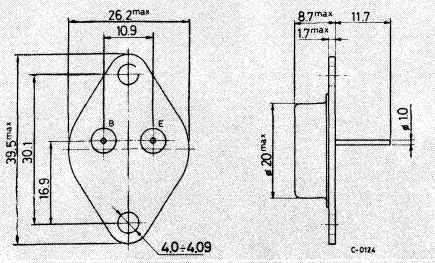
## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm

Collector connected to case




TO-3

## THERMAL DATA

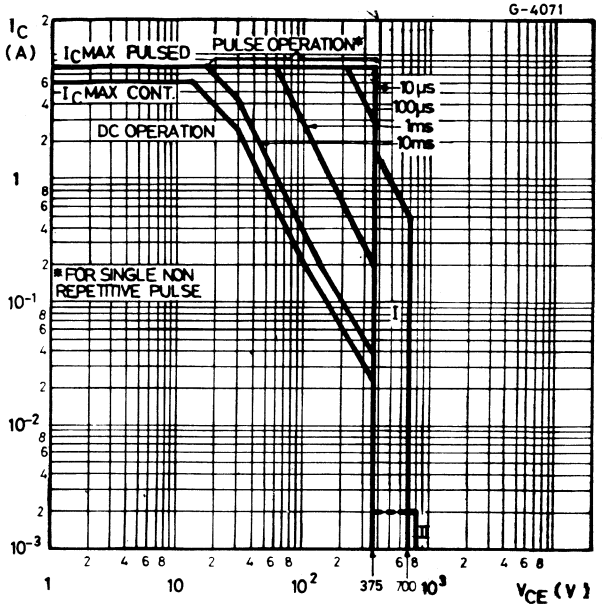
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 2.33 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25 °C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cutoff current ($V_{BE}$=0) | $V_{CE}$=800V<br>$V_{CE}$=800V $T_{case}$=125 °C | | | 1<br>2 | mA<br>mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C$=0) | $V_{EB}$=10V | | | 10 | mA |
| $V_{CEO\ (sus)}$ * | Collector-emitter sustaining voltage ($I_B$ = 0) | $I_C$ =100mA | 325 | | | V |
| $V_{CE\ (sat)}$ * | Collector-emitter saturation voltage | $I_C$ =2.5A $I_B$ =0.5A<br>$I_C$ =4A $I_B$ =1.25A | | | 1.5<br>3 | V<br>V |
| $V_{BE(sat)}$ * | Base-emitter saturation voltage | $I_C$ =2.5A $I_B$ =0.5A<br>$I_C$ =4A $I_B$ =1.25A | | | 1.4<br>1.6 | V<br>V |
| $h_{FE}$* | DC current gain | $I_C$ =1A $V_{CE}$=5V | 25 | | | – |
| $t_{on}$ | Turn-on time | $I_C$ =2.5A $I_{B1}$ =0.5A<br>$V_{CC}$=250V | | | 0.5 | µs |
| $t_s$ | Storage time | $I_C$ =2.5A $I_{B1}$ =0.5A<br>$I_{B2}$ =-1A $V_{CC}$=250V | | | 3.5 | µs |
| $t_f$ | Fall time | $I_C$ =2.5A $I_{B1}$ =0.5A<br>$I_{B2}$ =-1A $V_{CC}$=250V | | | 0.5 | µs |

* Pulsed: pulse duration = 300 µs, duty cycle = 1.5%

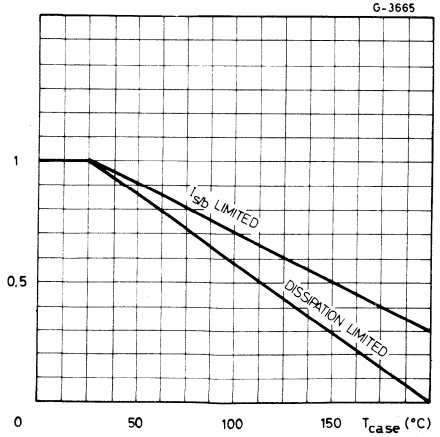
## Safe operating areas



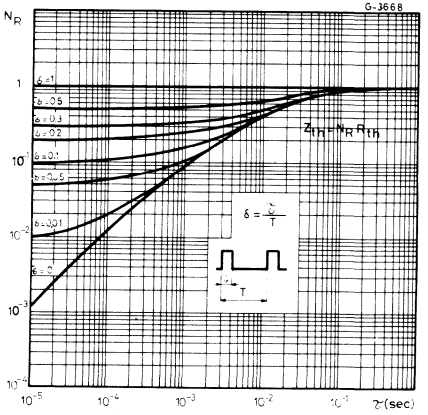

I — Area of permissible operation during turn-on provided $R_{BE} \leq 100\Omega$ and $t_p \leq 0.6$ μs

II — Area of permissible operation with $V_{BE} \leq 0$ and $t_p \leq 2$ μs

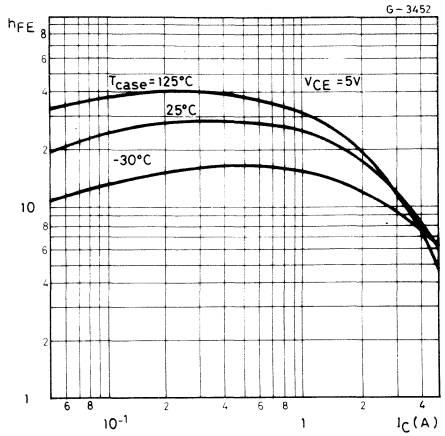
## Derating curves



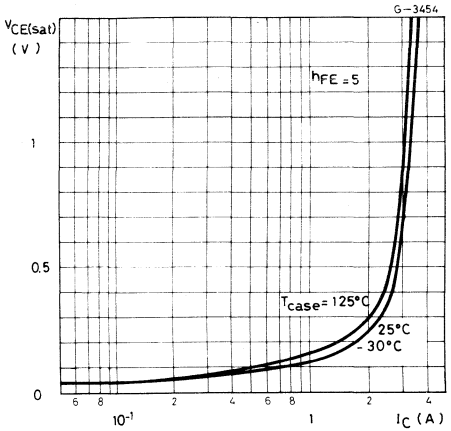

## Thermal transient response



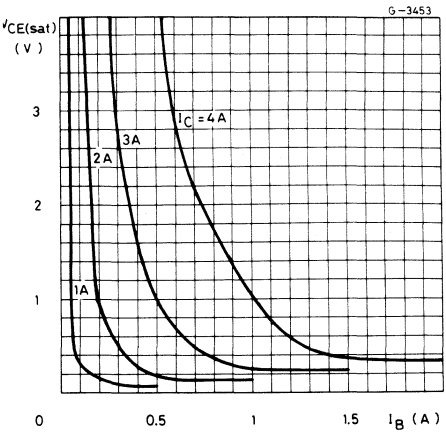
## DC current gain



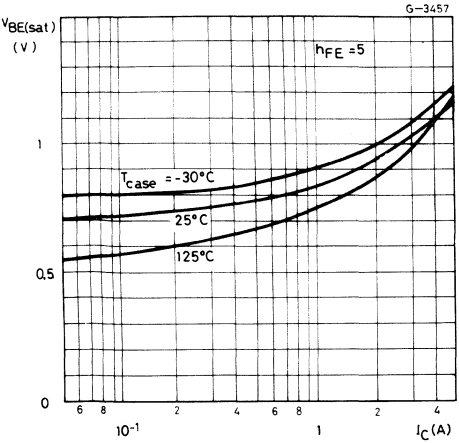

## Collector-emitter saturation voltage



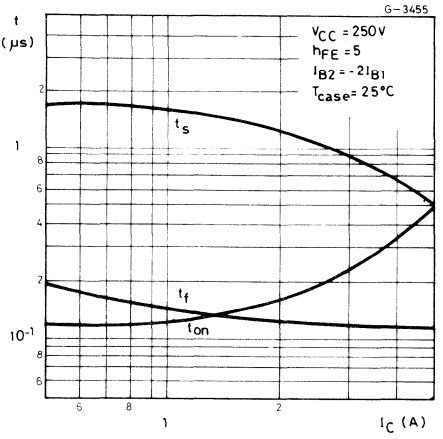

## Collector-emitter saturation voltage



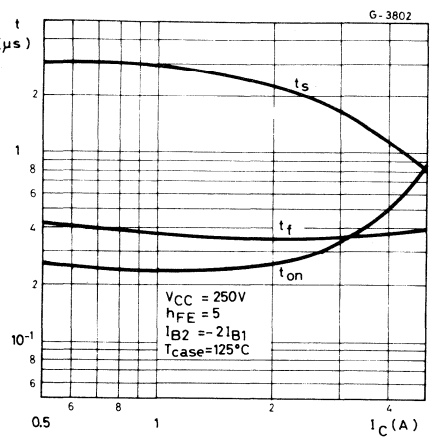

## Base-emitter saturation voltage



Saturated switching characteristics




Saturated switching characteristics



# MULTIEPITAXIAL MESA NPN

**BU326A**

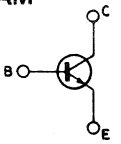
## HIGH VOLTAGE POWER SWITCH

The BU 326A is a silicon multiepitaxial mesa NPN transistor in Jedec TO-3 metal case particularly intended for switch-mode CTV supply system.

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{CES}$ | Collector-emitter voltage ($V_{BE}=0$) | 900 | V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B=0$) | 400 | V |
| $V_{EBO}$ | Emitter-base voltage ($I_C=0$) | 10 | V |
| $I_C$ | Collector current | 6 | A |
| $I_{CM}$ | Collector peak current | 8 | A |
| $I_B$ | Base current | 3 | A |
| $P_{tot}$ | Total power dissipation at $T_{case} \leq 25°C$ | 75 | W |
| $T_{stg}$ | Storage temperature | -65 to 200 | °C |
| $T_j$ | Junction temperature | 200 | °C |

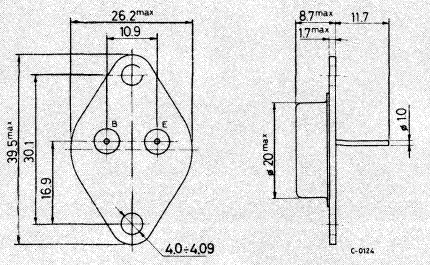
## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm

Collector connected to case




TO-3

## THERMAL DATA

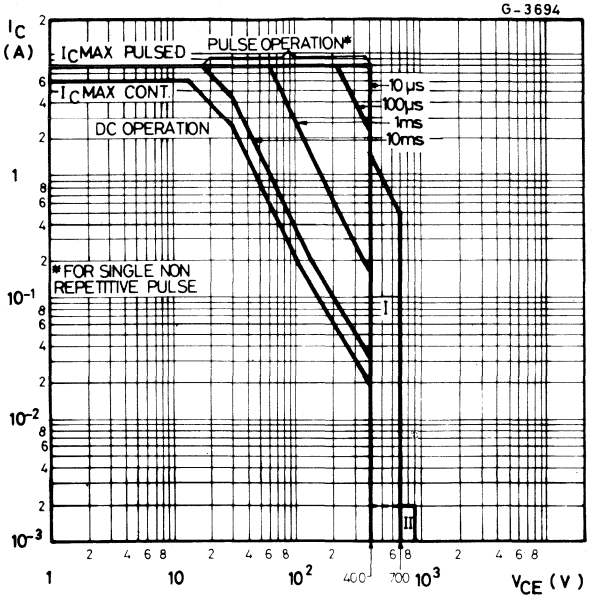
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 2.33 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25 °C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cutoff current ($V_{BE}$=0) | $V_{CE}$=900V<br>$V_{CE}$=900V $T_{case}$=125°C | | | 1<br>2 | mA<br>mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C$=0) | $V_{EB}$=10V | | | 10 | mA |
| $V_{CEO\ (sus)}$* | Collector-emitter sustaining voltage ($I_B$ = 0) | $I_C$ =100mA | 400 | | | V |
| $V_{CE\ (sat)}$* | Collector-emitter saturation voltage | $I_C$ =2.5A $I_B$ =0.5A<br>$I_C$ =4A $I_B$ =1.25A | | | 1.5<br>3 | V<br>V |
| $V_{BE(sat)}$* | Base-emitter saturation voltage | $I_C$ =2.5A $I_B$ =0.5A<br>$I_C$ =4A $I_B$ =1.25A | | | 1.4<br>1.6 | V<br>V |
| $h_{FE}$* | DC current gain | $I_C$ =1A $V_{CE}$=5V | 25 | | | — |
| $t_{on}$ | Turn-on time | $I_C$ =2.5A $I_{B1}$ =0.5A<br>$V_{CC}$=250V | | | 0.5 | µs |
| $t_s$ | Storage time | $I_C$ =2.5A $I_{B1}$ =0.5A<br>$I_{B2}$ =-1A $V_{CC}$=250V | | | 3.5 | µs |
| $t_f$ | Fall time | $I_C$ =2.5A $I_{B1}$ =0.5A<br>$I_{B2}$ =-1A $V_{CC}$=250V | | | 0.5 | µs |

* Pulsed: pulse duration =300 µs, duty cycle =1.5%

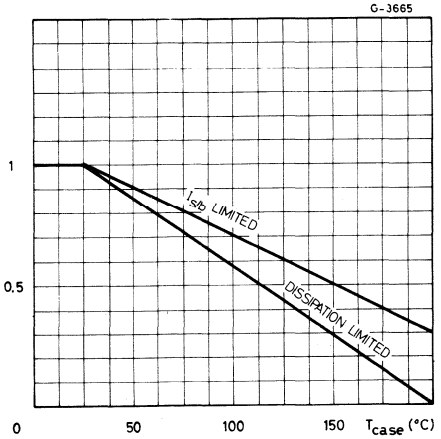
## Safe operating areas



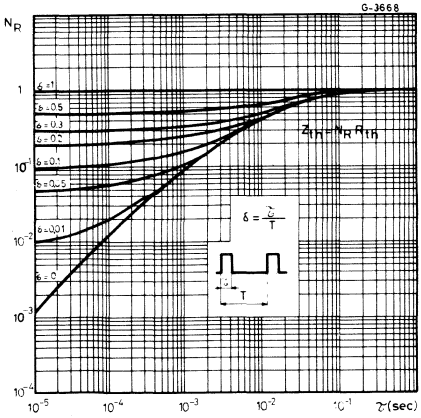

I — Area of permissible operation during turn – on provided $R_{BE}=100\Omega$ and $t_p \leq 0.6$ µs

II— Area of permissible operation with $V_{BE} \leq 0$ and $t_p \leq 2$ µs

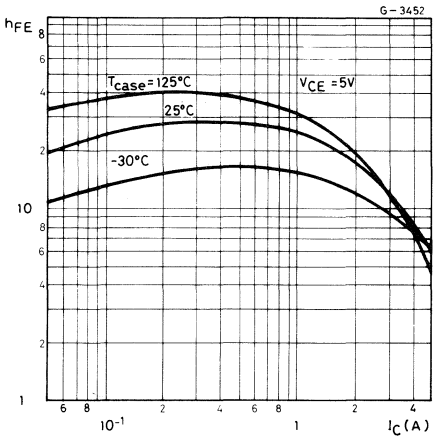
## Derating curves



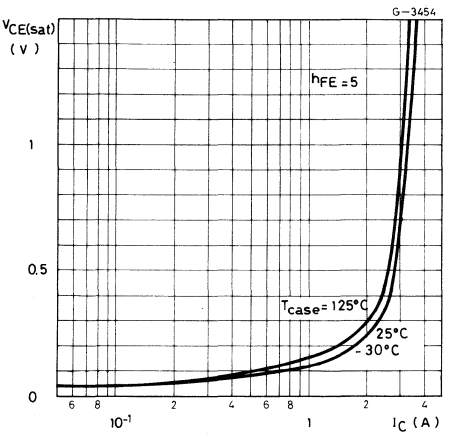

## Thermal transient response



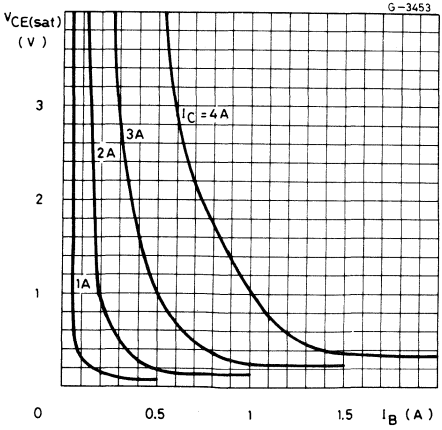
## DC current gain



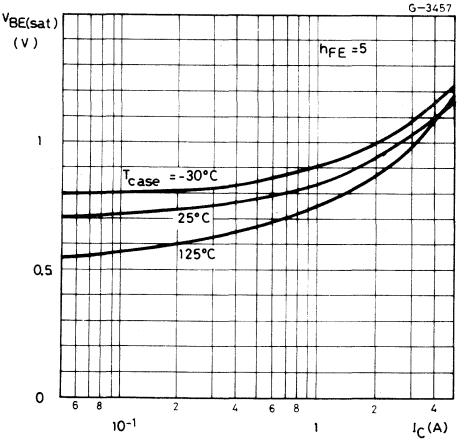

## Collector-emitter saturation voltage



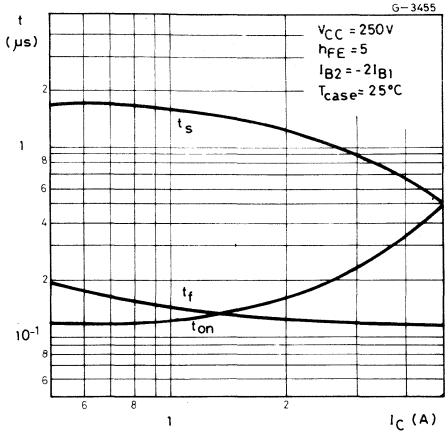

## Collector-emitter saturation voltage



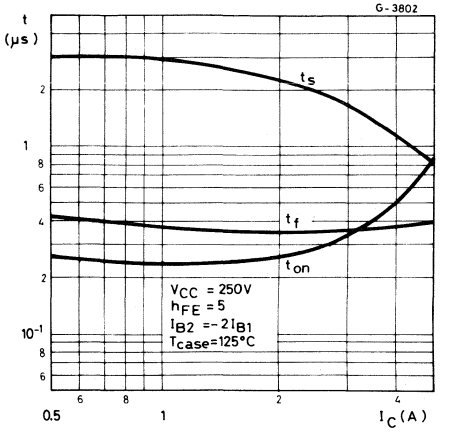

## Base-emitter saturation voltage



Saturated switching characteristics




Saturated switching characteristics



# BU326S

# MULTIEPITAXIAL MESA NPN

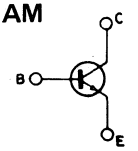
## HIGH VOLTAGE POWER SWITCH

The BU 326S is a silicon multiepitaxial NPN transistor in Jedec TO-3 metal case, particularly intended for switch-mode CTV applications.

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{CES}$ | Collector-emitter voltage ($V_{BE} = 0$) | 800 | V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B = 0$) | 400 | V |
| $V_{EBO}$ | Emitter-base voltage ($I_C = 0$) | 7 | V |
| $I_C$ | Collector current | 6 | A |
| $I_{CM}$ | Collector peak current | 8 | A |
| $I_B$ | Base current | 3 | A |
| $P_{tot}$ | Total power dissipation at $T_{case} \leqslant 75°C$ | 60 | W |
| $T_{stg}$ | Storage temperature | -65 to 175 | °C |
| $T_j$ | Junction temperature | 175 | °C |

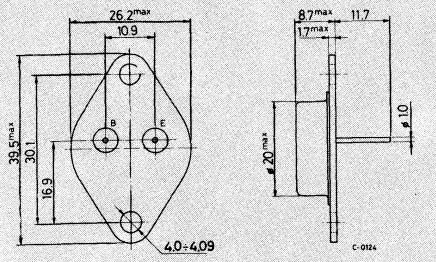
## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm

Collector connected to case




TO-3

## THERMAL DATA

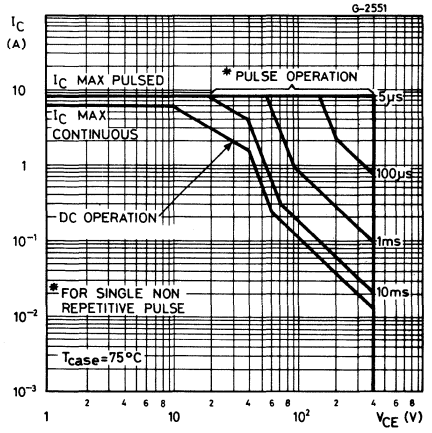
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 1.67 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless otherwise specified)

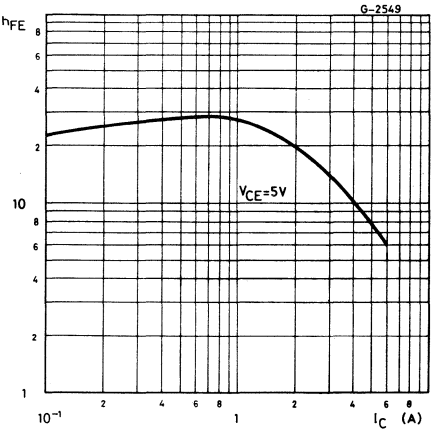
| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cutoff current ($V_{BE}$ = 0) | $V_{CE}$ = 800 V<br>$V_{CE}$ = 800 V $T_{case}$ = 150°C | | | 1<br>3 | mA<br>mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C$ = 0) | $V_{EB}$ = 7 V | | | 1 | mA |
| $V_{CEO\ (sus)}$* | Collector-emitter sustaining voltage ($I_B$ = 0) | $I_C$ = 100mA | 400 | | | V |
| $V_{CE\ (sat)}$* | Collector-emitter saturation voltage | $I_C$ = 2.5A $I_B$ = 0.5A<br>$I_C$ = 4A $I_B$ = 1.25A | | | 1.5<br>3 | V<br>V |
| $V_{BE\ (sat)}$* | Base-emitter saturation voltage | $I_C$ = 2.5A $I_B$ = 0.5A<br>$I_C$ = 4A $I_B$ = 1.25A | | | 1.4<br>1.8 | V<br>V |
| $h_{FE}$* | DC current gain | $I_C$ = 4 A $V_{CE}$ = 5V | 3.5 | 10 | | — |
| $f_T$ | Transition frequency | $I_C$ = 0.5A $V_{CE}$ = 10V | | 20 | | MHz |
| $t_{on}$ | Turn-on time | $I_C$ = 2.5A $V_{CC}$ = 250V<br>$I_{B1}$ = 0.5A | | | 0.3 | μs |
| $t_s$ | Storage time | $I_C$ = 2.5A $V_{CC}$ = 250V<br>$I_{B1}$ = 0.5A $I_{B2}$ = -1A | | | 1.8 | μs |
| $t_f$ | Fall time | | | | 0.3 | μs |

* Pulsed: pulse duration = 300 μs, duty cycle = 1.5%

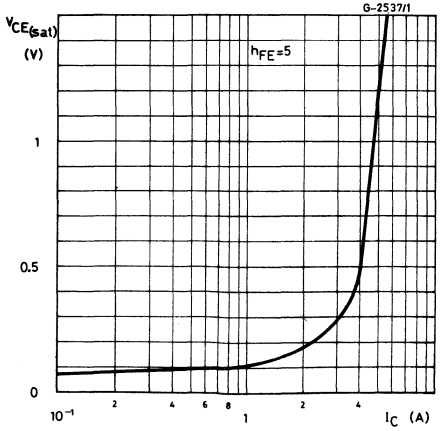
## Safe operating areas



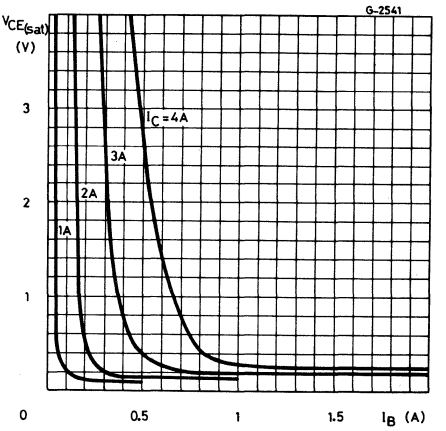

## DC current gain



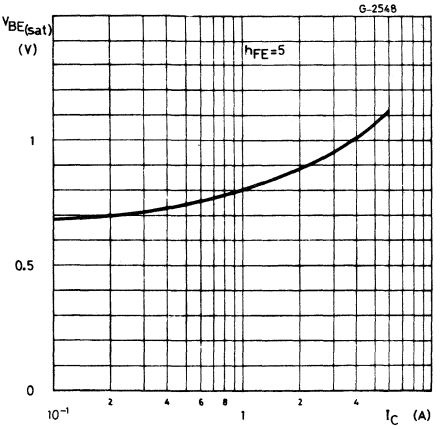

## Collector-emitter saturation voltage



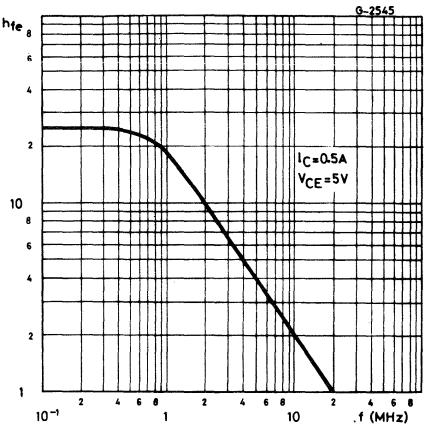

## Collector-emitter saturation voltage



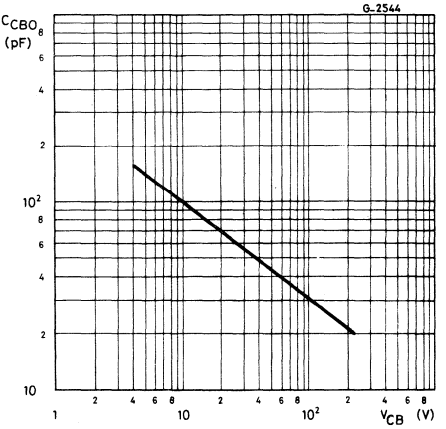
## Base-emitter saturation voltage



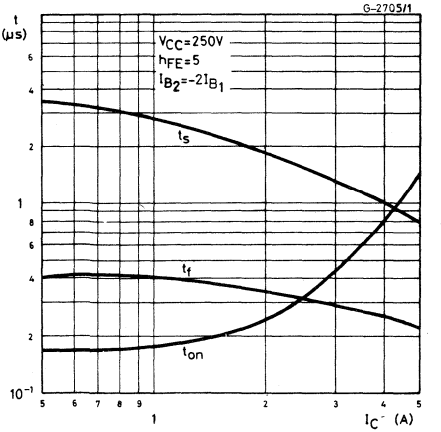

## Small signal current gain




## Collector-base capacitance




## Saturated switching characteristics



BU406
BU406H
BU408

# EPITAXIAL PLANAR NPN

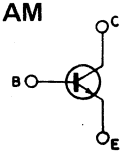
## HORIZONTAL TV DEFLECTORS

The BU 406, BU 406H and BU 408 are silicon epitaxial planar NPN transistors in Jedec TO-220 plastic package. They are fast switching, high voltage devices for use in horizontal deflection output stages of large screen MTV receivers with 110° CRT.

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{CBO}$ | Collector-base voltage ($I_E = 0$) | 400 | V |
| $V_{CEV}$ | Collector-emitter voltage ($V_{BE} = -1.5V$) | 400 | V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B = 0$) | 200 | V |
| $V_{EBO}$ | Emitter-base voltage ($I_C = 0$) | 6 | V |
| $I_C$ | Collector current | 7 | A |
| $I_{CM}$ | Collector peak current (repetitive) | 10 | A |
| $I_{CM}$ | Collector peak current (t = 10 ms) | 15 | A |
| $I_B$ | Base current | 4 | A |
| $P_{tot}$ | Total power dissipation at $T_{case} \leqslant 25$ °C | 60 | W |
| $T_{stg}$ | Storage temperature | -65 to 150 | °C |
| $T_j$ | Junction temperature | 150 | °C |

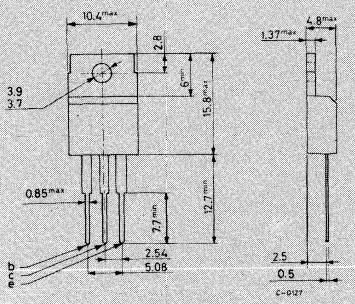
## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm

Collector connected to tab.




TO-220

## THERMAL DATA

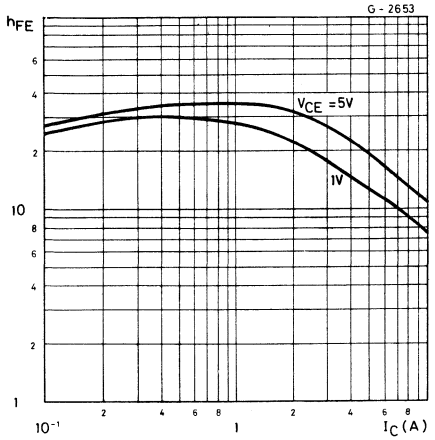
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 2.08 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless otherwise specified)

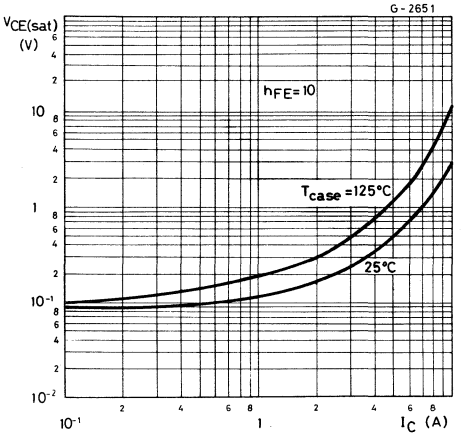
| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cutoff current ($V_{BE}$ = 0) | $V_{CE}$ = 400 V | | | 5 | mA |
| | | $V_{CE}$ = 250 V | | | 100 | μA |
| | | $V_{CE}$ = 250 V $T_{case}$ = 150°C | | | 1 | mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C$ = 0) | $V_{EB}$ = 6 V | | | 1 | mA |
| $V_{CE\ (sat)}$* | Collector-emitter saturation voltage | for **BU406** | | | | |
| | | $I_C$ = 5 A $I_B$ = 0.5 A | | | 1 | V |
| | | for **BU406H** | | | | |
| | | $I_C$ = 5 A $I_B$ = 0.8 A | | | 1 | V |
| | | for **BU408** | | | | |
| | | $I_C$ = 6 A $I_B$ = 1.2 A | | | 1 | V |
| $V_{BE\ (sat)}$* | Base-emitter saturation voltage | for **BU406** | | | | |
| | | $I_C$ = 5 A $I_B$ = 0.5 A | | | 1.2 | V |
| | | for **BU406H** | | | | |
| | | $I_C$ = 5 A $I_B$ = 0.8 A | | | 1.2 | V |
| | | for **BU408** | | | | |
| | | $I_C$ = 6 A $I_B$ = 1.2 A | | | 1.5 | V |
| $f_T$ | Transition frequency | $I_C$ = 0.5 A $V_{CE}$ = 10 V | 10 | | | MHz |
| $t_{off}$** | Turn-off time | for **BU406** | | | | |
| | | $I_C$ = 5 A $I_{B\ end}$ = 0.5A | | | 0.75 | μs |
| | | for **BU406H** | | | | |
| | | $I_C$ = 5 A $I_{B\ end}$ = 0.8A | | | 0.4 | μs |
| | | for **BU408** | | | | |
| | | $I_C$ = 6 A $I_{B\ end}$ = 1.2A | | | 0.4 | μs |
| $I_{s/b}$ | Second breakdown collector current | $V_{CE}$ = 40 V t = 10ms | 4 | | | A |

* Pulsed: pulse duration = 300 μs, duty cycle = 1.5%
** See test circuit

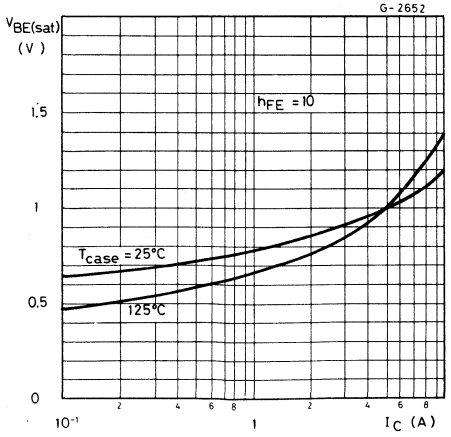
## DC current gain



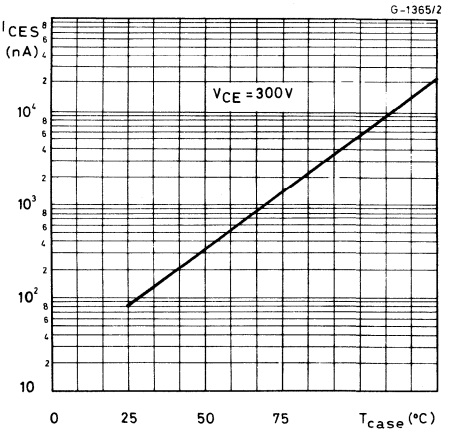

## Collector-emitter saturation voltage



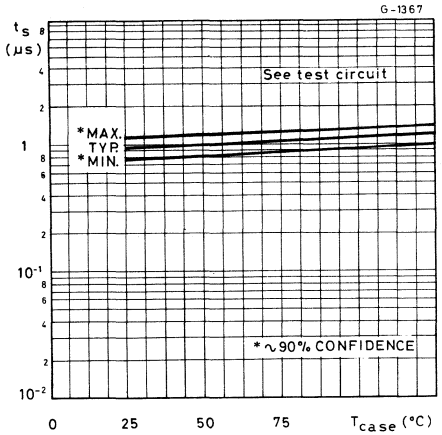

## Base-emitter saturation voltage



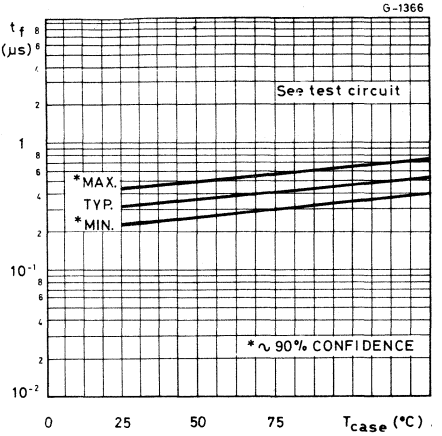

## Collector cutoff current



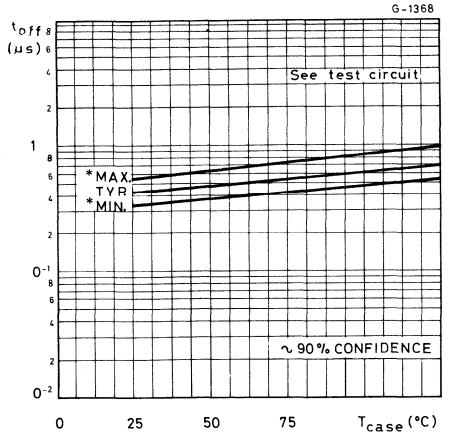
## Storage time




## Fall time

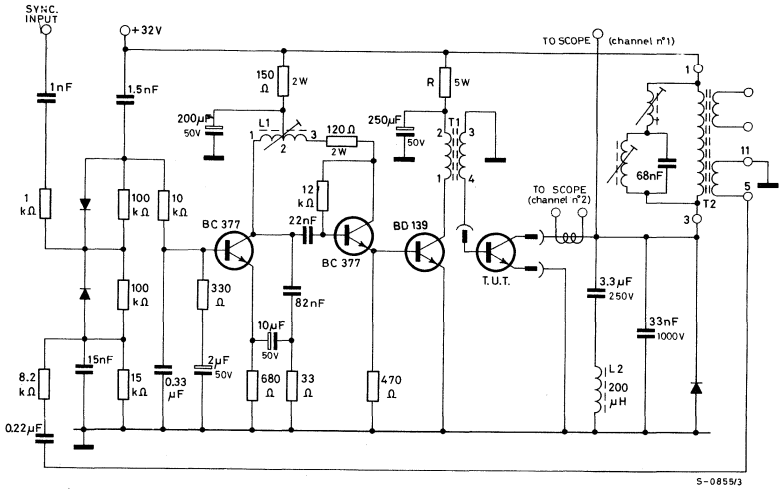



## Turn-off time



## SWITCHING TIMES

Test circuit (fall, storage and turn-off time)




L1 Horizontal hold coil: Pins 1-2=75 turns Ø 0.2 mm; R=1.5 Ω; L min = 0.62 mH
Pins 2-3=293 turns Ø 0.2 mm; R=4.8 Ω; L max = 4.1 mH Core = siferrit B62120 25X4X2

L2 Horizontal yoke = 200 µH

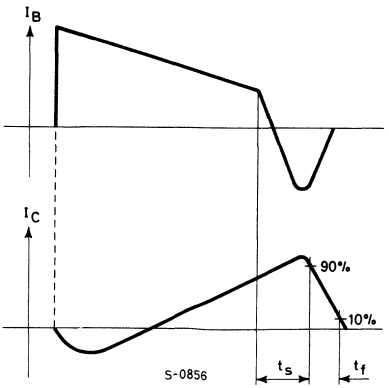
T1 Driver transformer: Pins 1-2=125 turns Ø 0.2 mm;
Pins 3-4=25 turns Ø 0.4 mm; Gap = 0.12 mm; Core = 3E3 double E 19x15x5

T2 EHT transformer manufacturer ARCO type 249.065/035

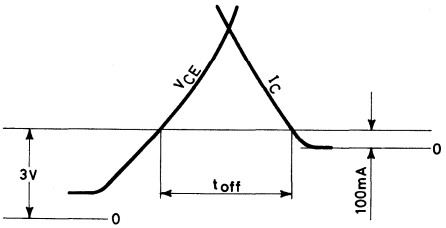
R = 330Ω for BU406
R = 220Ω for BU406H
R = 180Ω for BU408

Waveforms

Fall and storage time




Turn-off time

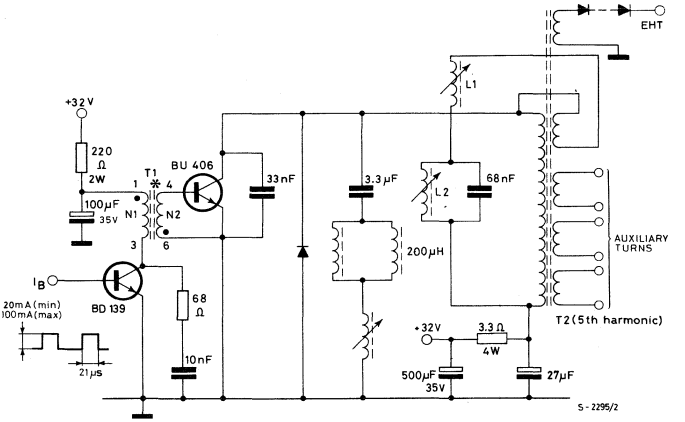



Turn-off time is the time for the collector current $I_C$ to decrease to 100 mA after the collector to emitter voltage $V_{CE}$ has risen 3V into its flyback excursion

S-0857

## APPLICATION INFORMATION

BU 406 - application circuit for 17'' to 24'' - 110° - 28 mm neck picture tubes




*N1=125 turns ø 0.3mm ; N2=25 turns ø 0.6mm ; GAP=0.12mm ; CORE=DOUBLE E 19x5x8 mm;FERRITE 3E1 TYPE

# BU406D
# BU407D
# BU408D

# EPITAXIAL PLANAR NPN

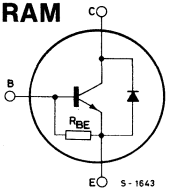
## HORIZONTAL TV DEFLECTORS

The BU 406D, BU 407D and BU 408D are silicon planar epitaxial NPN transistors with integrated damper diode, in Jedec TO-220 plastic package. They are fast switching, high voltage devices for use in horizontal deflection output stages of MTV receivers with 110° CRT.
The BU 406D and BU 408D are primarily intended for large screen, while the BU 407D is for medium and small screens.

## ABSOLUTE MAXIMUM RATINGS

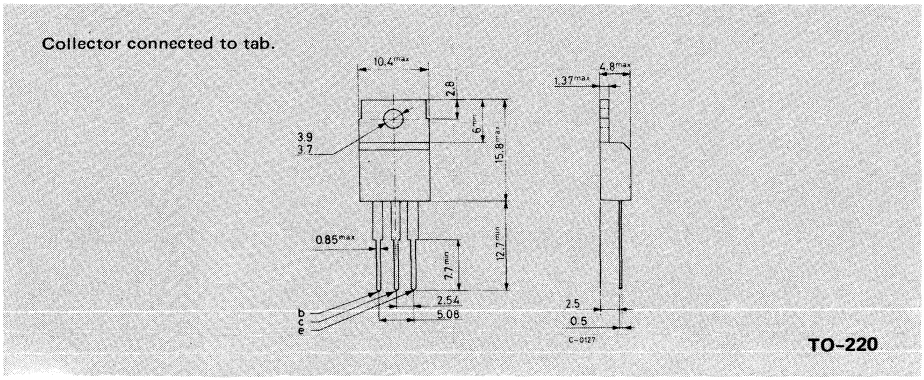
| | | BU406D | BU407D | BU408D |
|---|---|---|---|---|
| $V_{CBO}$ | Collector-base voltage ($I_E = 0$) | 400V | 330V | 400V |
| $V_{CEV}$ | Collector-emitter voltage ($V_{BE} = -1.5V$) | 400V | 330V | 400V |
| $V_{EBO}$ | Emitter-base voltage ($I_C = 0$) | 6V | | |
| $I_C$ | Collector current | 7A | | |
| $I_{CM}$ | Collector peak current (repetitive) | 10A | | |
| $I_{CM}$ | Collector peak current (t = 10 ms) | 15A | | |
| $I_B$ | Base current | 4A | | |
| $P_{tot}$ | Total power dissipation at $T_{case} \leqslant 25$ °C | 60W | | |
| $T_{stg}$ | Storage temperature | -65 to 150 °C | | |
| $T_j$ | Junction temperature | 150 °C | | |

## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm



## THERMAL DATA

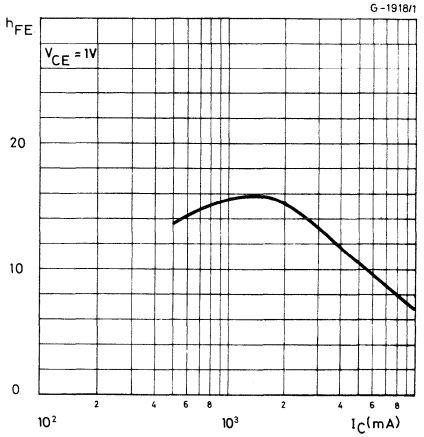
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 2.08 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless otherwise specified)

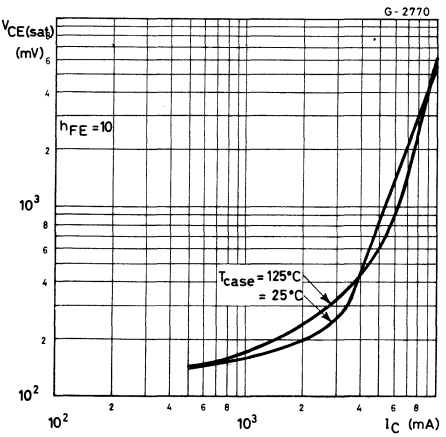
| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CEV}$ | Collector cutoff current ($V_{BE}$ = -1.5V) | for **BU406D** and **BU408D**<br>$V_{CE}$ = 400 V<br>for **BU407D**<br>$V_{CE}$ = 330 V | | | 15<br><br>15 | mA<br><br>mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C$ = 0) | $V_{EB}$ = 6 V | | | 400 | mA |
| $V_{CE\ (sat)}$* | Collector-emitter saturation voltage | for **BU406D** and **BU407D**<br>$I_C$ = 5 A $I_B$ = 0.65A<br>for **BU408D**<br>$I_C$ = 6 A $I_B$ = 1.2 A | | | 1<br><br>1 | V<br><br>V |
| $V_{BE\ (sat)}$* | Base-emitter saturation voltage | for **BU406D** and **BU407D**<br>$I_C$ = 5 A $I_B$ = 0.65A<br>for **BU408D**<br>$I_C$ = 6 A $I_B$ = 1.2 A | | | 1.3<br><br>1.5 | V<br><br>V |
| $f_T$ | Transition frequency | $I_C$ = 0.5 A $V_{CE}$ = 10 V | 10 | | | MHz |
| $t_{off}$ | Turn-off time | for **BU406D** and **BU407D**<br>$I_C$ = 5 A $I_{B\ end}$ = 0.65A<br>for **BU408D**<br>$I_C$ = 6 A $I_{B\ end}$ = 1.2A | | | 0.75<br><br>0.5 | µs<br><br>µs |
| $I_{s/b}$ | Second breakdown collector current | $V_{CE}$ = 40 V t = 10 ms | 4 | | | A |
| $V_F$ | Diode forward voltage | $I_F$ = 5 A | | | 1.5 | V |

* Pulsed: pulse duration = 300 µs, duty cycle = 1.5%

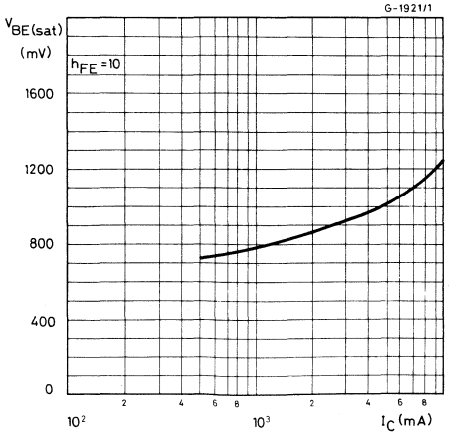
## DC current gain



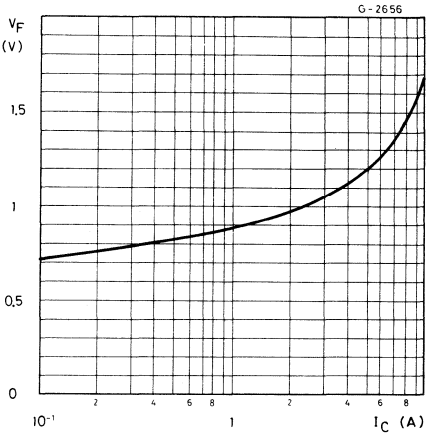

## Collector-emitter saturation voltage




## Base-emitter saturation voltage

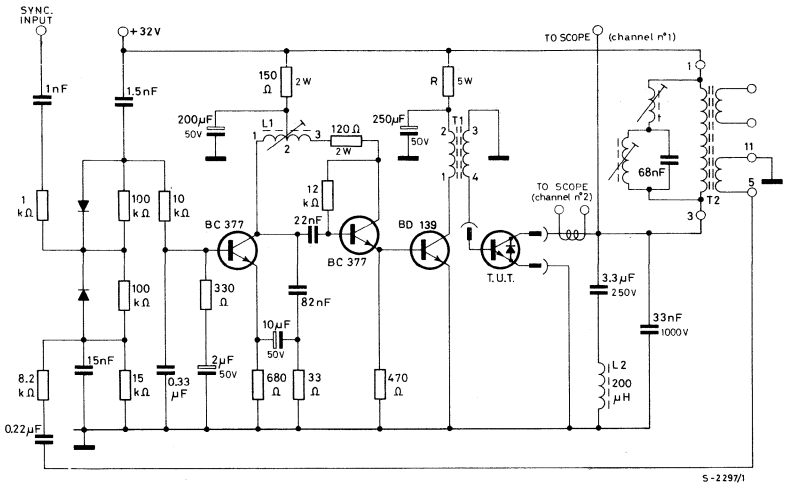



## Forward voltage



## SWITCHING TIMES

Test circuit (fall, storage and turn-off time)




L1 Horizontal hold coil: Pins 1-2=75 turns Ø 0.2 mm; R=1.5 Ω; L min = 0.62 mH
Pins 2-3=293 turns Ø 0.2 mm; R=4.8 Ω; L max = 4.1 mH Core = siferrit B 62120 25×4×2

L2 Horizontal yoke = 200 µH

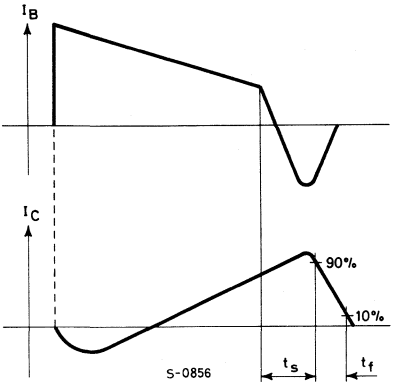
T1 Driver transformer: Pins 1-2=125 turns Ø 0.2 mm;
Pins 3-4=25 turns Ø 0.4 mm; Gap = 0.12 mm; Core = 3E3 double E 19×15×5

T2 EHT transformer manufacturer ARCO type 249.065/035

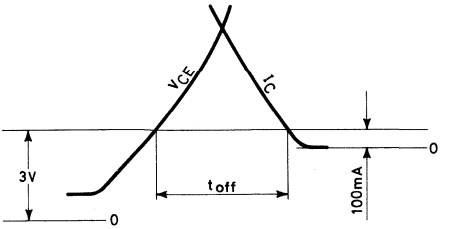
R = 270 Ω for BU406D and BU407D
R = 180 Ω for BU408D

Waveforms

Fall and storage time




Turn-off time



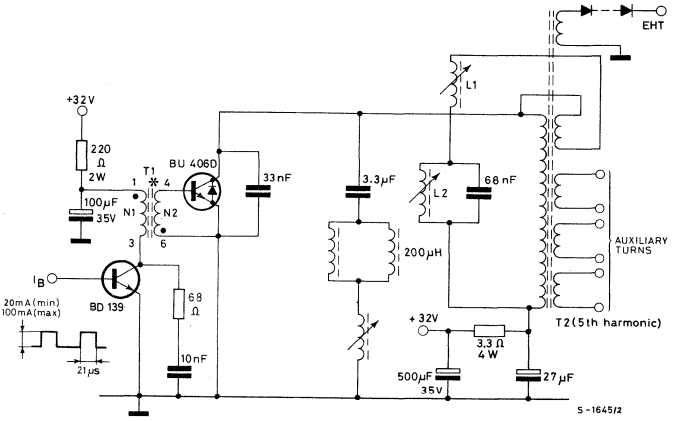

Turn-off time is the time for the collector current $I_C$ to decrease to 100 mA after the collector to emitter voltage $V_{CE}$ has risen 3V into its flyback excursion

S-0857

## APPLICATION INFORMATION

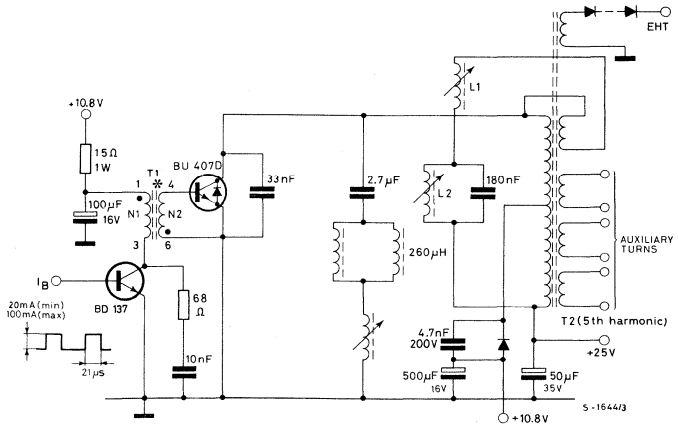
Two examples are given of the BU 406D and BU 407D in conventional MTV horizontal deflection circuits.

BU 406D - application circuit for 17'' to 24'' - 110° - 28 mm neck picture tubes




*N1=125 turns ø 0.3mm; N2=25 turns ø 0.6mm; GAP=0.12mm; CORE=DOUBLE E 19x5x8 mm;FERRITE 3E1 TYPE

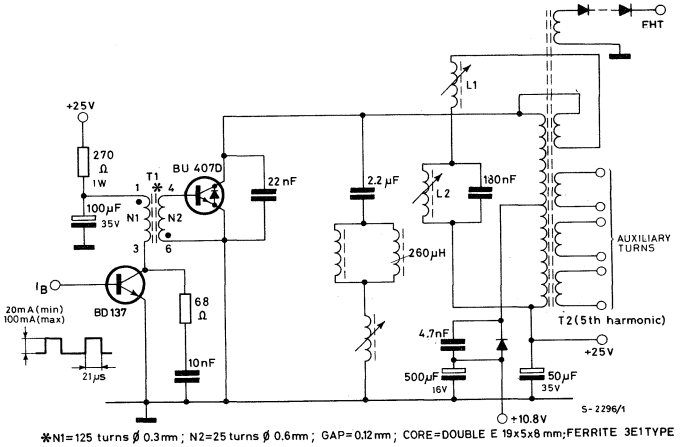
BU 407D - application circuit for 12'' to 17'' - 110° - 20 mm neck picture tubes
(driver supply voltage = 10.8 V)




*N1= 90 turns ø 0.3mm; N2=30 turns ø 0.6mm; GAP=0.12mm; CORE=DOUBLE E 19x5x8 mm;FERRITE 3E1 TYPE

**APPLICATION INFORMATION** (continued)

BU 407D - application circuit for 12'' to 17'' - 110° - 20 mm neck picture tubes
(driver supply voltage = 25 V)




*N1=125 turns ø 0.3mm ; N2=25 turns ø 0.6mm ; GAP=0.12mm ; CORE=DOUBLE E 19x5x8 mm;FERRITE 3E1 TYPE

# BU407
# BU407H

# EPITAXIAL PLANAR NPN

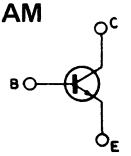
## HORIZONTAL TV DEFLECTORS

The BU 407 and BU 407H are silicon epitaxial planar NPN transistors in Jedec TO-220 plastic package.
They are fast switching, high voltage devices for use in horizontal deflection output stages of medium and small screens MTV receivers with 110° CRT.

## ABSOLUTE MAXIMUM RATINGS

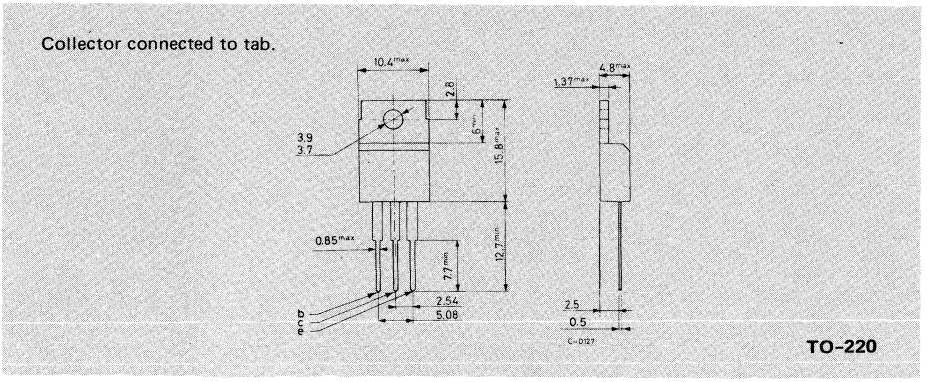
| | | | |
|---|---|---|---|
| $V_{CBO}$ | Collector-base voltage ($I_E = 0$) | 330 | V |
| $V_{CEV}$ | Collector-emitter voltage ($V_{BE} = -1.5V$) | 330 | V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B = 0$) | 150 | V |
| $V_{EBO}$ | Emitter-base voltage ($I_C = 0$) | 6 | V |
| $I_C$ | Collector current | 7 | A |
| $I_{CM}$ | Collector peak current (repetitive) | 10 | A |
| $I_{CM}$ | Collector peak current (t = 10 ms) | 15 | A |
| $I_B$ | Base current | 4 | A |
| $P_{tot}$ | Total power dissipation at $T_{case} \leq 25$ °C | 60 | W |
| $T_{stg}$ | Storage temperature | -65 to 150 | °C |
| $T_j$ | Junction temperature | 150 | °C |

## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm



## THERMAL DATA

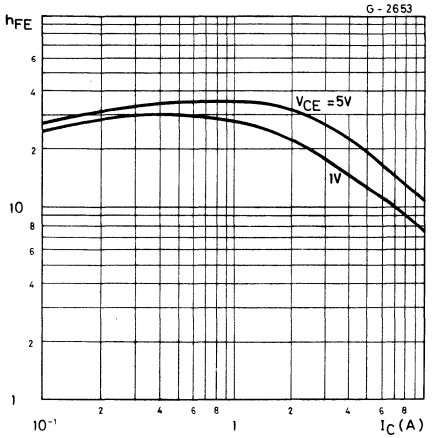
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 2.08 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25 °C unless otherwise specified)

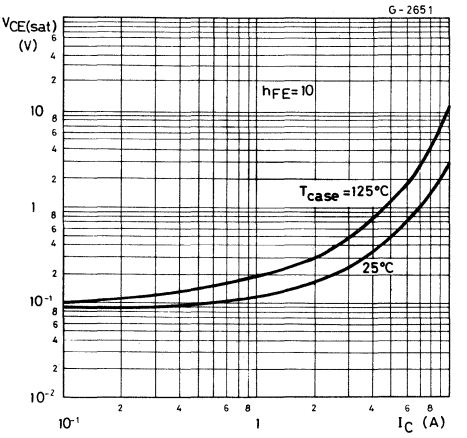
| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cutoff current ($V_{BE} = 0$) | $V_{CE}$ = 330V | | | 5 | mA |
| | | $V_{CE}$ = 200V | | | 100 | μA |
| | | $V_{CE}$ = 200V $T_{case}$ = 150°C | | | 1 | mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C = 0$) | $V_{EB}$ = 6 V | | | 1 | mA |
| $V_{CE\ (sat)}$* | Collector-emitter saturation voltage | for **BU407** | | | | |
| | | $I_C$ = 5 A $I_B$ = 0.5A | | | 1 | V |
| | | for **BU407H** | | | | |
| | | $I_C$ = 5 A $I_B$ = 0.8A | | | 1 | V |
| $V_{BE\ (sat)}$* | Base-emitter saturation voltage | for **BU407** | | | | |
| | | $I_C$ = 5 A $I_B$ = 0.5A | | | 1.2 | V |
| | | for **BU407H** | | | | |
| | | $I_C$ = 5 A $I_B$ = 0.8A | | | 1.2 | V |
| $f_T$ | Transition frequency | $I_C$ = 0.5 A $V_{CE}$ = 10 V | 10 | | | MHz |
| $t_{off}$** | Turn-off time | for **BU407** | | | | |
| | | $I_C$ = 5 A $I_{B\ end}$ = 0.5A | | | 0.75 | μs |
| | | for **BU407H** | | | | |
| | | $I_C$ = 5 A $I_{B\ end}$ = 0.8A | | | 0.4 | μs |
| $I_{s/b}$ | Second breakdown collector current | $V_{CE}$ = 40 V t = 10ms | | 4 | | A |

* Pulsed: pulse duration = 300 μs, duty cycle = 1.5%
** See test circuit

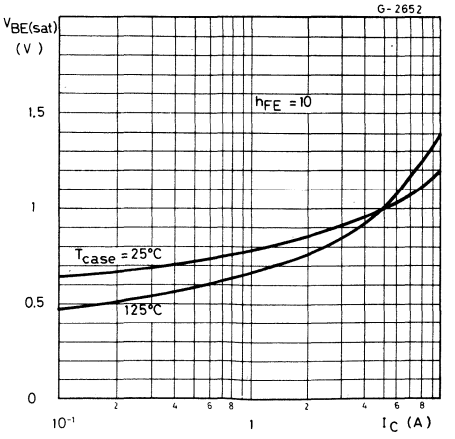
## DC current gain



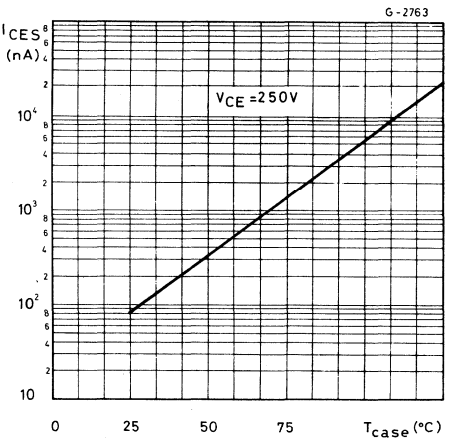

## Collector-emitter saturation voltage



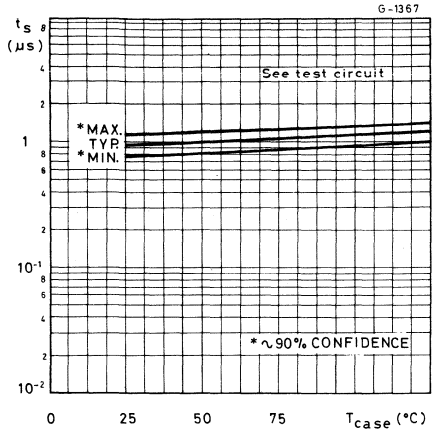

## Base-emitter saturation voltage



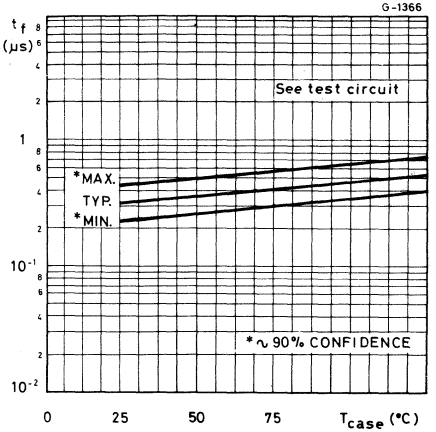

## Collector cutoff current



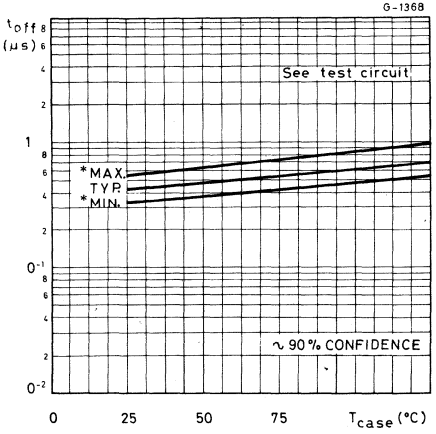
## Storage time




## Fall time

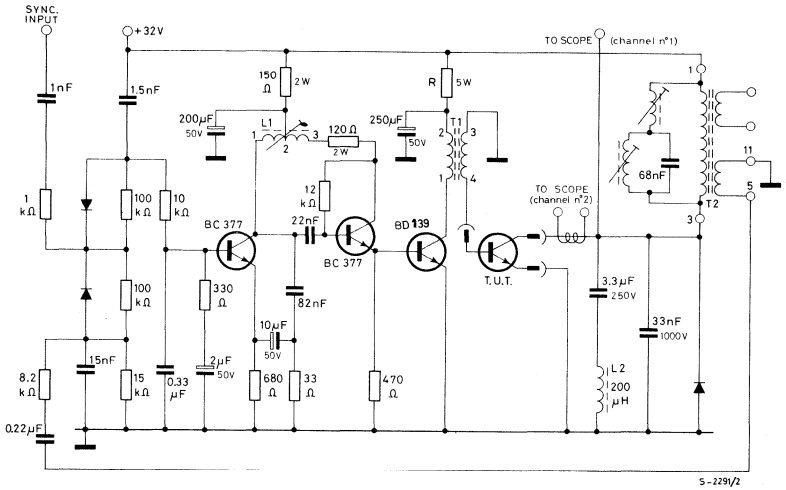



## Turn-off time



## SWITCHING TIMES

Test circuit (fall, storage and turn-off time)




L1 Horizontal hold coil: Pins 1-2=75 turns Ø 0.2 mm; R=1.5 Ω; L min = 0.62 mH
Pins 2-3=293 turns Ø 0.2 mm; R=4.8 Ω; L max = 4.1 mH Core = siferrit B62120 25X4X2

L2 Horizontal yoke = 200 μH

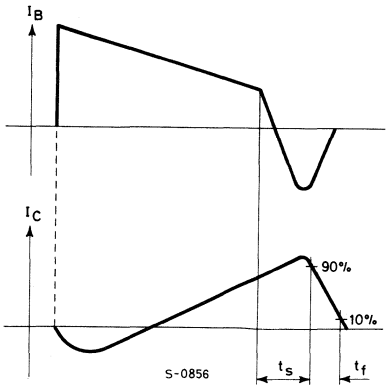
T1 Driver transformer: Pins 1-2=125 turns Ø 0.2 mm;
Pins 3-4=25 turns Ø 0.4 mm; Gap = 0.12 mm; Core = 3E3 double E 19x15x5

T2 EHT transformer manufacturer ARCO type 249.065/035

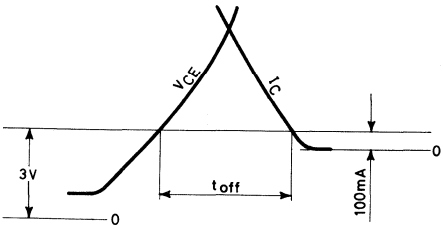
R = 330 Ω for BU407
R = 220 Ω for BU407H

Waveforms

Fall and storage time




Turn-off time



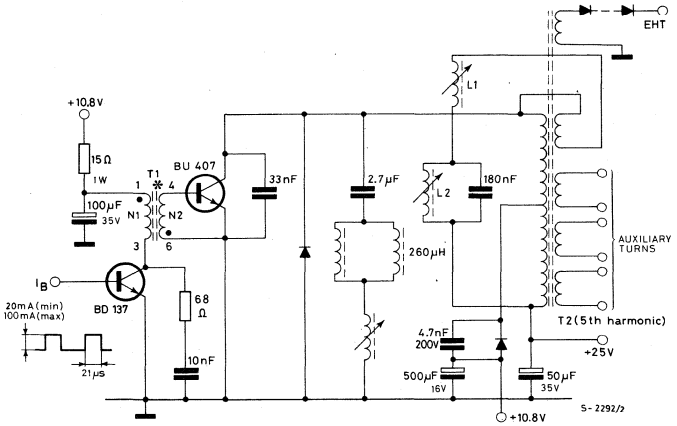

Turn-off time is the time for the collector current $I_C$ to decrease to 100 mA after the collector to emitter voltage $V_{CE}$ has risen 3V into its flyback excursion

S-0857

## APPLICATION INFORMATION

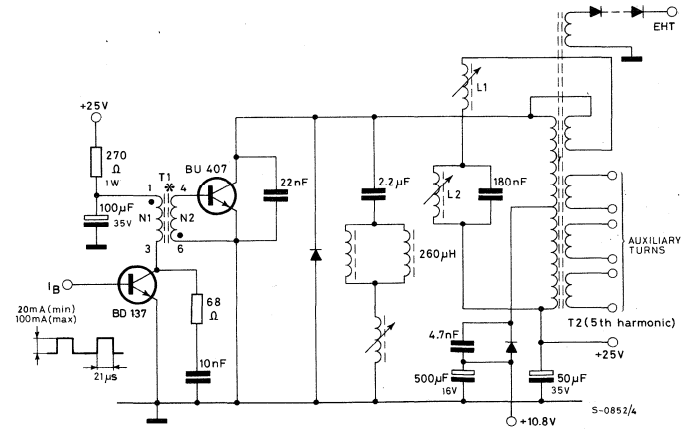
Two examples are given of the BU407 in conventional MTV horizontal deflection circuits

BU 407 - application circuit for 12'' to 17'' - 110° - 20 mm neck picture tubes
(driver supply voltage = 10.8V)




*N1=125 turns ø 0.3mm ; N2=30 turns ø 0.6mm ; GAP=0.12mm ; CORE=DOUBLE E 19x5x8 mm;FERRITE 3E1TYPE

BU 407 - application circuit for 12'' to 17'' - 110° - 20 mm neck picture tubes
(driver supply voltage = 25 V)




*N1=125 turns ø 0.3mm ; N2=25 turns ø 0.6mm ; GAP=0.12mm ; CORE=DOUBLE E 19x5x8 mm;FERRITE 3E1TYPE

# BU426
# BU426A

# MULTIEPITAXIAL MESA NPN

PRELIMINARY DATA

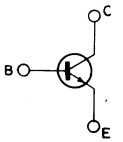
## HIGH VOLTAGE POWER SWITCH

The BU426 and BU426A are silicon multiepitaxial mesa NPN transistors in SOT-93 plastic package, particularly intended for switch-mode CTV supply systems.

## ABSOLUTE MAXIMUM RATINGS

| | | BU426 | BU426A |
|---|---|---|---|
| $V_{CES}$ | Collector-emitter voltage ($V_{BE} = 0$) | 800 V | 900V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B = 0$) | 375V | 400V |
| $V_{EBO}$ | Emitter-base voltage ($I_C = 0$) | 10V | |
| $I_C$ | Collector-current | 6A | |
| $I_{CM}$ | Collector-peak current ($t_p = 2ms$) | 8A | |
| $I_B$ | Base current | 3A | |
| $P_{tot}$ | Total power dissipation at $T_{case} \leqslant 25°C$ | 113W | |
| $T_{stg}$ | Storage temperature | -65°C to 150°C | |
| $T_j$ | Junction temperature | 150°C | |

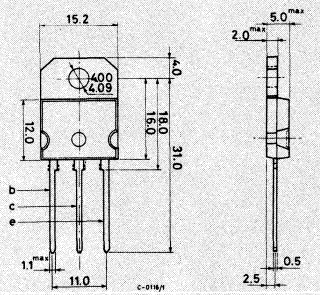
## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm

Collector connected to tab.




(sim. to **TO-218**) **SOT-93**

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max. | 1.1 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless otherwise specified)

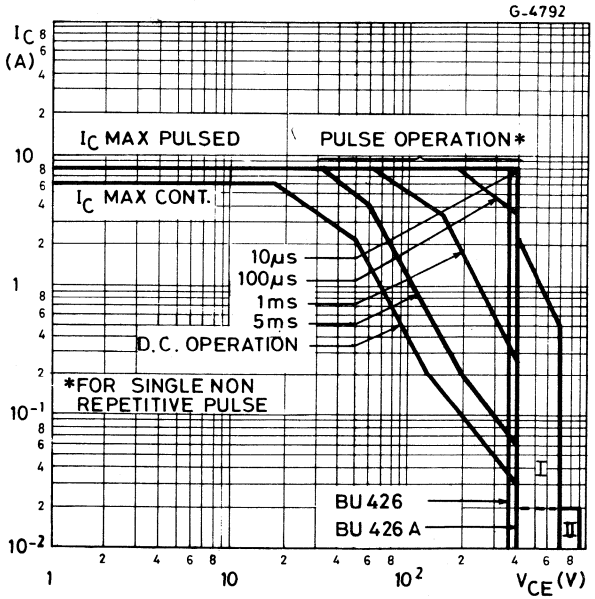
| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cutoff current ($V_{BE}$ = 0) | for **BU426** $V_{CE}$ = 800V | | | 1 | mA |
| | | for **BU426A** $V_{CE}$ = 900V | | | 1 | mA |
| | | $T_{case}$ = 125°C | | | | |
| | | for **BU426** $V_{CE}$ = 800V | | | 2 | mA |
| | | for **BU426A** $V_{CE}$ = 900V | | | 2 | mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C$ = 0) | $V_{EB}$ = 10V | | | 10 | mA |
| $V_{CEO(sus)}$* | Collector-emitter sustaining voltage ($I_B$ = 0) | for **BU426** $I_C$ = 100mA | 375 | | | V |
| | | for **BU426A** $I_C$ = 100mA | 400 | | | V |
| $V_{CE(sat)}$* | Collector-emitter saturation voltage | $I_C$ = 2.5A $I_B$ = 0.5A | | | 1.5 | V |
| | | $I_C$ = 4A $I_B$ = 1.25A | | | 3 | V |
| $V_{BE(sat)}$* | Base-emitter saturation voltage | $I_C$ = 2.5A $I_B$ = 0.5A | | | 1.4 | V |
| | | $I_C$ = 4A $I_B$ = 1.25A | | | 1.6 | V |
| $h_{FE}$* | DC current gain | $I_C$ = 0.6A $V_{CE}$ = 5V | 30 | | 60 | |
| $t_{on}$ | Turn-on time | $I_C$ = 2.5A $I_{B1}$ = 0.5A $V_{CC}$ = 250V | | 0.25 | 0.5 | μs |

## ELECTRICAL CHARACTERISTIC (Continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_s$ | Storage time | $I_C = 2.5A$ $I_{B1} = 0.5A$ $I_{B2} = -1A$ $V_{CC} = 250V$ | | 2.5 | 3.5 | $\mu s$ |
| $t_f$ | Fall time | | | 0.2 | 0.5 | $\mu s$ |
| $t_f$ | Fall time | $I_C = 2.5A$ $I_{B1} = 0.5A$ $I_{B2} = -1A$ $V_{CC} = 250V$ $T_{case} = 100°C$ | | | 0.75 | $\mu s$ |

* Pulsed: pulse duration = 300 $\mu s$ duty cycle = 1.5%.

Safe operating areas




I = Area of permissible operation driving turn-on provided $R_{BE} = 100\Omega$ and $t_p \leqslant 0.6\ \mu s$.
II = Area of permissible operation with $V_{BE} \leqslant 0$; $t_p \leqslant 2\ \mu s$.

# EPITAXIAL PLANAR NPN

**BU806**
**BU807**

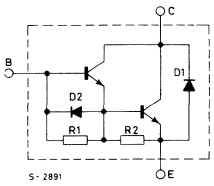
## FAST SWITCHING DARLINGTON TRANSISTORS

The BU 806 and BU 807 are silicon epitaxial planar NPN power Darlington transistors with integrated base-emitter speed-up diode, mounted in Jedec TO-220 plastic package. They are high voltage, high current devices for fast switching applications. In particular they can be used in horizontal output stages of 110° CRT video displays. The BU 806 is primarily intended for large screeen, while the BU 807 is for medium and small screens.

## ABSOLUTE MAXIMUM RATINGS

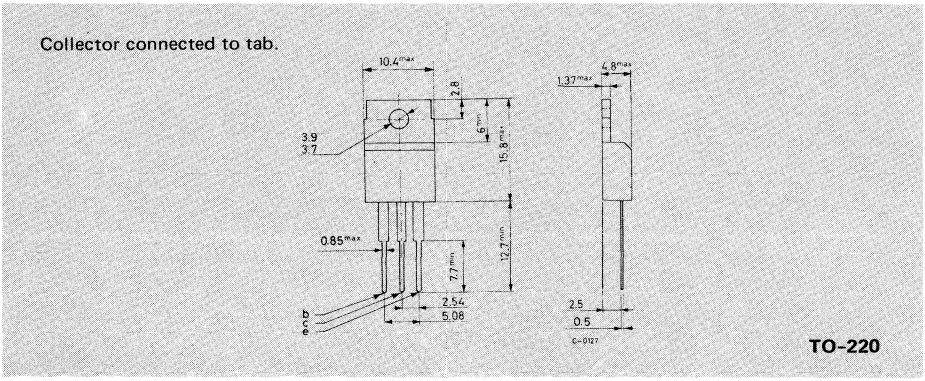
| | | BU 806 | BU 807 |
|---|---|---|---|
| $V_{CBO}$ | Collector-base voltage ($I_E=0$) | 400V | 330V |
| $V_{CEV}$ | Collector-emitter voltage ($V_{BE}=-6V$) | 400V | 330V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B=0$) | 200V | 150V |
| $V_{EBO}$ | Emitter-base voltage ($I_C=0$) | 6V | |
| $I_C$ | Collector current | 8A | |
| $I_{CM}$ | Collector peak current | 15A | |
| $I_{DM}$ | Damper diode peak forward current | 10A | |
| $I_B$ | Base current | 2A | |
| $P_{tot}$ | Total power dissipation at $T_{case} \leq 25°C$ | 60W | |
| $T_{stg}$ | Storage temperature | -65 to 150°C | |
| $T_j$ | Junction temperature | 150°C | |

## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm



## THERMAL DATA

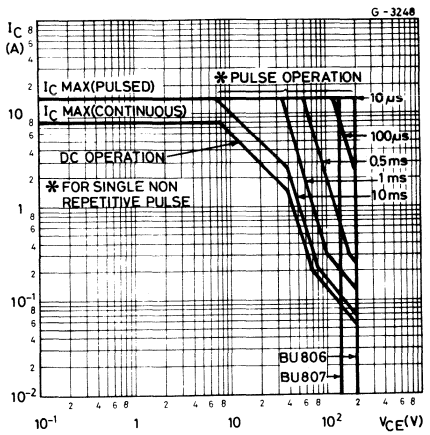
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 2.08 | °C/W |
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-ambient | max | 70 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25 °C unless otherwise specified)

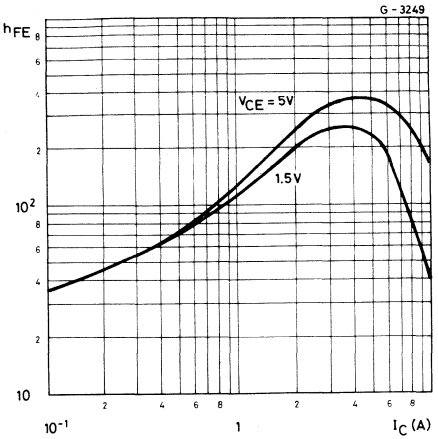
| | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cutoff current ($V_{BE}$=0) | for **BU807** $V_{CE}$=330V<br>for **BU806** $V_{CE}$=400V | | | 100<br>100 | µA<br>µA |
| $I_{CEV}$ | Collector cutoff current ($V_{BE}$=-6V) | for **BU807** $V_{CE}$=330V<br>for **BU806** $V_{CE}$=400V | | | 100<br>100 | µA<br>µA |
| $I_{EBO}$ | Emitter cutoff current ($I_C$=0) | $V_{EB}$=6V | | | 3 | mA |
| $V_{CEO\ (sus)}$ * | Collector-emitter sustaining voltage ($I_B$=0) | $I_C$ =100mA<br>for **BU807**<br>for **BU806** | <br>150<br>200 | | | <br>V<br>V |
| $V_{CE\ (sat)}$ * | Collector-emitter saturation voltage | $I_C$ =5A $I_B$ =50mA | | | 1.5 | V |
| $V_{BE\ (sat)}$ * | Base-emitter saturation voltage | $I_C$ =5A $I_B$ =50mA | | | 2.4 | V |
| $V_F$ * | Damper diode forward voltage | $I_F$ =4A | | | 2 | V |
| $t_{off}$ ** | Turn-off time | $I_C$ =5A $I_{B1}$ =50mA | | 0.4 | 1 | µs |
| $t_{on}$ | Turn-on time | **RESISTIVE LOAD** | | 0.35 | | µs |
| $t_s$ | Storage time | $I_C$ =5A $I_{B1}$ =50mA<br>$I_{B2}$ =-500mA $V_{CC}$=100V | | 0.55 | | µs |
| $t_f$ | Fall time | | | 0.2 | | µs |

* Pulsed: pulse duration = 300µs, duty cycle = 1,5%
** See test circuit

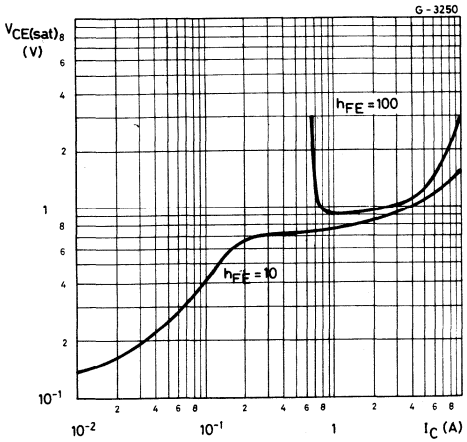
## Safe operating areas



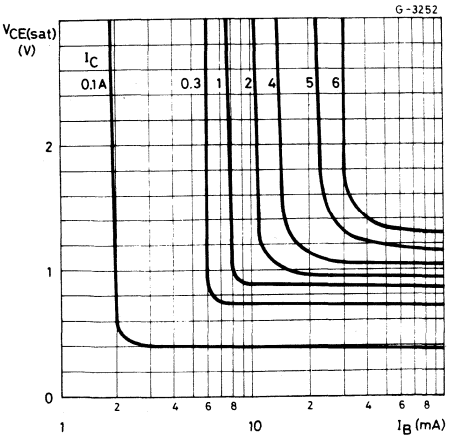

## DC current gain



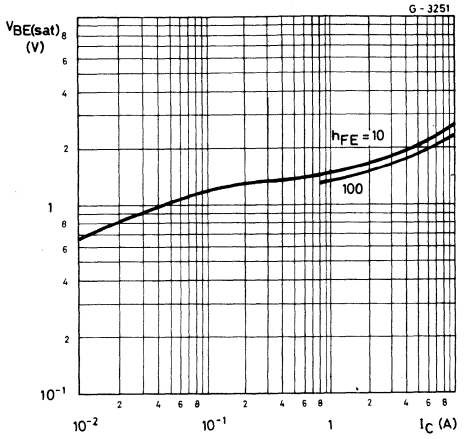

## Collector-emitter saturation voltage



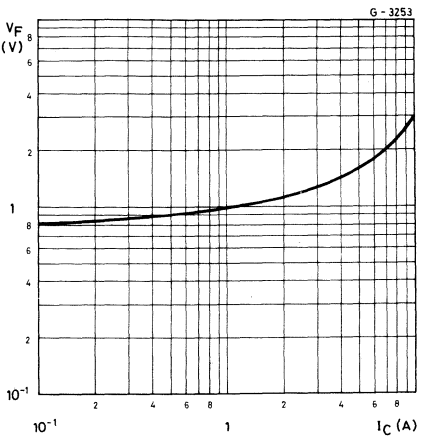

## Collector-emitter saturation voltage



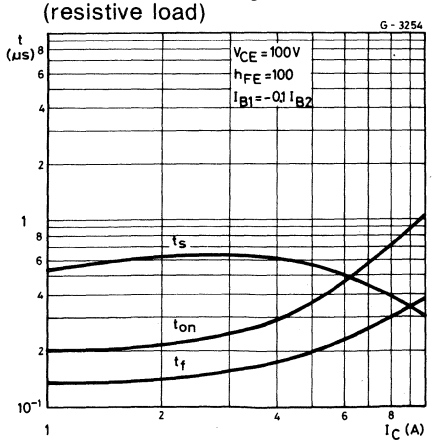
## Base-emitter saturation voltage



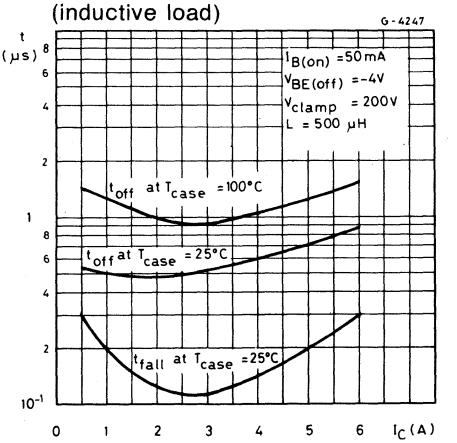

## Damper diode




## Saturated switching characteristics (resistive load)

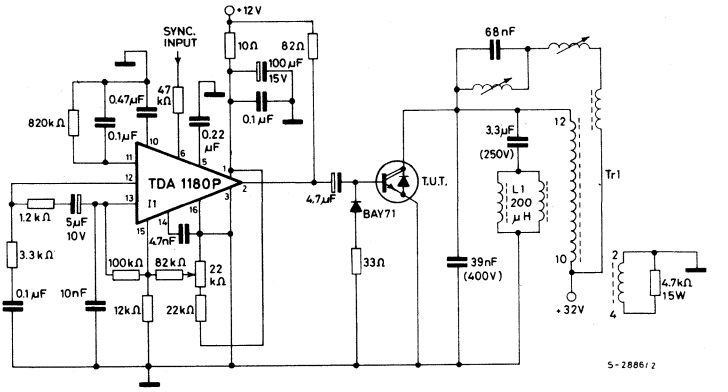



## Saturated switching characteristics (inductive load)



## HORIZONTAL DEFLECTION TURN-OFF TIME

Test circuit

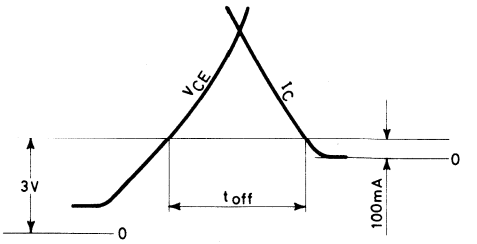



L1 = Horizontal yoke = 200 µH

Tr1 = EHT Transformer SAREAtype 900914 or equivalent

I1 = Horizontal oscillator linear I.C. TDA 1180P

Turn-off time waveform

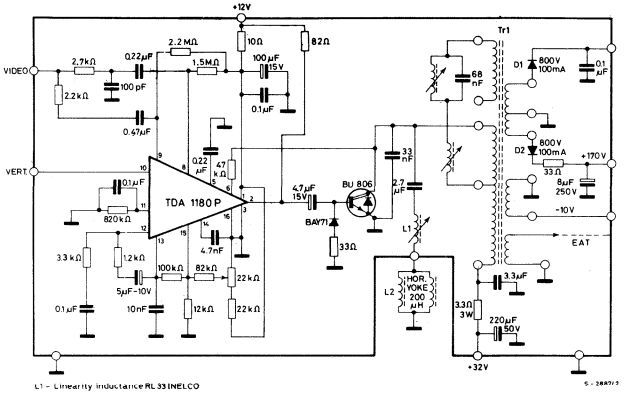



Turn-off time is the time for the collector current $I_C$ to decrease to 100 mA after the collector to emitter voltage $V_{CE}$ has risen 3V into its flyback excursion

S-0857

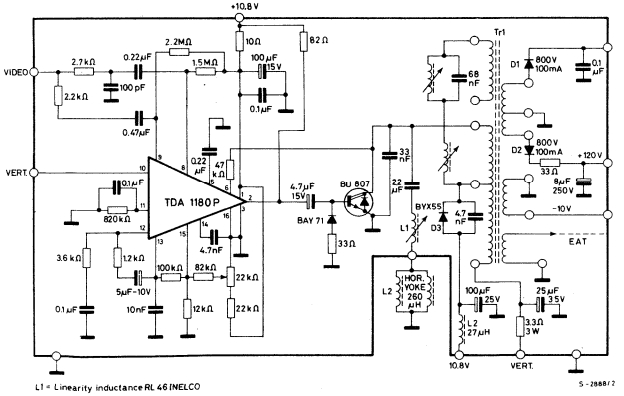
## APPLICATION INFORMATION

Horizontal deflection circuit using the darlington BU 806 directly driven by the TDA 1180 (B & W TV set: large screen solution)




$L_1$ = Linearity inductance 19÷39µH

Horizontal deflection circuit using the darlington BU 807 directly driven by the TDA 1180 (B & W TV set: small screen solution).




$L_1$ = Linearity inductance 37÷67µH

# MULTIEPITAXIAL MESA NPN

**BUX84**

PRELIMINARY DATA

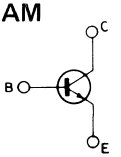
## HIGH VOLTAGE SWITCH

The BUX84, is a multiepitaxial mesa NPN transistor, intended for use in converters inverters, switching regulators, motor control systems and switching power supply in TV sets.
It is mounted in Jedec TO-220 plastic package.

## ABSOLUTE MAXIMUM RATINGS

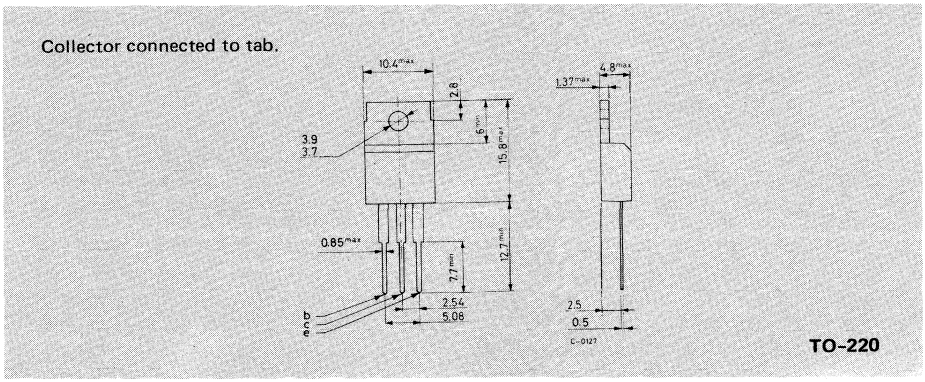
| | | | |
|---|---|---|---|
| $V_{CES}$ | Collector-emitter voltage ($V_{BE}$ = 0) | 800 | V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B$ = 0) | 400 | V |
| $I_C$ | Collector current | 2 | A |
| $I_{CM}$ | Collector peak current | 3 | A |
| $I_B$ | Base current | 0.75 | A |
| $I_{BM}$ | Base peak current | 1 | A |
| $P_{tot}$ | Total power dissipation at $T_{case} \leqslant 25°C$ | 50 | W |
| $T_{stg}$ | Storage temperature | -65 to 150 | °C |
| $T_j$ | Junction temperature | 150 | °C |

## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction--case | max. | 2.5 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless ohterwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CES}$ | Collector cutoff current ($V_{BE}$ = 0) | $V_{CE} = V_{CES}$<br>$V_{CE} = V_{CES}$ $T_j$ = 125°C | | | 200<br>1.5 | μA<br>mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C$ = 0) | $V_{EB}$ = 5V | | | 1 | mA |
| $V_{CEO\ (sus)}$* | Collector-emitter sustaining voltage | $I_C$ = 100mA $I_B$ = 0<br>L = 25mH | 400 | | | V |
| $V_{CE\ (sat)}$* | Collector-emitter saturation voltage | $I_C$ = 0.3A $I_B$ = 30mA<br>$I_C$ = 1A $I_B$ = 0.2A | | | 1.5<br>3 | V<br>V |
| $V_{BE\ (sat)}$* | Base-emitter saturation voltage | $I_C$ = 1A $I_B$ = 0.2A | | | 1.1 | V |
| $h_{FE}$* | DC current gain | $V_{CE}$ = 5V $I_C$ = 0.1A | 50 | | | — |
| $t_{on}$ | Turn-on time | $I_C$ = 1A $V_{CC}$ = 250V<br>$I_{B1}$ = 0.2A $-I_{B2}$ = 0.4A | | 300 | 500 | ns |
| $t_s$ | Storage time | | | 1 | 3.5 | μs |
| $t_f$ | Fall time | | | 0.3 | 1.4 | μs |

* Pulsed. pulse duration = 300 μs, duty cycle = 1%.

# LINEAR INTEGRATED CIRCUITS

## ADJUSTABLE VOLTAGE AND CURRENT REGULATOR

- ADJUSTABLE OUTPUT CURRENT UP TO 2A (GUARANTEED UP TO $T_j$= 150°C)
- ADJUSTABLE OUTPUT VOLTAGE DOWN TO 2.85V
- INPUT OVERVOLTAGE PROTECTION (UP TO 60V, 10 ms)
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSISTOR S.O.A. PROTECTION
- THERMAL OVERLOAD PROTECTION
- LOW BIAS CURRENT ON REGULATION PIN
- LOW STANDBY CURRENT DRAIN

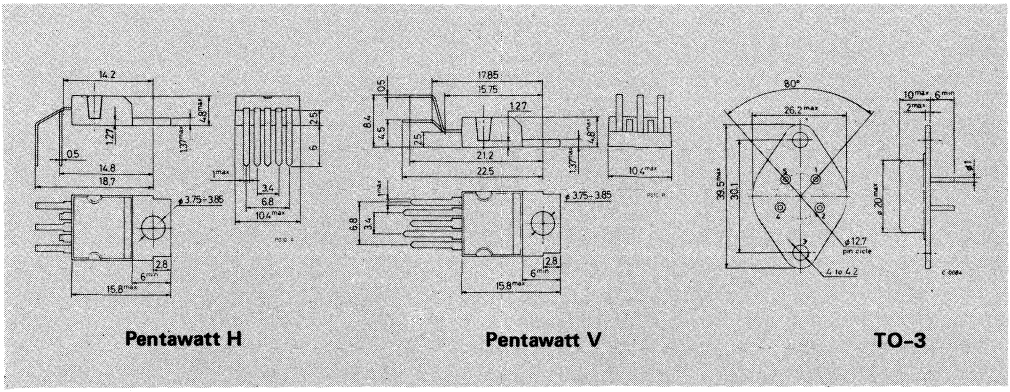
The L200 is a monolithic integrated circuit for voltage and current programmable regulation. It is available in PENTAWATT package or 4-lead TO-3 metal case. Current limiting, power limiting, thermal shutdown and input overvoltage protection (up to 60V) make the L200 virtually blowout proof. The L200 can be used to replace fixed voltage regulators when high output voltage precision is required and eliminates the need to stock a range of fixed voltage regulators.

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_i$ | DC input voltage | 40 | V |
| $V_i$ | Peak input voltage (10 ms) | 60 | V |
| $\Delta V_{i-o}$ | Dropout voltage | 32 | V |
| $I_o$ | Output current | internally limited | |
| $P_{tot}$ | Power dissipation | internally limited | |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |
| $T_{op}$ | Operating junction temperature for L200C | -25 to 150 | °C |
| | for L200 | -55 to 150 | °C |

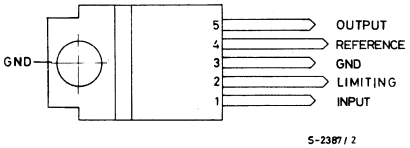
## MECHANICAL DATA

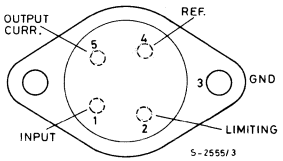
Dimensions in mm



Pentawatt H | Pentawatt V | TO-3

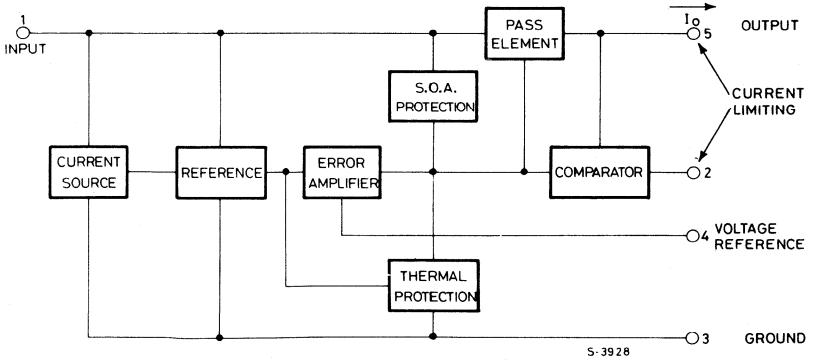
## CONNECTION DIAGRAMS AND ORDERING NUMBERS
(top views)



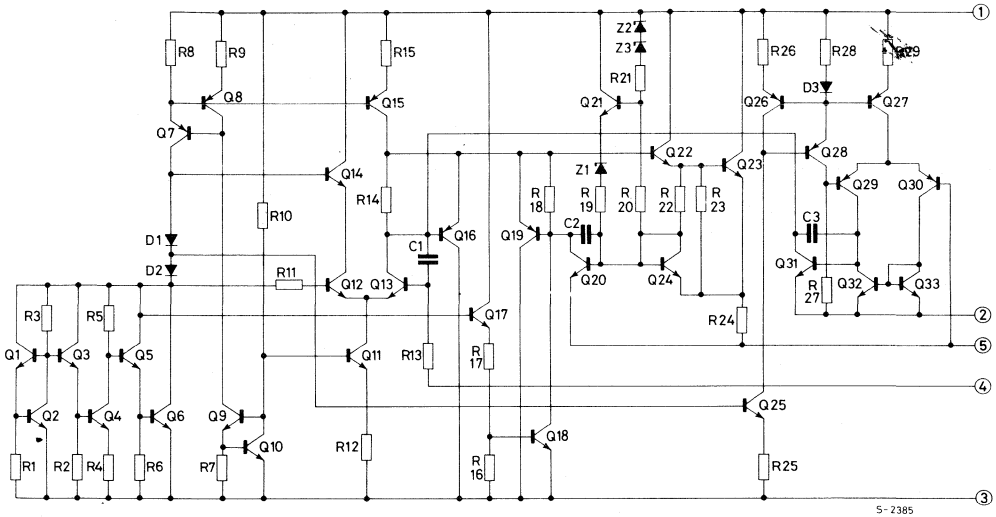




| Type | Pentawatt® | TO-3 |
|---|---|---|
| L 200 | | L 200 T |
| L 200 C | L 200 CH<br>L 200 CV | L 200 CT |

## BLOCK DIAGRAM



## SCHEMATIC DIAGRAM




## THERMAL DATA

| | | | TO-3 | Pentawatt® |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 4 °C/W | 3 °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 35 °C/W | 50 °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **VOLTAGE REGULATION LOOP** | | | | | | |
| $I_d$ | Quiescent drain current (pin 3) | $V_i$ = 20V | | 4.2 | 9.2 | mA |
| $e_N$ | Output noise voltage | $V_o = V_{ref}$ $I_o$ = 10 mA<br>B = 1 MHz | | 80 | | μV |
| $V_o$ | Output voltage range | $I_o$ = 10 mA | 2.85 | | 36 | V |
| $\frac{\Delta V_o}{V_o}$ | Voltage load regulation (note 1) | $\Delta I_o$ = 2A<br>$\Delta I_o$ = 1.5A | | 0.15<br>0.1 | 1<br>0.9 | %<br>% |
| $\frac{\Delta V_i}{\Delta V_o}$ | Line regulation | $V_o$ = 5V<br>$V_i$ = 8 to 18V | 48 | 60 | | dB |
| SVR | Supply voltage rejection | $V_o$ = 5V $I_o$ = 500 mA<br>$\Delta V_i$ = 10 $V_{pp}$<br>f = 100 Hz (note 2) | 48 | 60 | | dB |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $\Delta V_{i-o}$ | Droupout voltage between pins 1 and 5 | $I_o$ = 1.5A $\Delta V_o \leqslant 2\%$ | | 2 | 2.5 | V |
| $V_{ref}$ | Reference voltage (pin 4) | $V_i$ = 20V $I_o$ = 10 mA | 2.64 | 2.77 | 2.86 | V |
| $\Delta V_{ref}$ | Average temperature coefficient of reference voltage | $V_i$ = 20V $I_o$ = 10 mA<br>for $T_j$ = -25 to 125°C<br>for $T_j$ = 125 to 150°C | | <br>-0.25<br>-1.5 | | <br>mV/°C<br>mV/°C |
| $I_4$ | Bias current at pin 4 | | | 3 | 10 | μA |
| $\frac{\Delta I_4}{\Delta T \cdot I_4}$ | Average temperature coefficient (pin 4) | | | -0.5 | | %/°C |
| $Z_o$ | Output impedance | $V_i$ = 10V $V_o = V_{ref}$<br>$I_o$ = 0.5A f = 100 Hz | | 1.5 | | mΩ |

## CURRENT REGULATION LOOP

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{SC}$ | Current limit sense voltage between pins 5 and 2 | $V_i$ = 10V $V_o = V_{ref}$<br>$I_5$ = 100 mA | 0.38 | 0.45 | 0.52 | V |
| $\frac{\Delta V_{sc}}{\Delta T \cdot V_{sc}}$ | Average temperature coefficient of $V_{SC}$ | | | 0.03 | | %/°C |
| $\frac{\Delta I_o}{I_o}$ | Current load regulation | $V_i$ = 10V $\Delta V_o$ = 3V<br>$I_o$ = 0.5A<br>$I_o$ = 1A<br>$I_o$ = 1.5A | | <br>1.4<br>1<br>0.9 | | <br>%<br>%<br>% |
| $I_{sc}$ | Peak short circuit current | $V_i - V_o$ = 14V<br>(pins 2 and 5 short circuited) | | | 3.6 | A |

Note 1): A load step of 2A can be applied provided that input-output differential voltage is lower than 20V (see fig. 1).

Note 2): The same performance can be maintained at higher output levels if a bypassing capacitor is provided between pins 2 and 4.

Fig. 1 - Typical safe operating area protection

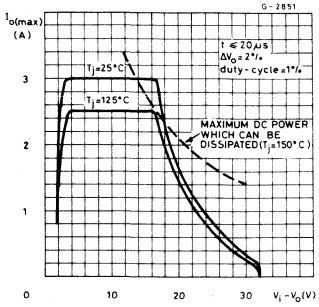



Fig. 2 - Quiescent current vs. supply voltage

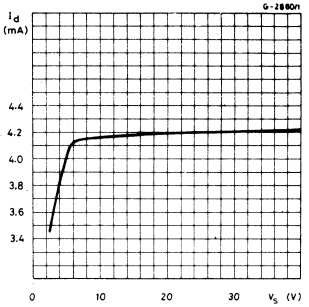



Fig. 3 - Quiescent current vs. junction temperature

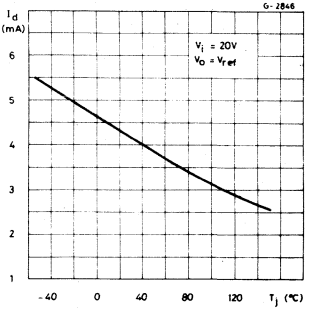



Fig. 4 - Quiescent current vs. output current

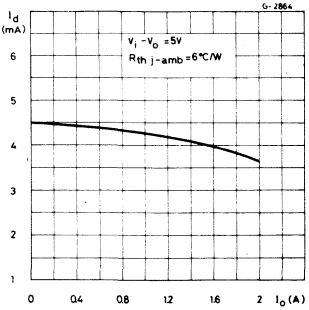



Fig. 5 - Output noise voltage vs. output voltage

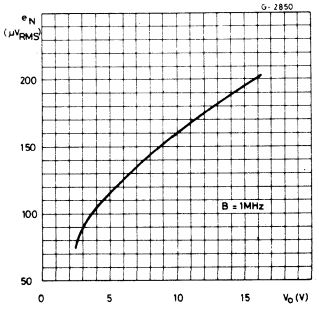



Fig. 6 - Output noise voltage vs. frequency

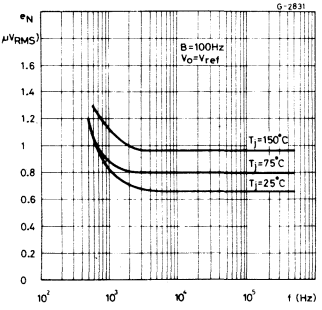



Fig. 7 - Reference voltage vs. junction temperature

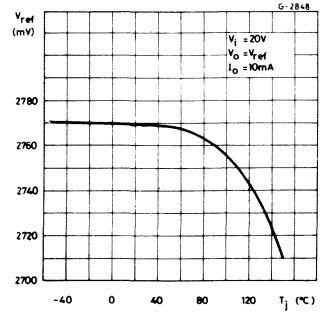



Fig. 8 - Voltage load regulation vs. junction temperature

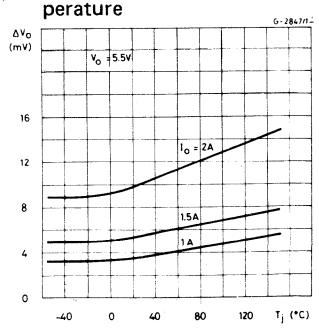



Fig. 9 - Supply voltage rejection vs. frequency

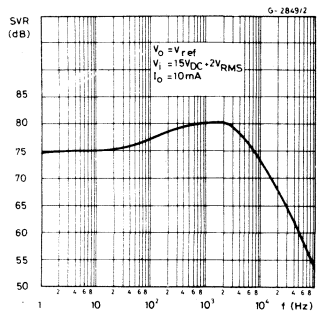


Fig. 10 - Dropout voltage vs. junction temperature

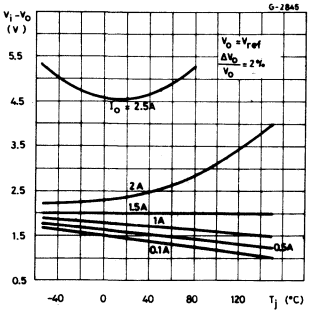



Fig. 11 - Output impedance vs. frequency

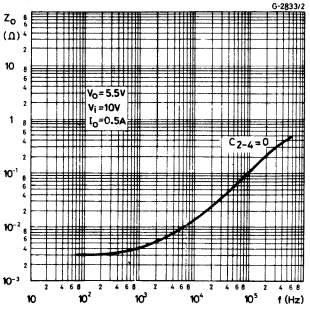



Fig. 12 - Output impedance vs. output current

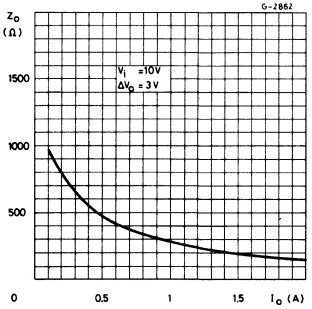



Fig. 13 - Voltage transient response

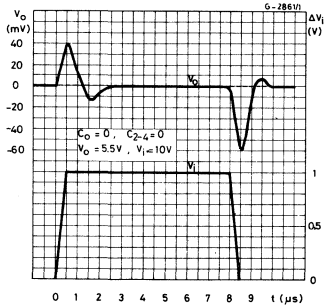



Fig. 14 - Load transient response

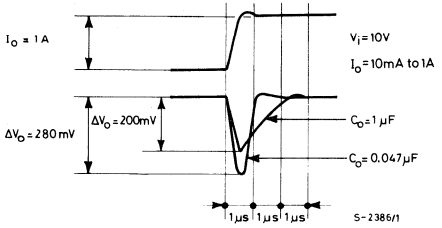



Fig. 15 - Load transient response

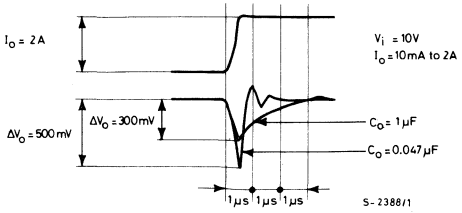
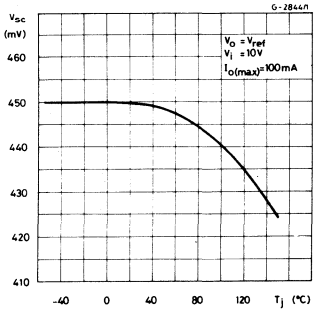



Fig. 16 - Current limit sense voltage vs. junction temperature



## APPLICATION CIRCUITS

Fig. 17 - Programmable voltage regulator

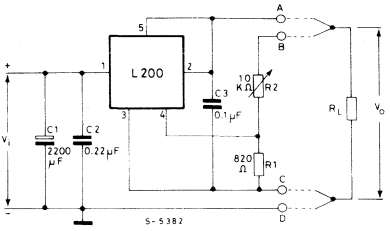



Fig. 18 - P.C. board and components layout of fig. 17. (1 : 1 scale)

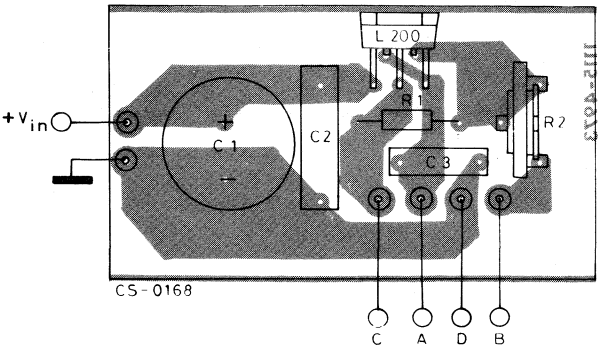



Fig. 19 - Programmable voltage regulator with current limiting

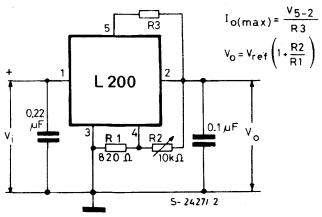



Fig. 20 - Programmable current regulator

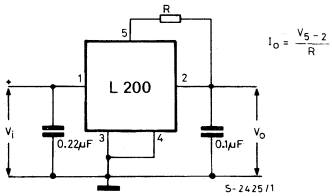



Fig. 21 - High current voltage regulator with short circuit protection

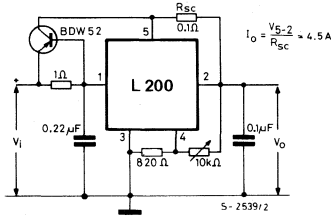
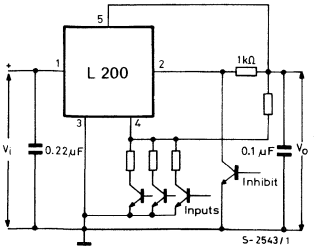
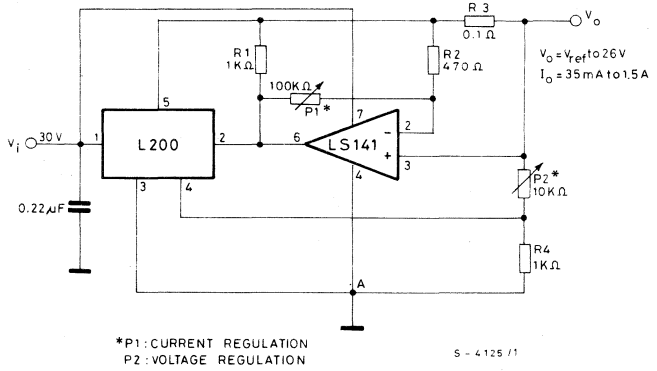



Fig. 22 - Digitally selected regulator with inhibit



## APPLICATION CIRCUITS

Fig. 23 - Programmable voltage and current regulator




Note: Connecting point A to a negative voltage (for example-3V/10 mA) it is possible to extend the output voltage range down to 0V and to obtain the current limiting down to this level (output short-circuit condition).

Fig. 24 - High current regulator with NPN pass transistor

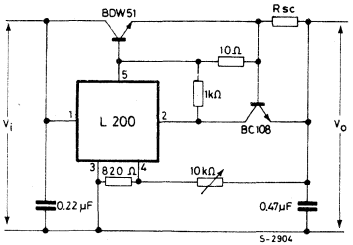
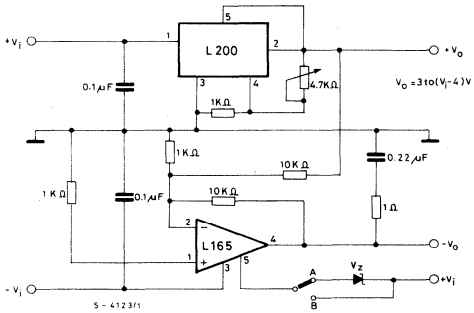



Fig. 25 - High current tracking regulator




A: for $\pm 18 \leqslant V_i \leqslant \pm 32$

Note – $V_z$ must be chosen in order to verify $2\,V_i - V_z \leqslant 36V$

B: for $V_i \leqslant \pm 18V$

## APPLICATION CIRCUITS (continued)

Fig. 26 - High input and output voltage

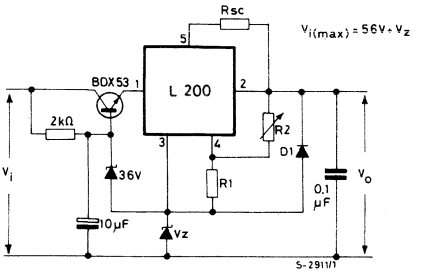
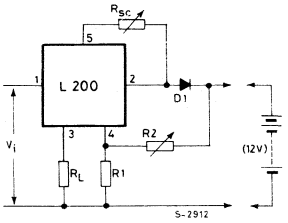
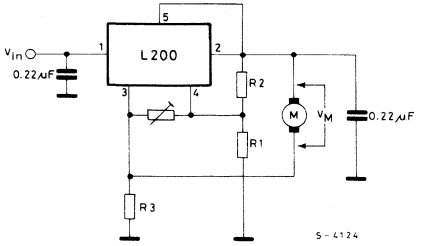



Fig. 27 - Constant current battery charger




The resistors $R_1$ and $R_2$ determine the final charging voltage and $R_{sc}$ the initial charging current. $D_1$ prevents discharge of the battery throught the regulator.
The resistor $R_L$ limits the reverse currents through the regulator (which should be 100 mA max) when the battery is accidentally reverse connected. If $R_L$ is in series with a bulb of 12V/50 mA rating this will indicate incorrect connection.

Fig. 28 - 30W Motor speed control




$$R_3 = \frac{R_1}{R_2} \cdot R_M$$

$$V_M = V_{ref} \cdot (1 + \frac{R_2}{R_1})$$

Fig. 29 - Low turn on

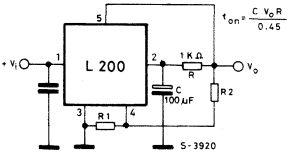
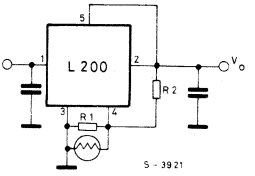



Fig. 30 - Light controller



# LINEAR INTEGRATED CIRCUITS

ADVANCE DATA

## DUAL POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE RANGE
- LARGE DIFFERENTIAL MODE RANGE
- STABLE WITH UNITY GAIN
- GROUND COMPATIBLE INPUTS
- LOW SATURATION (1V/0.5A)
- THERMAL SHUTDOWN

The L272 is a monolithic integrated circuit in powerdip package, intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies.
The high gain and high output power capability provide superior performance whetever an operational amplifier/power booster combination is required.

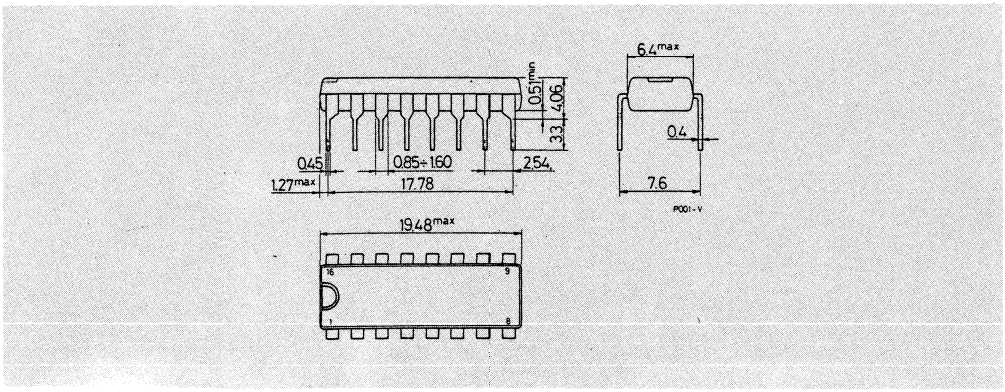
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 28 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential input voltage | $\pm V_s$ | |
| $I_o$ | DC output current | 1 | A |
| $I_p$ | Peak output current (non repetitive) | 1.5 | A |
| $P_{tot}$ | Power dissipation at $T_{amb} = 80°C$ | 1 | W |
| | $T_{case} = 75°C$ | 5 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

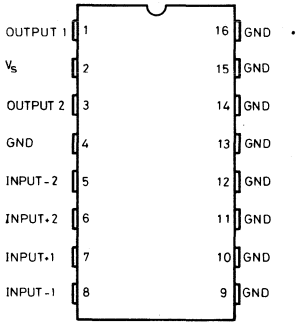
**ORDERING NUMBER:** L272B

## MECHANICAL DATA

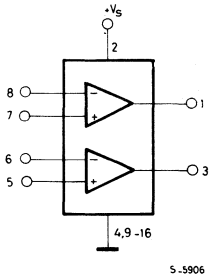
Dimensions in mm



## CONNECTION AND BLOCK DIAGRAM
(top view)

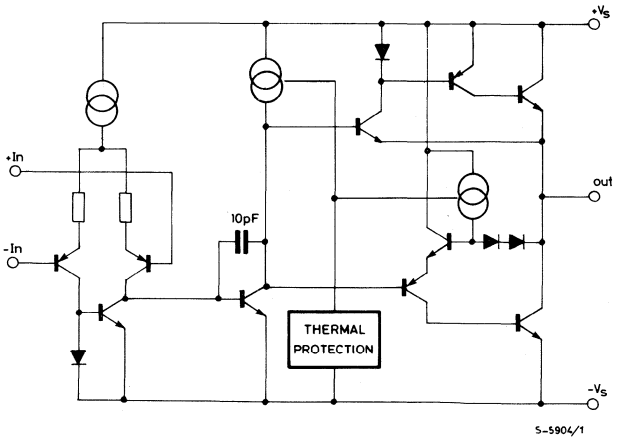



S-5905




S-5906

## SCHEMATIC DIAGRAM




S-5904/1

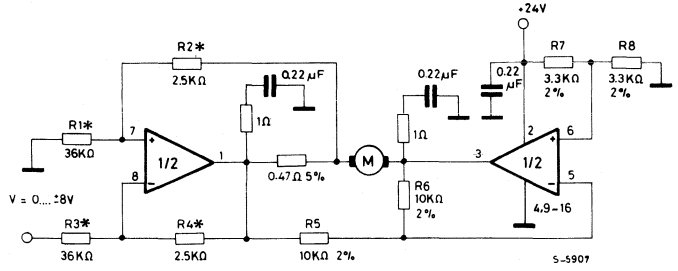
## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-pins | max | 15 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-amb | max | 70 | °C/W |

## ELECTRICAL CHARACTERISTICS ($V_s$ = 24V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | 4 | | 28 | V |
| $I_d$ | Quiescent drain current | | | | 5.5 | 12 | mA |
| $I_b$ | Input bias current | | | | 0.5 | 2.5 | μA |
| $V_{os}$ | Input offset voltage | | | | 15 | | mV |
| $I_{os}$ | Input offset current | | | | 50 | 250 | nA |
| SR | Slew-Rate | $G_v$ = 1 | | | 1 | | V/μs |
| B | Gain-bandwidth product | | | | 350 | | KHz |
| $V_o$ | Output voltage swing | f = 1 kHz | $I_p$ = 0.1A<br>$I_p$ = 0.5A | | 23<br>22.5 | | Vpp |
| $R_i$ | Input resistance | | | 500 | | | KΩ |
| $G_v$ | Voltage gain (open loop) | | | | 70 | | dB |
| $e_N$ | Input noise voltage | B = 10 to 10 000 Hz | | | 5 | | μV |
| $i_N$ | Input noise current | | | | 200 | | pA |
| CMR | Common mode rejection | | | | 70 | | dB |
| SVR | Supply voltage rejection | $f_{ripple}$ = 100 Hz | Single Supply | | 70 | | dB |
| | | | Split Supply | | 62 | | dB |
| $T_{sd}$ | Thermal shutdown junction temperature | | | | 160 | | °C |

Fig. 1 - Motor current control circuit

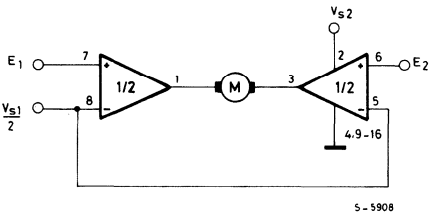



$I_M = 0.14 \cdot V_i$

* < 1%

Note: The input voltage level is compatible with L291 (5-bit D/A converter).

Fig. 2 - Bidirectional DC motor control with µP compatible inputs




$V_{S1}$ = logic supply voltage  Must be $V_{S2} > V_{S1}$  E1, E2 = logic inputs

Fig. 3 - Bidirectional speed control of DC motors

For circuit stability ensure that $R_x > \frac{2\ R3 \cdot R1}{R_M}$ where $R_M$ = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\ (V_i - \frac{V_s}{2}) + |R_o| \cdot I_M$ where $|R_o| = \frac{2\ R3 \cdot R1}{R_x}$ and $I_M$ is the motor current;

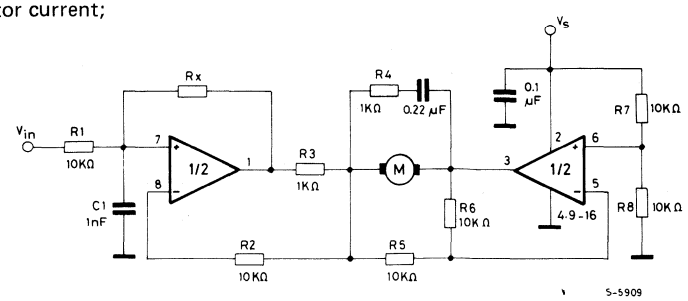
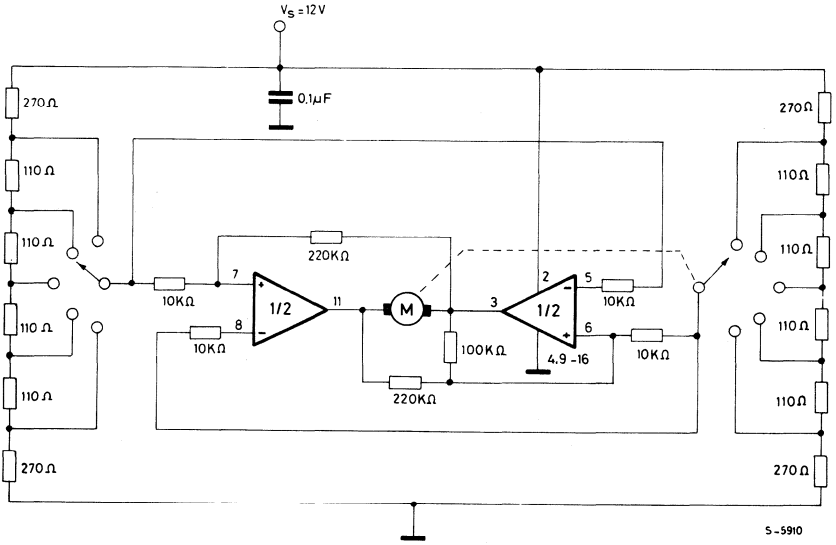


Fig. 4 - Position control for car headlights.



# LINEAR INTEGRATED CIRCUITS

**L272M**

**ADVANCE DATA**

## DUAL POWER OPERATIONAL AMPLIFIER

- OUTPUT CURRENT TO 1A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE RANGE
- LARGE DIFFERENTIAL MODE RANGE
- STABLE WITH UNITY GAIN
- GROUND COMPATIBLE INPUTS
- LOW SATURATION (1V/0.5A)
- THERMAL SHUTDOWN

The L272M is a monolithic integrated circuit in 8 lead minidip package, intended for use as power operational amplifier in a wide range of applications including servo amplifiers and power supplies. The high gain and high output power capability provide superior performance whetever an operational amplifier/power booster combination is required.

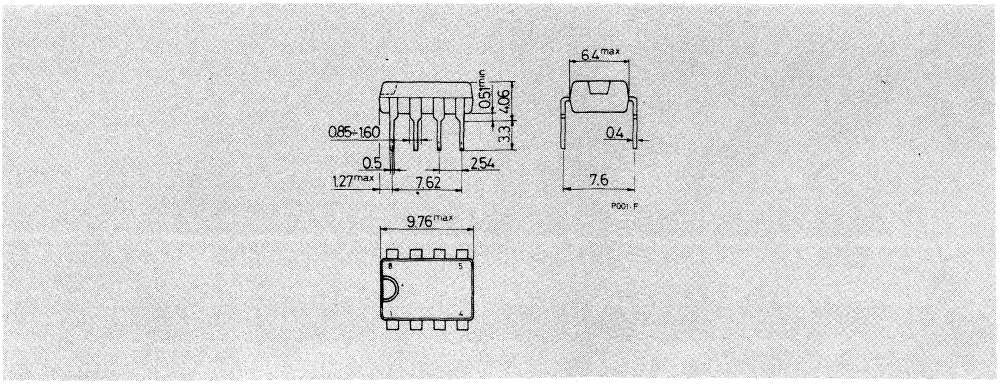
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 28 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential Input Voltage | $\pm V_s$ | |
| $I_o$ | DC Output Current | 1 | A |
| $I_P$ | Peak Output Current (non repetitive) | 1.5 | A |
| $P_{tot}$ | Power Dissipation at $T_{amb} = 50°C$ | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

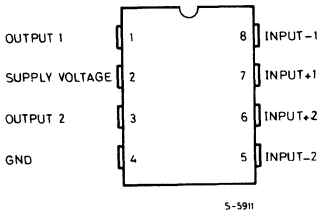
**ORDERING NUMBER:** L272 MB

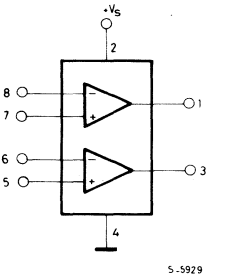
## MECHANICAL DATA

Dimensions in mm

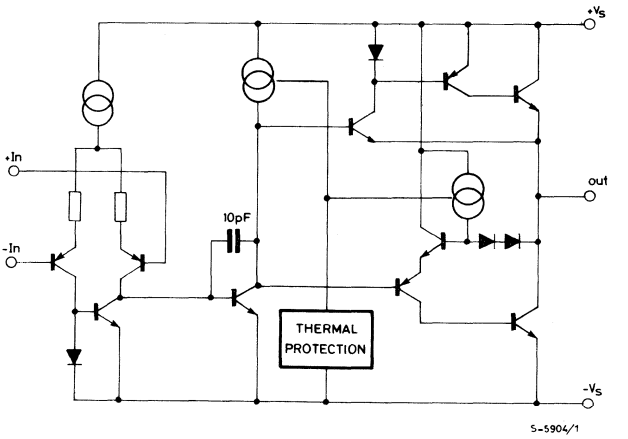


## CONNECTION AND BLOCK DIAGRAM
(top view)




## SCHEMATIC DIAGRAM



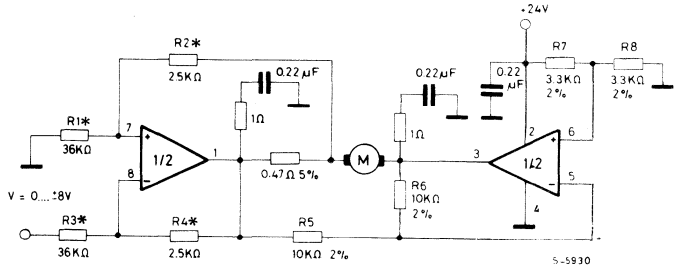

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-pin 4 | max | 70 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-amb | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS ($V_s$ = 24V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | 4 | | 28 | V |
| $I_d$ | Quiescent drain current | | | | 5.5 | 12 | mA |
| $I_b$ | Input bias current | | | | 0.5 | 2.5 | μA |
| $V_{os}$ | Input offset voltage | | | | 15 | | mV |
| $I_{os}$ | Input offset current | | | | 50 | 250 | nA |
| SR | Slew-Rate | $G_v$ = 1 | | | 1 | | V/μs |
| B | Gain-bandwidth product | | | | 350 | | KHz |
| $V_o$ | Output voltage swing | f = 1 kHz | $I_p$ = 0.1A<br>$I_p$ = 0.5A | | 23<br>22.5 | | Vpp |
| $R_i$ | Input resistance | | | 500 | | | KΩ |
| $G_v$ | Voltage gain (open loop) | | | | 70 | | dB |
| $e_N$ | Input noise voltage | B = 10 to 10 000 Hz | | | 5 | | μV |
| $i_N$ | Input noise current | | | | 200 | | pA |
| CMR | Common mode rejection | | | | 70 | | dB |
| SVR | Supply voltage rejection | $f_{ripple}$= 100 Hz | Single Supply | | 70 | | dB |
| | | | Split Supply | | 62 | | dB |
| $T_{sd}$ | Thermal shutdown junction temperature | | | | 160 | | °C |

Fig. 1 - Motor current control circuit

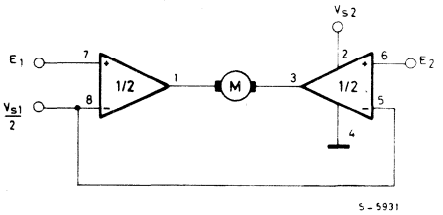



* < 1%

$I_M = 0.14 \cdot V_i$

Note: The input voltage level is compatible with L291 (5 - BIT D/A converter).

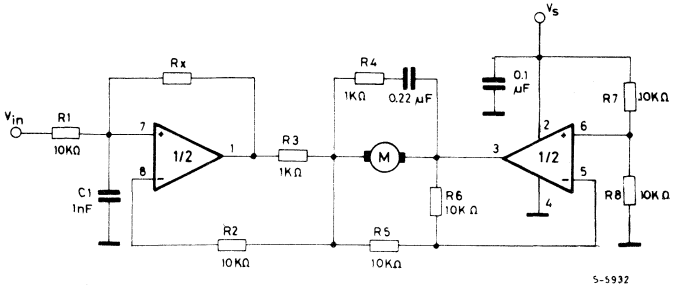
Fig. 2 - Bidirectional DC motor control with µP compatible inputs




$V_{S1}$ = logic supply voltage  Must be $V_{S2} > V_{S1}$  E1, E2 = logic inputs

Fig. 3 - Bidirectional speed control of DC motors

For circuit stability ensure that $R_x > \frac{2\,R3 \cdot R1}{R_M}$ where $R_M$ = internal resistance of motor. The voltage available at the terminals of the motor is $V_M = 2\,(V_i - \frac{V_s}{2}) + |R_o| \cdot I_M$ where $|R_o| = \frac{2\,R3 \cdot R1}{R_x}$ and $I_M$ is the motor current.



# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## HIGH CURRENT SWITCHING REGULATOR

- 5.1V TO 40V OUTPUT
- 4A OUTPUT CURRENT
- DELIVERS MORE THAN 2A AT 5V WITHOUT HEATSINK
- PROGRAMMABLE CURRENT LIMITER
- SOFT START
- RESET OUTPUT
- PRECISE (± 2%) ON-CHIP REFERENCE
- VERY FEW COMPONENTS
- SWITCHING FREQUENCY TO 200 kHz
- VERY HIGH EFFICIENCY (UP TO 90%)
- THERMAL SHUTDOWN
- REMOTE INHIBIT AND SYNC INPUT
- CONTROL CIRCUIT FOR CROWBAR SCR

The L296 is a monolithic power switching regulator delivering 4A at a voltage variable from 5.1V to 40V in step down configurations. Features of the device include programmable current limiting, soft start, remote inhibit, thermal protection, a reset output for microprocessors and a synchronisation input for multichip configurations. The L296 is mounted in a 15-lead MULTIWATT plastic power package and requires very few external components. Efficient operation at switching frequencies up to 200 kHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

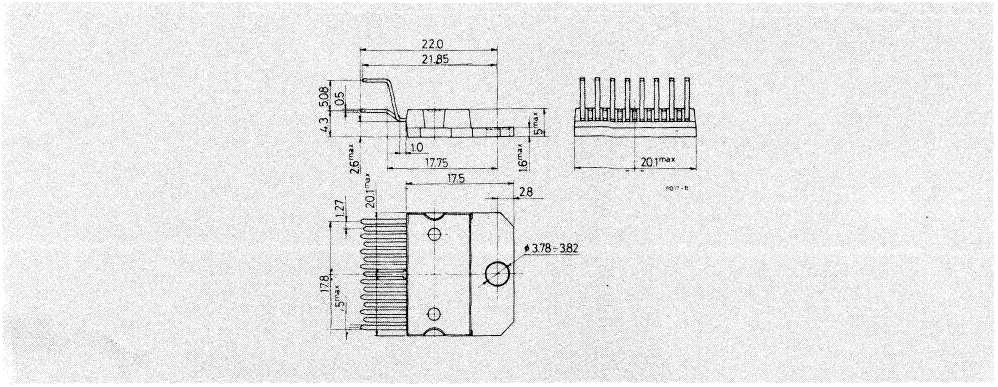
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_i$ | Input voltage | 50 | V |
| $V_{i/o}$ | Input/Output voltage | 50 | V |
| $I_o$ | Output current | internally limited | |
| $I_R$ | Reset output current | 50 | mA |
| $V_R$ | Reset output voltage | 50 | V |
| $V_{inh}$ | Inhibit voltage | 15 | V |
| $P_{tot}$ | Power dissipation at $T_{case} < 90°C$ | 20 | W |
| $T_j$ | Junction temperature range | -25 to +150 | °C |
| $T_{stg}$ | Storage temperature range | -65 to +150 | °C |

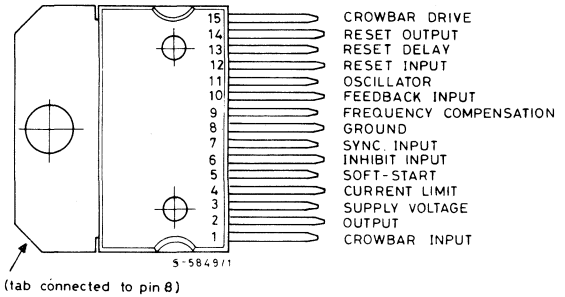
**ORDERING NUMBER:** L296

## MECHANICAL DATA

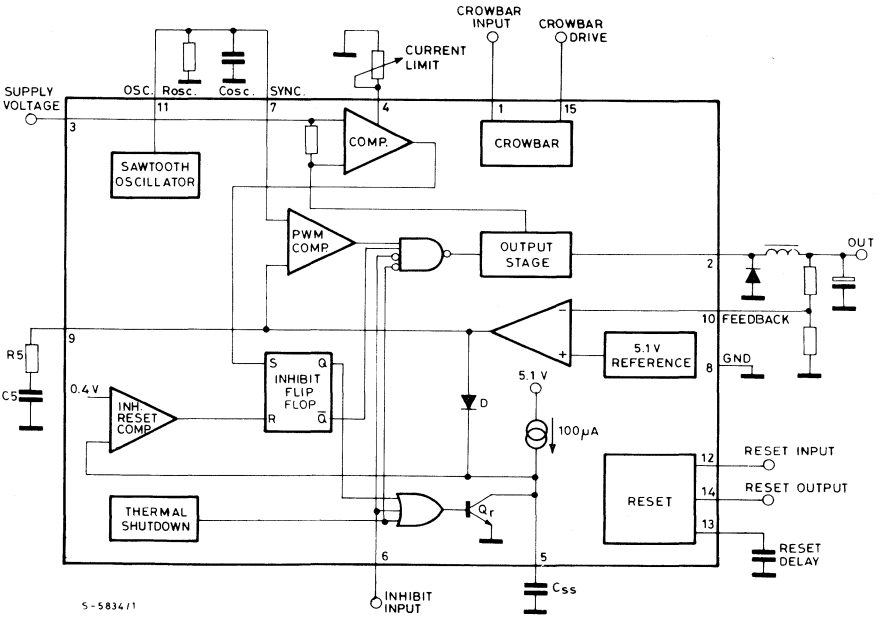
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## BLOCK DIAGRAM




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 35 | °C/W |

## PIN FUNCTIONS

| N° | NAME | FUNCTION |
|---|---|---|
| 1 | CROWBAR INPUT | Voltage sense input for crowbar overvoltage protection. Normally connected to the feedback input thus triggering the SCR when $V_{out}$ exceeds nominal by 20%. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used. |
| 2 | OUTPUT | Regulator output. |
| 3 | SUPPLY VOLTAGE | Unregulated voltage input. An internal regulator powers the L296's internal logic. |
| 4 | CURRENT LIMIT | A resistor connected between this terminal and ground sets the current limiter threshold (1.5 to 5A). If this terminal is left unconnected the threshold will be 5A. |
| 5 | SOFT START | Soft start time constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current. |
| 6 | INHIBIT INPUT | TTL – level remote inhibit. A logic high level on this input disables the L296. |
| 7 | SYNC INPUT | Multiple L296s are synchronised by connecting the sync inputs together and omitting the oscillator RC network on all but one device. |
| 8 | GROUND | Common ground terminal. |
| 9 | FREQUENCY COMPENSATION | A series RC network connected between this terminal and ground determines the regulation loop gain characteristics. |
| 10 | FEEDBACK INPUT | The feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages. |
| 11 | OSCILLATOR | A parallel RC network connected to this terminal determines the switching frequency. This pin must be connected to the sync input when the internal oscillator is used. |

## PIN FUNCTIONS (continued)

| N° | NAME | FUNCTION |
|---|---|---|
| 12 | RESET INPUT | Input of the reset circuit. The threshold is roughly 5V. It may be connected to the feedback point or via a divider to the input. |
| 13 | RESET DELAY | A capacitor connected between this terminal and ground determines the reset signal delay time. |
| 14 | RESET OUTPUT | Open collector reset signal output. This output is high when the supply is safe. |
| 15 | CROWBAR OUTPUT | SCR gate drive output of the crowbar circuit. |

## CIRCUIT OPERATION

The L296 is a monolithic stepdown switching regulator providing output voltages from 5.1V to 40V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2%). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage.
The precision and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor $C_s$ and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The crowbar circuit senses the output voltage and the crowbar output can provide a current of 100 mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20%. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

## CIRCUIT OPERATION (continued)

A TTL – level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches 150°C and has a hysteresis of 20°C.

Fig. 1 - Reset output waveforms

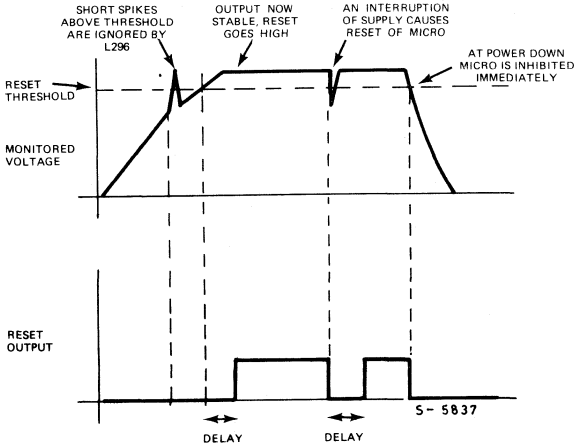



Fig. 2 - Soft start waveforms

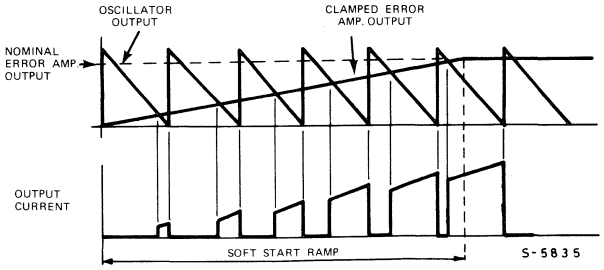
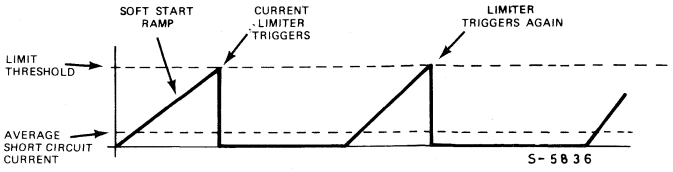



Fig. 3 - Current limiter waveforms



**ELECTRICAL CHARACTERISTICS** (Refer to the test circuit, $T_{amb}$= 25°C unless otherwise specified)

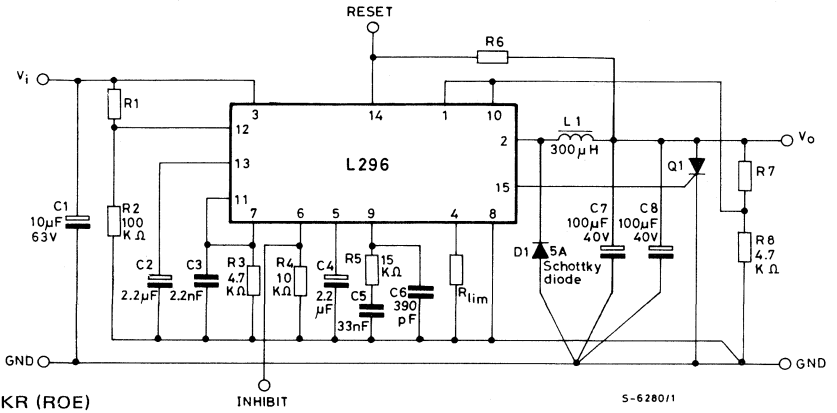
| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_o$ | Output voltage range | | 5.1 | | 40 | V |
| $V_i$ | Supply voltage range | | 8 | | 50 | V |
| $I_{o\ max}$ | Output current | Pin 4 open | 4 | | | A |
| $I_{OL}$ | Current limit | Pin 4 open | | 5 | | A |
| | | $R_{lim}$= 33 KΩ | | 2.5 | | A |
| $V_{sat}$ | Output transistor saturation voltage | $I_o$ = 4A<br>$I_o$ = 2A | | 2<br>1.3 | | V<br>V |
| $f_s$ | Switching frequency | $R_{osc}$= 4.7 KΩ $C_{osc}$= 2.2 nF | | 100 | | kHz |
| | Efficiency | f = 100 KHz<br>$V_i$ = 35V $V_o$ = 5.1V<br>$I_o$ = 3A $V_o$ = 12V | | <br>75<br>85 | | <br>%<br>% |
| $\Delta V_o$ | Line regulation | $V_i$ = 10 to 40V<br>$V_o$ = 5.1V $I_o$ = 2A | | <br>20 | | <br>mV |
| $\Delta V_o$ | Load regulation | $V_i$ = 15V $V_o$ = 5.1V<br>$I_o$ = 2A to 4A<br>$I_o$ = 0.5A to 4A | | <br>10<br>15 | | <br>mV<br>mV |
| SVR | Supply voltage rejection | f = 100 Hz | | 60 | | dB |
| $V_{REF}$ | Internally reference voltage | $V_i$ = 8 to 50V | 5 | 5.1 | 5.2 | V |
| $V_{REF}$ | Average temperature coeff. of reference voltage | | | 0.2 | | mV/°C |
| $t_{ss}$ | Stoft start time | $C_s$ = 2.2 μF | | 20 | | ms |
| $I_{SH}$ | Output average current with short circuit output | | | 0.5 | | A |
| **RESET SECTION** | | | | | | |
| $V_{RTi}$ | Reset threshold voltage (pin 12) | $V_i$ = 8 to 50V | $V_{ref}$ -110mV | $V_{ref}$ -100mV | $V_{ref}$ -90 mV | V |
| $V_{RTo}$ | Reset out low voltage (pin 14) | $I_L$ = 16 mA | | | 0.2 | V |
| | Delay time (pin 13) | $C_{reset}$ = 2.2 μF | | 100 | | ms |
| **CROWBAR SECTION** | | | | | | |
| | Threshold voltage (pin 12) | | +12% | $V_{ref}$ +20% | +23% | |
| | I source (Pin 15) | | | 100 | | mA |
| | I sink (Pin 15) | | | 5 | | mA |
| | Delay time | | | 10 | | μs |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **INHIBIT SECTION** | | | | | | |
| $V_{INHL}$ | Low input voltage | | | | 1.2 | V |
| $V_{INHH}$ | High input voltage | | 2.2 | | | V |
| $I_{INHL}$ | Input current with low input voltage | | | | 100 | μA |
| $I_{INHH}$ | Input current with high input voltage | | | | 10 | μA |
| **ERROR AMPLIFIER SECTION** | | | | | | |
| $I_b$ | Input bias current | | | 2 | | μA |
| $G_v$ | Large signal open loop gain | | | 60 | | dB |
| $I_{OE}$ | Out sink current | | | 200 | | μA |
| | Out source current | | | 200 | | μA |

**Note:** Measurements are performed with low duty cycle pulse signals.

Fig. 4 - Test and application circuit



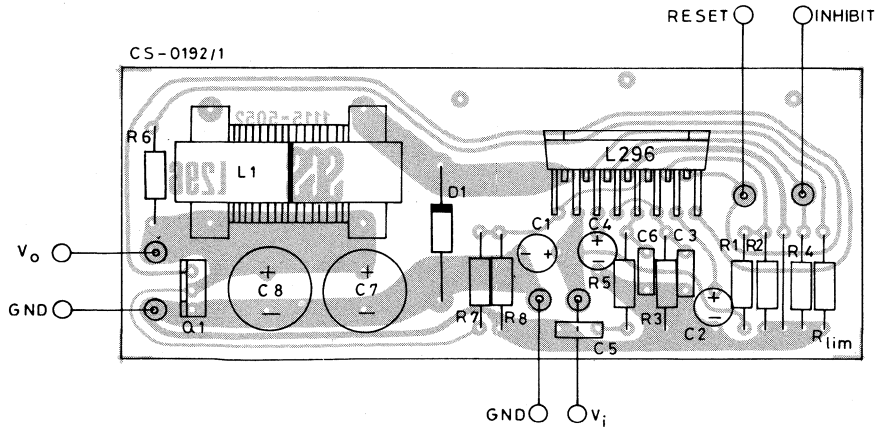

C7, C8: EKR (ROE)

## SUGGESTED INDUCTOR (L1)

| Core Type | No. Turns | Wire Gauge | Air Gap |
|---|---|---|---|
| Thomson GUP 20x16x7 | 50 | 0.8 mm. | 0.7 mm |
| Siemens EC 35/17/10 (B66337 - G0500 - X127) | 40 | 2x0.8 mm. | – |
| VOGT 250 μH Toroidal coil, part number 5730501800 | | | |

| Resistor values for standard output voltages | | |
|---|---|---|
| $V_o$ | R8 | R7 |
| 12V | 4.7 kΩ | 6.2 kΩ |
| 15V | 4.7 kΩ | 9.1 kΩ |
| 18V | 4.7 kΩ | 12 kΩ |
| 24V | 4.7 kΩ | 18 kΩ |

Fig. 5 - P.C. board and component layout of the circuit of fig. 4 (1:1 scale)



## SELECTION OF COMPONENT VALUES

| Component | Recommended Value | Purpose | Allowed range Min. | Allowed range Max. | NOTES |
|---|---|---|---|---|---|
| R1<br>R2 | –<br>100 kΩ | Set input voltage threshold for reset | – | <br>220 kΩ | $R1/R2 = \frac{V_{i\,min}}{5} - 1$<br>If output voltage is sensed R1 and R2 may be omitted and pin 12 connected to pin 10. |
| R3 | 4.7 kΩ | Sets switching frequency | 1 kΩ | 100 kΩ | |
| $R_{lim}$ | – | Sets current limit level | | | If $R_{lim}$ is omitted and pin 4 left open the current limit is 5A. |
| R5 | 15 kΩ | Frequency compensation | 10 kΩ | | |
| R7<br>R8 | –<br>4.7 kΩ | Divider to set output voltage | –<br>– | –<br>5.1 kΩ | $R7/R8 = \frac{V_o - V_{ref}}{V_{ref}}$<br>Omitted for 5V output. |
| R4 | 10 kΩ | Pull-down resistor | | 12 kΩ | May be omitted and pin 6 grounded if inhibit not used. |
| R6 | | Collector load for reset output | $\frac{V_o}{0.05}$ | | Omitted if reset function not used. |
| C1 | 10 μF | Stability. | 1 μF | | |
| C2 | 2.2 μF | Sets reset delay | 1 μF | 4.7 μF | Omitted if reset function not used. |
| C3 | 2.2 nF | Sets switching frequency | 1 nF | 3.3 nF | |
| C4 | 2.2 μF | Soft start | 1 μF | 4.7 μF | Also determines average short circuit current. |
| C5 | 33 nF | Frequency compensation | | | |
| C6 | 390 pF | High frequency compensation | | | Not required for 5V operation. |
| C7, C8<br>L1 | 100 μF<br>300 μH | Output filter | | | |
| Q1 | | Crowbar protection | | | The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device. |

**Note:** Depending on the PCB layout, component values and operating conditions, switching frequency spikes may be present on the output with an amplitude of 30 mV to 1V.
In critical applications an LC filter should be added to remove these spikes.

Fig. 6 - Efficiency vs. output current

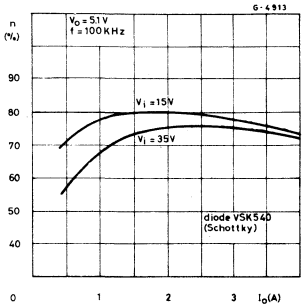



Fig. 7 - Dissipated Power vs. output current (L296 only)

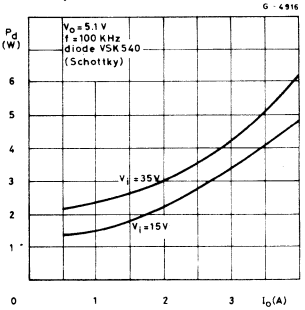



Fig. 8 - Efficiency vs. output current

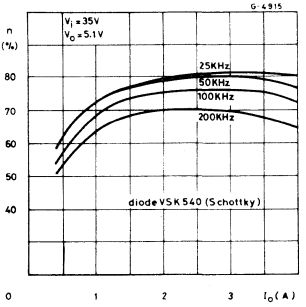



Fig. 9 - Efficiency vs. output voltage

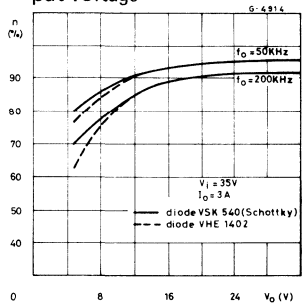



Fig. 10 - Operating frequency vs. R3 and C3

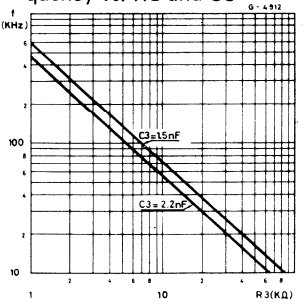



Fig. 11 - Power dissipation derating curve

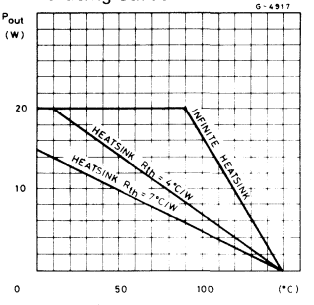



Fig. 12 - Voltage sensing for remote load

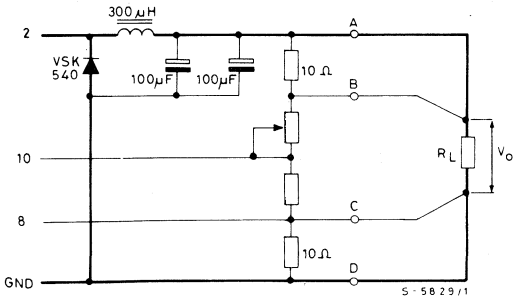
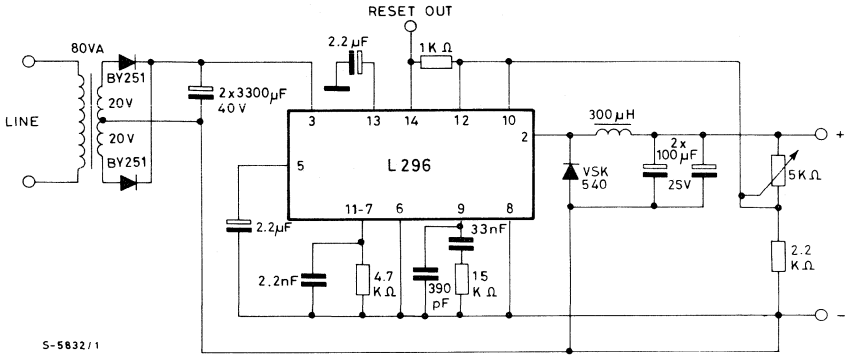
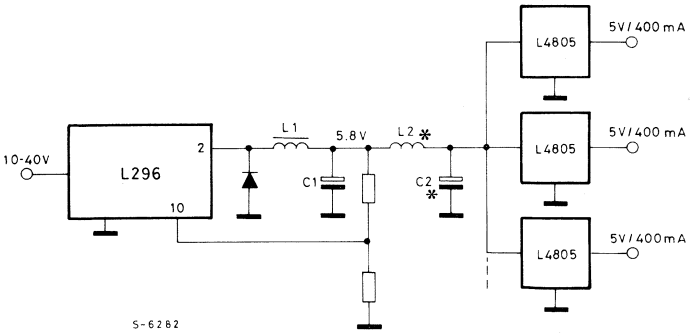


Fig. 13 - Typical application




$V_o$ = 5.1 to 15V
$I_o$ = 4A max. (min. load current = 100 mA)
ripple ⩽ 20 mV
load regulation (1A to 4A) = 10 mV ($V_o$ = 5.1V)
line regulation (220V ± 15% and to $I_o$ = 3A) = 15 mV ($V_o$ = 5.1V)

Fig. 14 - Preregulator for distributed supplies




(*) L2 and C2 are necessary to reduce the switching frequency spikes.

Fig. 15 - In multiple supplies several L296s can be synchronised as shown.

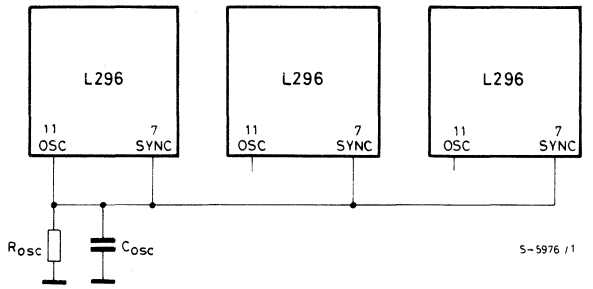
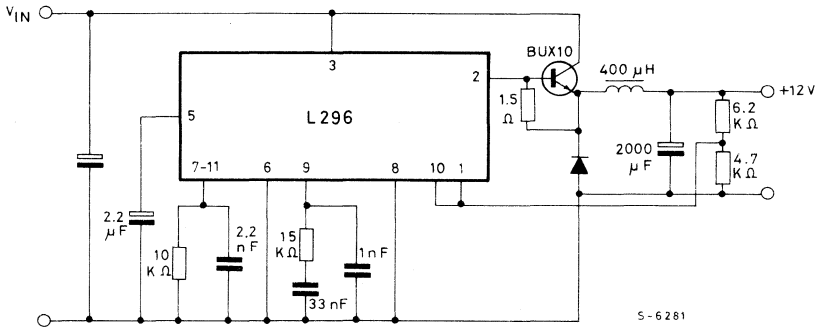



Fig. 16 - 12V/10A Power Supply



# L387

**ADVANCE DATA**

## VERY LOW DROP 5V VOLTAGE REGULATOR

- PRECISE OUTPUT VOLTAGE (5V ± 4%)
- VERY LOW DROPOUT VOLTAGE
- OUTPUT CURRENT IN EXCESS OF 500 mA
- POWER-ON, POWER-OFF INFORMATION (RESET FUNCTION)

The L387 is a very low drop voltage regulator in a PENTAWATT package specially designed to provide stabilized 5V supplies in consumer and industrial applications. Thanks to its very low input/output voltage drop this device is very useful in battery powered equipment, reducing consumption and prolonging battery life. A reset output makes the L387 particularly suitable for microprocessor systems. This output provides a reset pulse when power is applied (after an externally programmable delay) and goes low when power is removed, inhibiting the microprocessor.

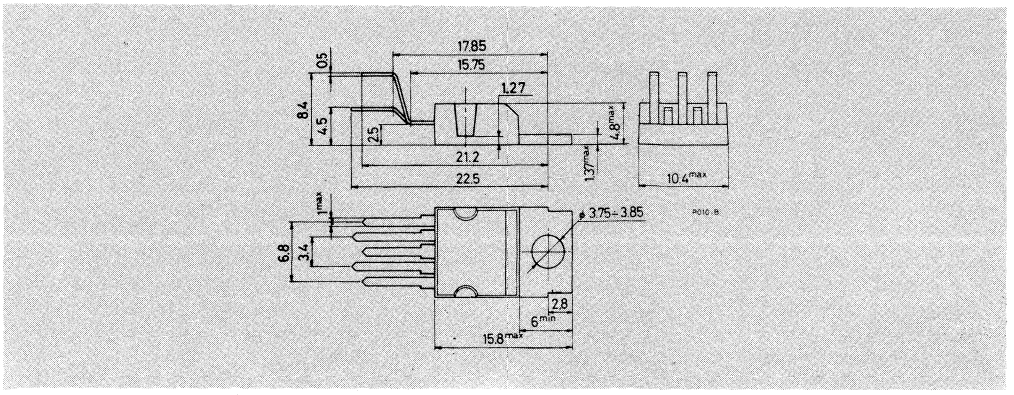
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_i$ | Forward input voltage | 28 | V |
| $T_{op}$ | Operating junction temperature | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |

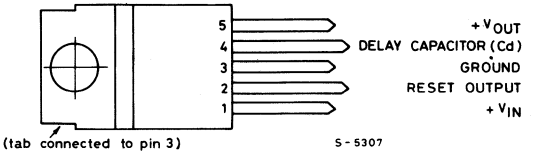
**ORDERING NUMBER:** L387

## MECHANICAL DATA

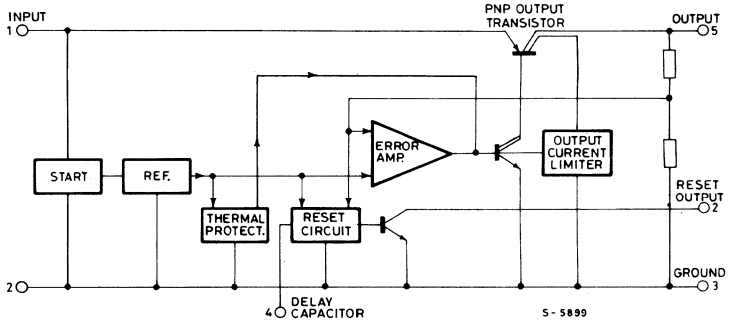
Dimensions in mm



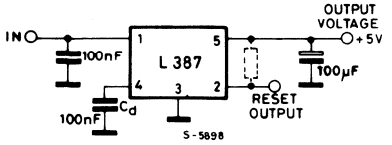
## CONNECTION DIAGRAM
(top view)



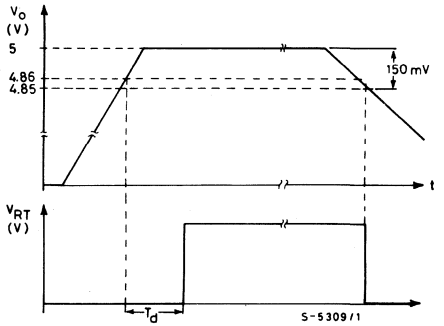

## BLOCK DIAGRAM




## TEST AND APPLICATION CIRCUIT




## TIMING DIAGRAM FOR RESET FUNCTION




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 4 | °C/W |

**ELECTRICAL CHARACTERISTICS** (Refer to the test circuit, $V_I$ = 12V, $T_j$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_o$ | Output voltage | $I_o$ = 5 mA to 500 mA | 4.80 | 5 | 5.20 | V |
| $V_i$ | Operating input voltage | | | | 26 | V |
| $\Delta V_o$ | Line regulation | $V_i$ = 6 to 26V $I_o$ = 5 mA | | 5 | | mV |
| $\Delta V_o$ | Load regulation | $I_o$ = 5 to 500 mA | | 15 | | mV |
| $V_i$-$V_o$ | Dropout voltage | $I_o$ = 500 mA | | 0.60 | 0.8 | V |
| $I_q$ | Quiescent current | $I_o$ = 0 mA<br>$I_o$ = 150 mA<br>$I_o$ = 500 mA | | 5<br>20<br>100 | —<br>40<br>300 | mA |
| $\frac{\Delta V_o}{\Delta T}$ | Temperature output voltage drift | | | -0.5 | | mV/°C |
| SVR | Supply voltage rejection | $I_o$ = 350 mA f = 120 Hz<br>$C_o$ = 100 $\mu$F $V_i$ = 12V ± 5 Vpp | | 60 | | dB |
| $I_{sc}$ | Output short circuit current | | | 0.8 | | A |
| $V_R$ | Reset output voltage | $I_R$= 16 mA $V_o \leqslant$ 4.75V | | | 0.8 | V |
| $I_R$ | Reset output leakage current | $V_o$ in regulation | | | 50 | $\mu$A |
| $t_d$ | Delay time for reset output | Cd = 100 nF | | 30 | | ms |
| $V_{RT}$ | Reset threshold | | 4.75 | $V_o$ -150mV | | V |
| $V_{RTH}$ | Threshold hysteresis | | | 10 | | mV |

Fig. 1 - Dropout voltage vs. output current

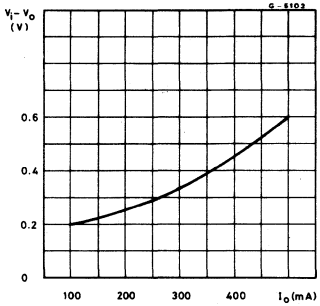



Fig. 2 - Quiescent current vs. output current

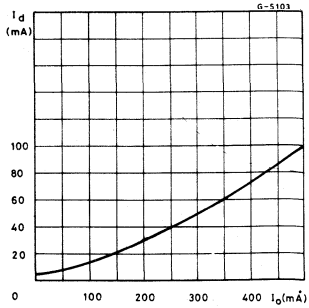
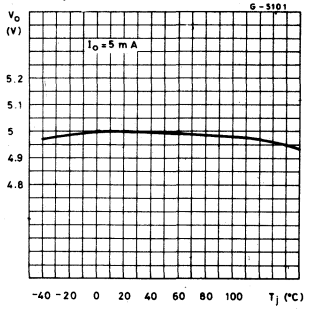



Fig. 3 - Output voltage vs. temperature



L4705
L4785
L4710

# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## VERY LOW DROP VOLTAGE REGULATORS

- INPUT/OUTPUT DROP TYP. 0.6V
- 500 mA OUTPUT CURRENT
- 80V LOAD DUMP PROTECTION
- -80V TRANSIENT PROTECTION
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION
- OUTPUT CURRENT LIMITING
- THERMAL SHUTDOWN

L4700 series voltage regulators feature a very low voltage drop, an output current of 500 mA and protection against load dump transients of ± 80V. Available in 5V, 8.5V and 10V (± 4%) versions, these regulators also include reverse polarity protection, overvoltage protection, output current limiting and a thermal shutdown circuit.
L4700 series regulators are specially designed for automotive and industrial applications where the electrical environment is very demanding and low voltage drop is required. For example, the L4705 can be used in 5V automotive applications, continuing to function even when the battery voltage falls to 6V, a common event during starting. Moreover, the L4705 is fully protected against the transients, overvoltages and polarity reversal encountered on the battery rail.

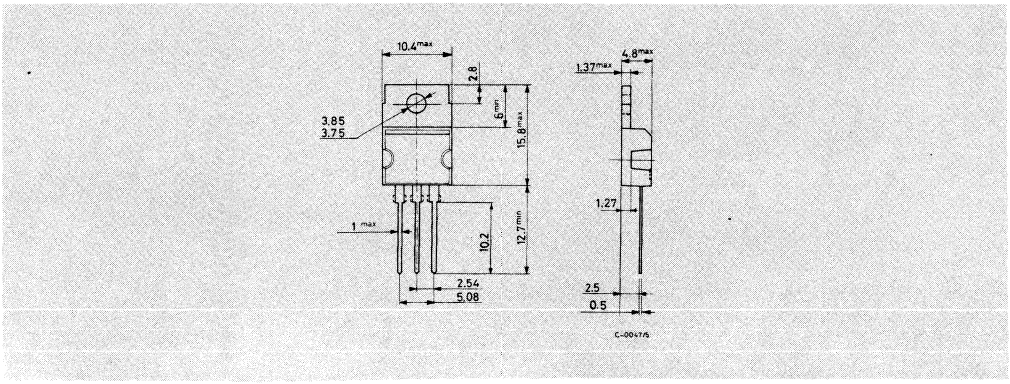
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_i$ | Forward input voltage | 35 | V |
| $V_i$ | Reverse input voltage | -18 | V |
| $V_t$ | Positive transient peak voltage (t = 300 ms) | + 80 | V |
| $V_t$ | Negative transient peak voltage (t = 100 ms) | -80 | V |
| $T_{op}$ | Operating junction temperature | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |

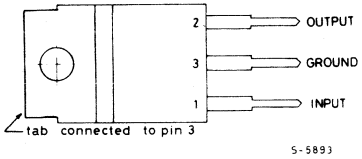
**ORDERING NUMBER:** L4705CV (5V), L4785CV (8.5V), L4710CV (10V)

## MECHANICAL DATA

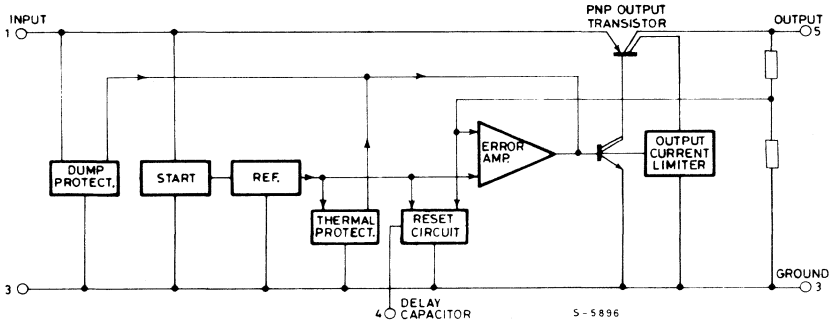
Dimensions in mm



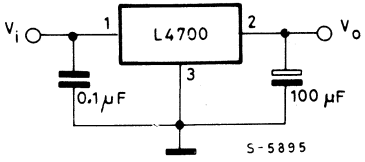
## CONNECTION DIAGRAM (top view)




## BLOCK DIAGRAM




## TEST AND APPLICATION CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 4 | °C/W |

## ELECTRICAL CHARACTERISTICS ($V_i$ = 14.4V, $T_j$ = 25°C)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_o$ | Output voltage | $I_o$ = 5 mA to 500 mA | 4.80 | 5 | 5.20 | V |
| | | | 8.16 | 8.5 | 8.84 | V |
| | | | 9.6 | 10 | 10.4 | V |
| $V_i$ | Operating input voltage | (*) see note | | | 28 | V |
| $\Delta V_o/V_o$ | Line regulation | $V_i$ = 11 to 26V $I_o$ = 5 mA | | 1 | | mV/V |
| $\Delta V_o/V_o$ | Load regulation | $I_o$ = 5 to 500 mA | | 3 | | mV/V |
| $V_i$-$V_o$ | Dropout voltage | $I_o$ = 500 mA | | 0.6 | 0.9 | V |
| $I_q$ | Quiescent current | $I_o$ = 0 mA | | 6 | | mA |
| | | $I_o$ = 150 mA | | 20 | 40 | mA |
| | | $I_o$ = 500 mA | | 130 | | mA |
| $\frac{\Delta V_o}{\Delta T \cdot V_o}$ | Temperature output voltage drift | | | 0.1 | | $\frac{mV}{°C \cdot V}$ |
| SVR | Supply voltage rejection | $I_o$ = 350 mA f = 120 Hz<br>$C_o$ = 100 μF $V_i$=$V_o$+3V+2$V_{pp}$ | | 55 | | dB |
| $I_{sc}$ | Output short circuit current | | | 800 | | mA |

(*) For a DC input voltage 28V < $V_i$ < 35V the device is not operating.

Fig. 1 - Dropout voltage vs. output current

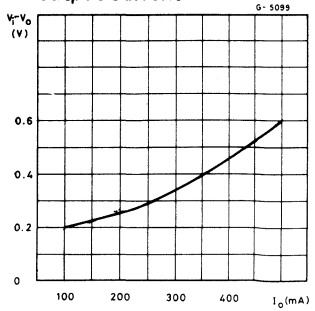



Fig. 2 - Quiescent current vs. output current

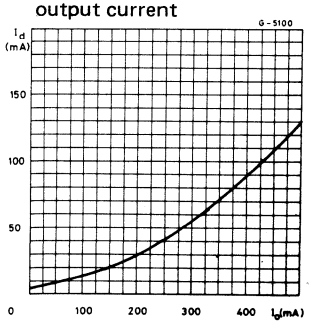
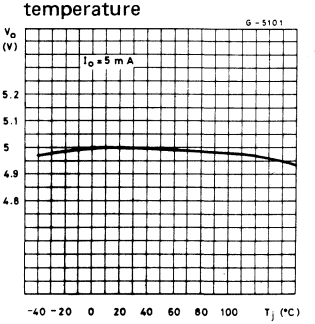



Fig. 3 - Output voltage vs. temperature



# LINEAR INTEGRATED CIRCUITS

**L4805**
**L4885**
**L4810**

**PRELIMINARY DATA**

## VERY LOW DROP VOLTAGE REGULATORS

- INPUT/OUTPUT DROP TYP. 0.4V
- 400 mA OUTPUT CURRENT
- LOW QUIESCENT CURRENT
- 60V LOAD DUMP PROTECTION
- -60V TRANSIENT PROTECTION
- REVERSE POLARITY PROTECTION
- OVERVOLTAGE PROTECTION
- FOLDBACK CURRENT LIMITING
- THERMAL SHUTDOWN

L4800 series devices are voltage regulators with a very low voltage drop (typically 0.4V at full rated current), output current up to 400 mA, low quiescent current and comprehensive on-chip protection. These devices are protected against load dump transients of ± 60V, input overvoltage, polarity reversal and overheating. A foldback current limiter protects against load short circuits. Available in 5V, 8.5V and 10V versions (all ± 4%), these regulators are designed for automotive, industrial and consumer applications where low consumption is particularly important.
In automotive applications the L4805 is ideal for 5V logic supplies because it functions with battery voltages as low as 5.5V. In battery backup and standby applications the low consumption of these devices extends battery life.

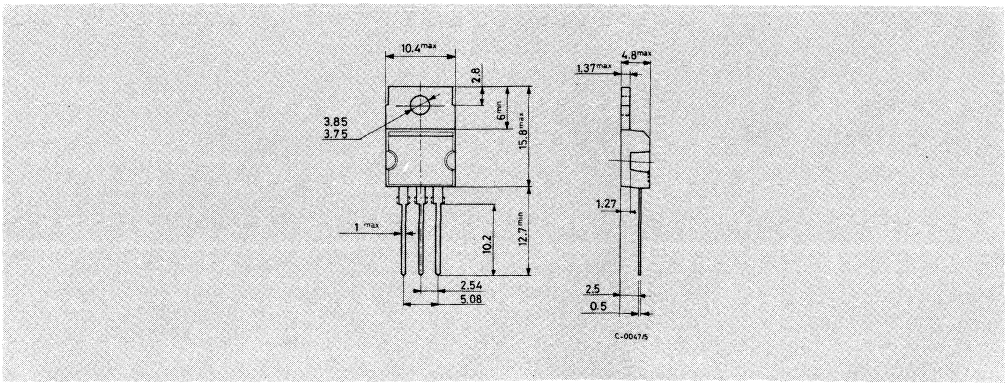
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_i$ | Forward input voltage | 26 | V |
| $V_i$ | Reverse input voltage | -18 | V |
| $V_t$ | Positive transient peak voltage (t = 300 ms) | +60 | V |
| $V_t$ | Negative transient peak voltage (t = 100 ms) | -60 | V |
| $T_{op}$ | Operating junction temperature | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |

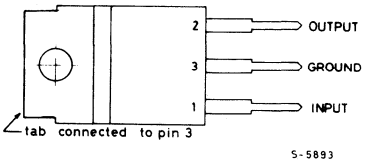
**ORDERING NUMBER:** L4805CV (5V), L4885CV (8.5V), L4810CV (10V)

## MECHANICAL DATA

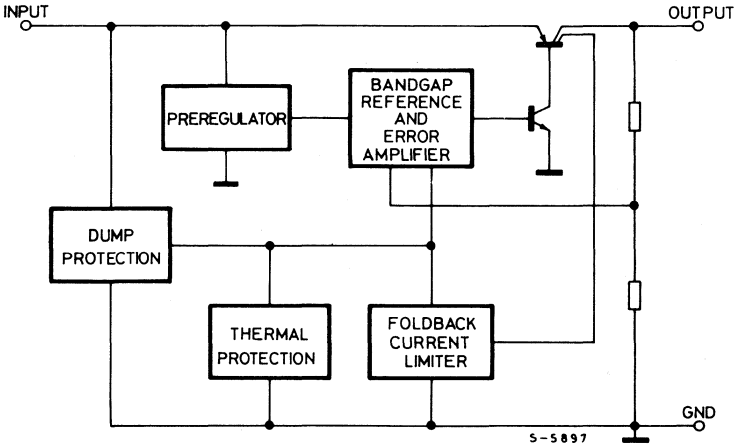
Dimensions in mm



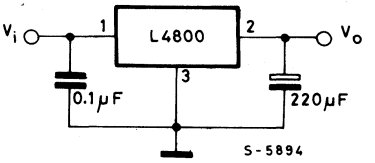
## CONNECTION DIAGRAM (top view)




## BLOCK DIAGRAM




## TEST AND APPLICATION CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 4 | °C/W |

## ELECTRICAL CHARACTERISTICS ($V_i$ = 14.4V, $T_j$ = 25°C)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_o$ | Output voltage | $I_o$ = 5 mA to 400 mA | 4.80 | 5 | 5.20 | V |
| | | | 8.16 | 8.5 | 8.84 | V |
| | | | 9.6 | 10 | 10.4 | V |
| $V_i$ | Operating input voltage | | | | 26 | V |
| $\Delta V_o/V_o$ | Line regulation | $V_i$ = 11 to 26V $I_o$ = 5 mA | | 1 | 10 | mV/V |
| $\Delta V_o/V_o$ | Load regulation | $I_o$ = 5 to 400 mA | | 3 | 15 | mV/V |
| $V_i-V_o$ | Dropout voltage | $I_o$ = 400 mA | | 0.4 | 0.7 | V |
| | | $I_o$ = 150 mA | | 0.2 | 0.4 | V |
| $I_q$ | Quiescent current | $I_o$ = 0 mA | | 0.8 | 3 | mA |
| | | $I_o$ = 150 mA | | 16 | 45 | mA |
| | | $I_o$ = 400 mA | | 80 | 100 | mA |
| $\frac{\Delta V_o}{\Delta T \cdot V_o}$ | Temperature output voltage drift | | | 0.1 | | $\frac{mV}{°C \cdot V}$ |
| SVR | Supply voltage rejection | $I_o$ = 350 mA f = 120 Hz<br>$C_o$ = 100 $\mu$F $V_i=V_o+3V+2V_{pp}$ | | 60 | | dB |
| $I_o$ | Max output current | | | 750 | | mA |
| $I_{sc}$ | Output short circuit current (fold back condition) | | | 220 | | mA |

Fig. 1 - Dropout voltage vs. output current

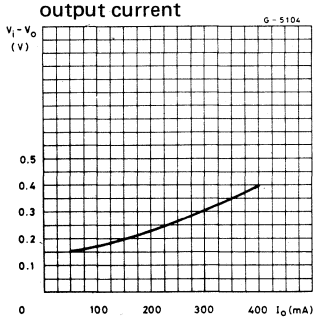



Fig. 2 - Quiescent current vs. output current

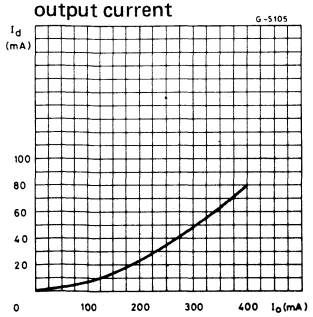


Fig. 3 - Output voltage vs. temperature

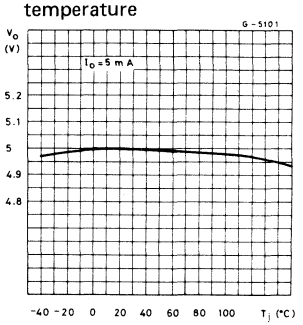



Fig. 4 - Foldback current limiting (L4805)

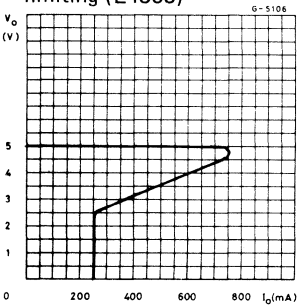
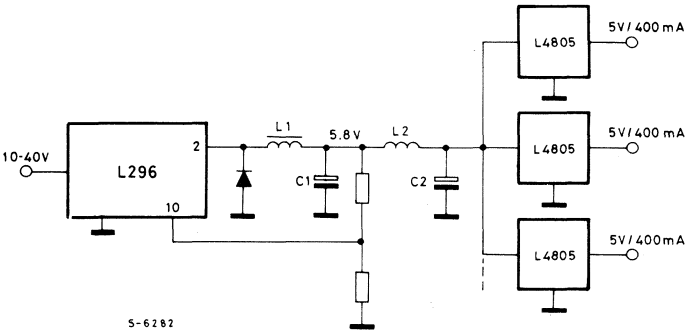



Fig. 5 - Preregulator for distributed supplies



## ON-SCREEN TUNING SCALE AND BAND DISPLAY

- DIGITAL TUNING BAR DISPLAY WITH MINIMUM EXTERNAL PRESETS
- ON-SCREEN DISPLAY OF THE BAND
- VERTICAL POSITION ON THE SCREEN EXTERNALLY ADJUSTABLE
- AUTOMATIC DISPLAY AT SEARCH COMMAND
- DESIGNED FOR USE WITH THE M193 ELECTRONIC PROGRAM MEMORY
- M191: STANDARD VERSION
- M091: FOR AUTOMATIC SEARCH IN FRENCH STANDARD APPLICATIONS

The M091 and M191 are monolithic integrated circuits designed to display on the screen of the television receiver a variable length strip corresponding to the voltage applied to the varicap tuner.
A variable number of rectangles symbolizing the selected band can also be displayed.
The circuits operate in conjunction with the M193 (Electronic Program Memory), from which they take the voltage and band information in a digital serial mode.
The 7 most significant digits of voltage information coming from the M193 are digitally converted into a 64 step variable pulse width giving either positive and negative polarity outputs for easy and versatile interfacing.
The variable length strip is displayed over 11 lines of a half frame picture with nine vertical graduations of 31 lines.
The vertical position of the strip can be adjusted with an external potentiometer over the whole screen.
The 2 digits of band information determine the number of rectangles appearing on the screen under the tuning strip. The rectangles are displayed over 11 lines of a half frame picture.
Automatic display is provided when the Electronic Program Memory is in the Search Mode; display on manual command is also possible.
The M191 is the standard version. The M091 is alternatively for displaying the tuning voltage when the automatic search is made by scanning the band in a reverse way (i.e. from 30 to 0V) as is required by the French standard.
The M091 displays 30V (maximum length of the strip) when the M193 Electronic Program Memory transmits information corresponding to 0V. It displays 0V when the M193 transmits information corresponding to 30V.
It displays 0V when the M193 transmits information corresponding to 30V.
The M091 and M191 are constructed in N-channel silicon gate technology and are available in a 16 pin dual in-line plastic package.

## ABSOLUTE MAXIMUM RATINGS

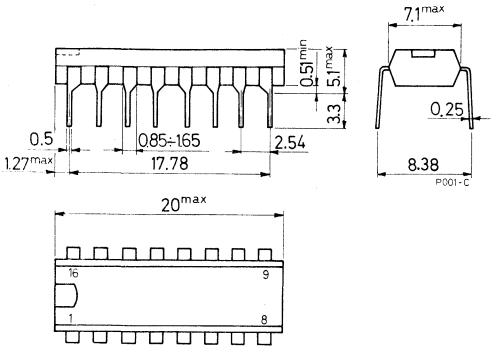
| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 20 | V |
| $V_I$ | Input voltage | -0.3 to 20 | V |
| $I_I$ | Input current | -5 | mA |
| $V_{O\,(off)}$ | Off-state output voltage | 20 | V |
| $I_O$ | Output current (except pins 12-13) | 5 | mA |
| | (pins 12-13) | 15 | mA |
| $P_{tot}$ | Total package power dissipation | 500 | mW |
| $T_{stg}$ | Storage temperature | -65 to 150 | °C |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

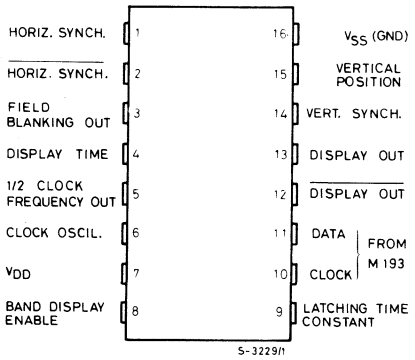
**ORDERING NUMBERS:** M191 B1
M091 B1

# M 091
# M 191

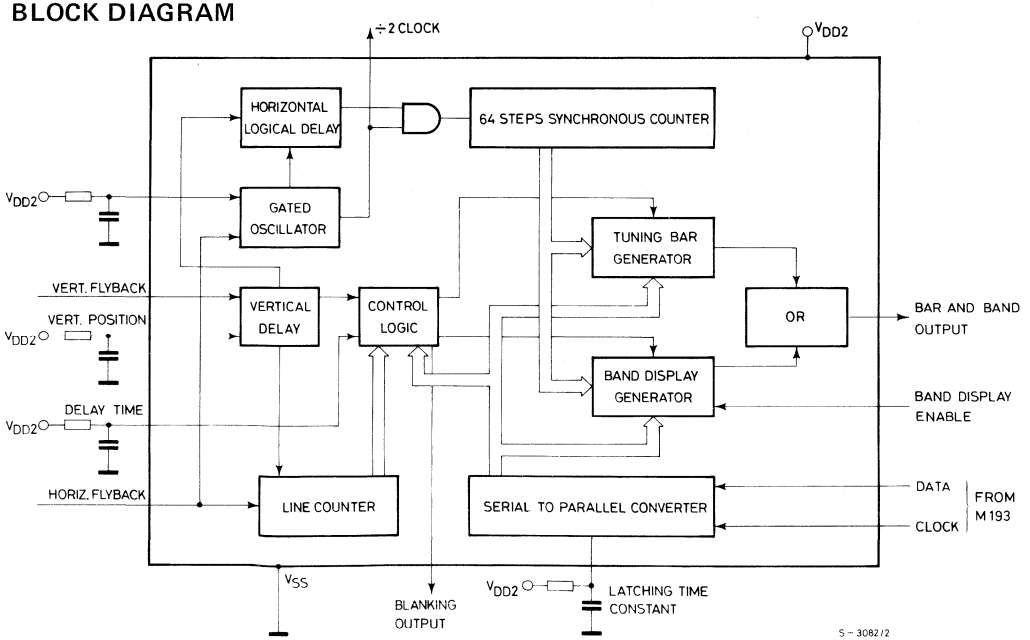
## MECHANICAL DATA (dimensions in mm)




## PIN CONNECTIONS




## BLOCK DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

| Parameter | | Min. | Typ. | Max. | |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 11.5 | 13 | 14.5 | V |
| $V_I$ | Input voltage | | | 14.5 | V |
| $V_{O\,(off)}$ | Off-state output voltage | | | 14.5 | V |
| $I_O$ | Output current - all pins except 4-6-12-13* | | | 1 | mA |
| | - pin 6 | | | 3 | mA |
| | - pins 12-13 | | | 10 | mA |
| f | Clock frequency | | 1.8 | 2.2 | MHz |
| $T_{op}$ | Operating temperature | 0 | | 70 | °C |
| $P_{tot}$ | Total package power dissipation | | | 500 | mW |
| $C_9$ | Capacitance at pin 9 | | 330 | 390 | pF |
| $C_6$ | Capacitance at pin 6 | | 68 | 100 | pF |
| $C_{15}$ | Capacitance at pin 15 | | 270 | 330 | nF |
| $C_4$ | Capacitance at pin 4** | | 10 | 12 | μF |
| $R_{4,\,15}$ | Resistance at pins 4-15 | | 220 | 270 | KΩ |

* $I_{O4}$ The output current of pin 4 is internally limited.
** $C_4$ Values up to 100 μF are allowed using a 1KΩ resistor in series with pin 4.

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions).

Typical values are at $T_{amb}$= 25°C, $V_{DD}$= 13V.

| Parameter | | Test conditions | Pins | Values | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{IL}$ | Low level input voltage | $V_{DD}$= 11.5 to 14.5V | 1-2-10-11-14 | | | 0.8 | V |
| $V_{IH}$ | High level input voltage | $V_{DD}$= 11.5 to 14.5V | 1-2-10-11-14 | 3.5 | | | V |
| $V_{OL}$ | Low level output voltage | $V_{DD}$= 11.5V<br>$I_{OL}$ = 10 mA | 12-13 | | | 1 | V |
| | | $V_{DD}$= 11.5V<br>$I_{OL}$= 1 mA | 3 | | | 1 | V |
| $V_T$ | Threshold voltage | $V_{DD}$= 11.5 to 14.5V | 6-9-15 | | 4 | | V |
| | | | 4-8 | | 2 | | |
| $I_I$ | Input current | $V_I$ = 14.5V | | | | 10 | μA |
| $I_{O\,(off)}$ | Off-state output current | $V_{DD}$ = 14.5V | 3-4-5-9-15 | | | 20 | μA |
| | | | 12-13 | | | 100 | |
| $I_{DD}$ | Supply current | $V_{DD}$= 14.5V | | | | 25 | mA |

## DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb}$= 25°C)

| Parameter | | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{TLH}$, $t_{THL}$ | Transition time | Pins 12–13 See fig. 3 | | 80 | | ns |
| $t_D$ | Delay time | | | 50 | | ns |

## TYPICAL APPLICATION

Fig. 1

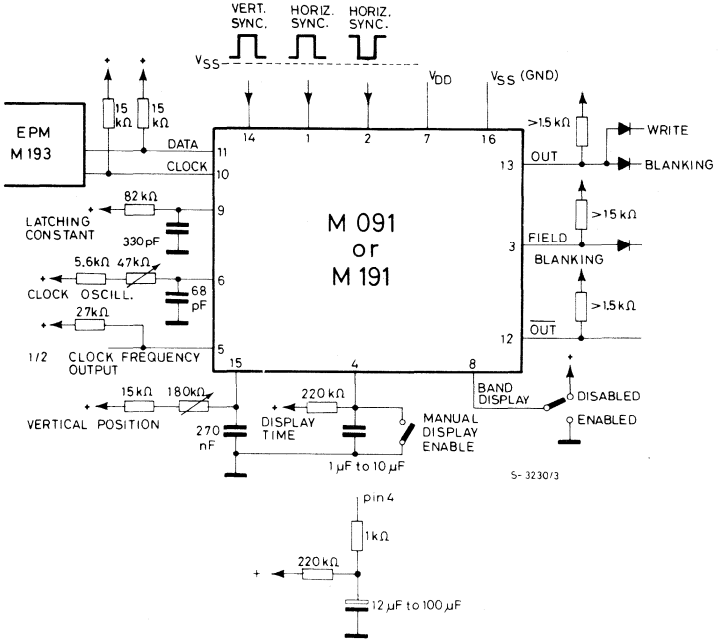
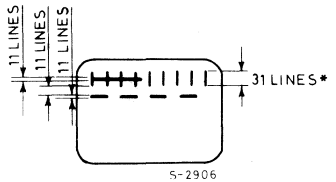
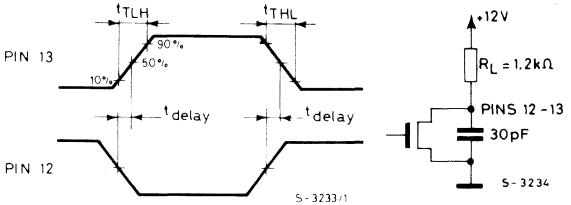



Fig. 2




* : THE LINES CORRESPOND TO A HALF FRAME

Fig. 3

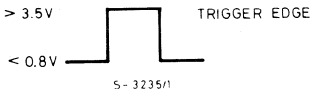


## DESCRIPTION

### Pins 1, 2 - Horizontal synchronization

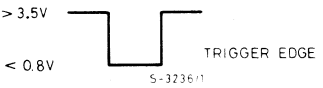
Two Horizontal sync inputs are provided to allow for positive or negative pulses from the TV receiver.
Pin 1 is designed to accept a positive pulse derived from the line flyback through an interface.
The circuit is triggered on the negative edge of the incoming pulse.

Fig. 4 - Pin 1




The negative flyback pulses must be applied to pin 2. In this case the circuit is triggered on the positive edge of the pulse.

Fig. 5 - Pin 2




The display is delayed for a time corresponding to 32 clock periods after the triggering.
With a clock frequency of 1.8 MHz the delay is 9 $\mu$sec.
When pin 1 is used, pin 2 must be connected to $V_{SS}$ (GND); when using pin 2, pin 1 must be at $V_{DD}$.

### Pin 3 - Field blanking output

An open drain transistor is disabled during the lines which correspond to the display of the tuning scale and band information. This makes it possible to write the tuning scale and the band identification rectangles on a dark or alternative colour area. The signal is present for the full line period.

### Pin 4 - Display time input

The display is automatically enabled when the M193 (Electronic Program Memory) is in the Search mode.
The RC network applied to pin 4 determines the time the display will last after a station is found.
When identification occurs the capacitor is unclamped and allowed to be charged by the external resistor.
The display is disabled when an internal threshold is reached.
The display is also enabled if the capacitor is discharged by connecting this pin to $V_{SS}$ (GND) with an external clamp.
If a capacitor $>$ 10 $\mu$F is used a 1 K$\Omega$ resistor must be placed in series with pin 4.

### Pin 5 - 1/2 frequency clock output

The clock frequency divided by two is present on this pin for measurement purposes. To allow this, connect temporarily pin 1 to $V_{SS}$ and pin 2 to $V_{DD}$. The output is open drain and an external pull-up resistor is needed.
If the output is not used it must be connected to $V_{SS}$.

## DESCRIPTION (continued)

### Pin 6 - Clock oscillator input

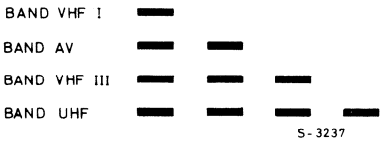
This pin is connected to a RC network as shown in fig. 1.
The clock frequency determines the horizontal width on the screen of the tuning scale, of the rectangles and the distance of the display from the left edge of the screen.
Fine adjustment of the clock frequency is obtained by the trimming resistor. Typical clock frequency is 1.8 MHz.

### Pin 7 - $V_{DD}$

### Pin 8 - Band display enable

When this pin is connected to $V_{SS}$ (GND) a band display with the following format is enabled, on command, together with the tuning voltage display.

Fig. 6

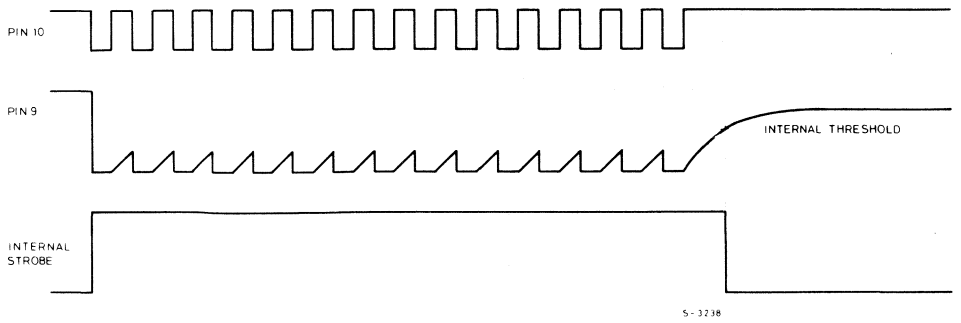



If this pin is connected to $V_{DD}$ only the tuning voltage will be displayed.

### Pin 9 - Latching time constant

An RC time constant must be applied to this pin to generate the internal latching signal.
The content of the internal shift register is transferred to the internal decoding circuit only at the end of the clock burst to avoid noise on the display during data transfer.
This is made by integrating the incoming clock burst with the RC time constant connected to pin 9 as shown in fig. 7.

Fig. 7

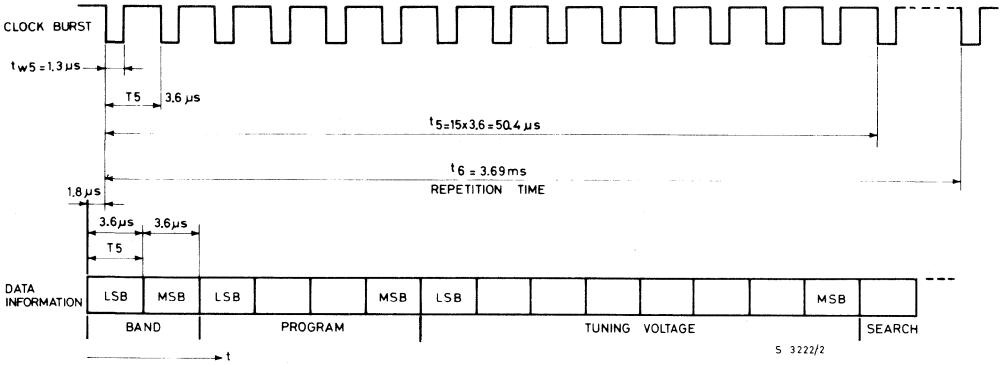


## DESCRIPTION (continued)

### Pin 10 - Clock input

This pin accepts the burst containing the 15 clock pulses available from the M193. The burst is used to load the serial Data on pin 11 into the internal 15 bit shift register (see fig. 8).

Fig. 8




### Pin 11 - Data input

This pin accepts the 15 bit serial Data information available from the M193 EPM.
The burst contains 2 bits for band information, 4 bits for program, 8 bits for tuning voltage and 1 bit which indicates if the system is in the Search mode.

### Pin 12 - Inverted video signal output

The signals of pin 13 are inverted and presented on this pin to allow easy interfacing in some chroma kits. The output is open drain.

### Pin 13 - Video signal output

The tuning scale and band information video signal is available on this pin, a load resistor is connected between the open drain output transistor and $V_{DD}$. White level corresponds to disable of the internal transistor.

### Pin 14 - Vertical synchronization

The frame flyback pulse must be applied to this pin by means of an interface. The signal must be positive. The circuit is triggered by the negative edge of the pulse.

Fig. 9



## DESCRIPTION (continued)

### Pin 15 - Vertical position input

An internal monostable is triggered by the frame pulse applied on pin 14.
The display is allowed at the end of the cycle of the monostable. The RC network applied to this pin gives the time constant of the monostable determining the position of the display on the screen.

### Pin 16 - $V_{SS}$ (GND)

All voltages quoted are referred to Pin 16.




## PCM REMOTE CONTROL RECEIVER

- 128 CHANNEL DECODING
- 5-BIT BINARY STATIC OUTPUTS (32 PROGRAMS)
- 4 ANALOGUE CONTROLS/63 STEPS
- 445 TO 510 kHz REFERENCE OSCILLATOR
- 5V SUPPLY VOLTAGE
- LOCAL CONTROLS AVAILABLE
- INTEGRATED DIGITAL POWER ON RESET
- SERIAL "I-BUS" OUTPUT FOR TELETEXT AND VIEWDATA
- TO BE USED IN CONJUNCTION WITH M709 OR M710 R.C. TRANSMITTERS (FLASH TRANSMISSION MODE)
- TECHNICAL NOTE TN 155 AVAILABLE

The M104 has been developed for remote control of TV or radio sets in conjunction with M709/M710 R.C. transmitters. The receiver decodes the transmitted commands only if the transmitted address matches the address code selected at the receiver. 2 addresses are available for this purpose. The accepted command is afterwards released on the serial data bus.

When the M104 is operating in the subsystem mode (e.g. Teletext, Viewdata) and a command is continuously received, the Data Bus is disabled after the first signal has been released; it is reenabled after the reception or the internal generation of the "end of transmission code". The frequency of the clock oscillator can be in the range 445 to 510 kHz and no synchronization is required with the transmitter clock.

The M104 is produced with N-channel silicon gate technology and is assembled in a 28 pin dual in-line plastic package.

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 7 | V |
| $V_I$ | Input voltage (except pin 2) | -0.3 to 7 | V |
| | Input voltage pin 2 | -0.3 to 14 | V |
| $V_{O(off)}$ | Off-state output voltage (pins 26, 25, 24, 23, 22, 27, 21, 20, 19, 18, 28) | 14 | V |
| | Off-state output voltage (pins 17, 10, 9, 4, 12, 11, 13) | 7 | V |

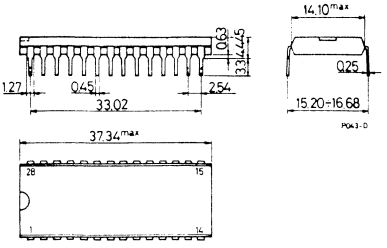
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ORDERING NUMBER:** M104 B1

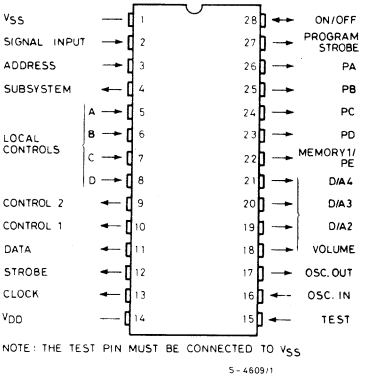
# M104

## MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package



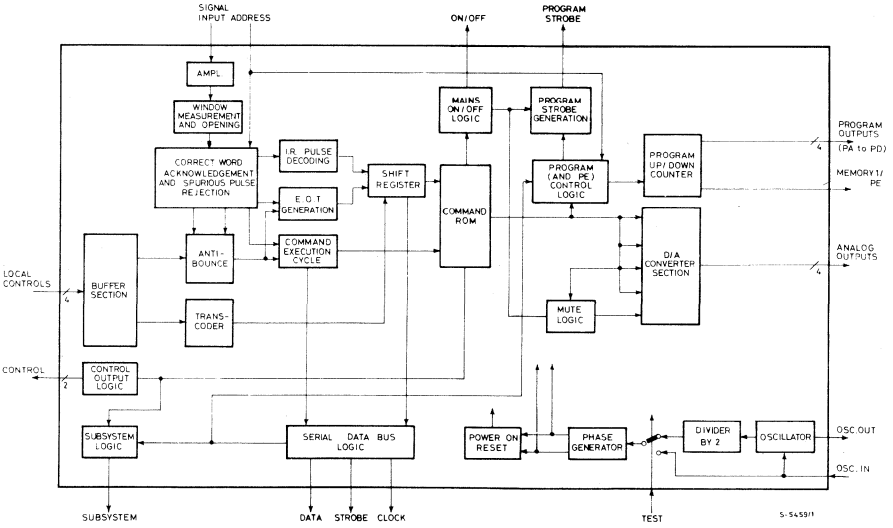

## PIN CONNECTIONS




NOTE: THE TEST PIN MUST BE CONNECTED TO $V_{SS}$

S-4609/1

## BLOCK DIAGRAM




## RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | 4.75 to 5.25 | V |
| $V_I$ | Input voltage (except pin 2) | 0 to 5.25 | V |
| | Input voltage pin 2 | 0 to 13.2 | V |
| $V_{O(off)}$ | Off state output voltage (pins 26, 25, 24, 23, 22, 27, 21, 20, 19, 18, 28) | max 13.2 | V |
| | Off state output voltage (pins 17, 10, 9, 4, 12, 11, 13) | max 5.5 | V |

Note: Test pin and unused open drain outputs must be connected to $V_{SS}$.

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at 5V, $T_{amb} = 25°C$

| Parameter | | Pins | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{IL}$ | Input low voltage | 3-28 | | | | 0.8 | V |
| | | 5-6-7-8 | | | | 1.5 | |
| $V_{IH}$ | Input high voltage | 3-28 | | 2.5 | | | V |
| | | 5-6-7-8 | | 4 | | | |
| $V_{IPP}$ | Peak to peak voltage | 2 | | 0.5 | | 13.2 | V |
| $V_{OL}$ | Output low voltage | 26-25-24-23-22 10-9-21-20 19-18-28-4 | $V_{DD}$= 4.75V $I_{OL}$= 0.8 mA | | | 0.4 | V |
| | | 27-12-11-13 | $V_{DD}$= 4.75V $I_{OL}$= 1.6 mA | | | 0.4 | |
| $I_{IL}$ | Input low current | 3-5-6-7-8 | $V_{DD}$= 5.25V $V_{IL}$= 0.4V | | | -0.4 | mA |
| $I_{IH}$ | Input high current | 28-3 | $V_{DD}$= 5.25V $V_{IH}$= 5.25V | | | 25 | μA |
| $I_{O(off)}$ | Output leakage current | 26-25-24-23-22 27-21-20-19 18-28 | $V_{DD}$= 5.25V $V_{O(off)}$= 13.2V | | | 50 | μA |
| | | 10-9-4 12-11-13 | $V_{DD}$= 5.25V $V_{O(off)}$= 5.25V | | | 25 | |
| $I_{DD}$ | Supply current | 14 | $V_{DD}$= 5.25V all outputs open | | | 50 | mA |

## DESCRIPTION

### Pin 1 – $V_{SS}$

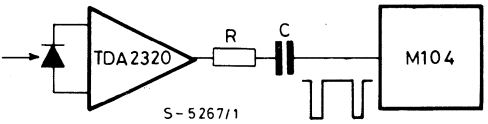
The substrate of the ICs is connected to this pin. It is the reference pin for all parameters of the ICs.

### Pin 2 – Signal input

The minimum signal to be applied is 0.5V peak to peak.
The receiver input section performs the following tests on the incoming signal to achieve the necessary noise immunity:

- measurement of the pulse distance (time base synchronization)
- check of the position of the received bits opening window at the time bases
- check of the parity bit
- check of the absence of pulses between the parity bit and the stop-pulse
- check of noise level; the receiver checks parasitic transient inside and outside the time windows.

If the above test conditions are not fulfilled, the received word is rejected and not decoded. If the received signal is acknowledged as a valid word it is stored and decoded. The received coded word is also released on the serial data bus.
The end of transmission will be acknowledged by receiving the end of transmission code or by means of an internal timer if the transmission remains interrupted for more than about 550 ms.
The end of transmission code is also released on the Data Bus.




| SUPPLY VOLTAGE OF TDA 2320 | R | C |
|---|---|---|
| 5 | 2.2K | 4.7 nF |
| 12 | 10K | 4.7 nF |

## Pin 3 — Address input

The receiver decodes only signals transmitted with addresses 1 and 2. This input has integrated pull-up resistor of 50 KΩ (max)

| Address | Pin 3 |
|---|---|
| 1 | Low |
| 2 | High |

## Pin 4 — Subsystem mode indication

This open drain output is set high at power on reset and can be switched low with commands 56 to 62. It is repositioned high by commands 2, 12 and 63.
When the receiver is in the subsystem mode (output low) and a command is received continuously the data bus is disabled after the first signal has been released.
It is reenabled after the reception or the internal generation of the "end of transmission code".
No Program change command is executed when M104 is in subsystem mode.

## Pins 5-6-7-8 — Local control inputs LOC-A, LOC-B, LOC-C, LOC-D

These inputs are provided for emergency operations. Therefore only a few controls are provided.
Local input commands and I.R. commands have the same priority.
If a complete I.R. command has been received, the local inputs are blocked until the command has been executed and the "end of transmission code" generated.
Viceversa an I.R. signal cannot be decoded until an issued local command has been executed and the "end of transmission" released.
All these inputs have integrated pull-up resistor of 50 KΩ (max.)
Each command is accepted after it has been present continuously for about 40 ms.

| Inputs | | | | Data bus codes | | | | | | Function |
|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | C1 | C2 | C3 | C4 | C5 | C6 | |
| H | H | H | H | | | | | | | |
| L | H | H | H | L | L | L | H | L | L | Program + |
| H | L | H | H | H | L | L | H | L | L | Program – |
| L | L | H | H | H | L | L | L | L | H | Volume – |
| H | H | L | H | H | H | L | L | L | L | |
| L | H | L | H | L | L | L | L | L | H | Volume + |
| H | L | L | H | L | H | L | L | L | H | A 2 + |
| L | L | L | H | L | H | L | H | L | L | Normalization |
| H | H | H | L | L | H | H | H | L | L | Memory 1 H |
| L | H | H | L | H | H | L | L | L | H | A 2 – |
| H | L | H | L | L | L | H | L | L | H | A 3 + |
| L | L | H | L | H | L | H | L | L | H | A 3 – |
| H | H | L | L | H | L | H | H | L | L | Memory 1L |
| L | H | L | L | L | H | H | L | L | H | A 4 + |
| H | L | L | L | H | H | H | L | L | H | A 4 – |
| L | L | L | L | L | H | L | L | L | L | Mains off |

## Pins 9-10 – Control output R2, R1

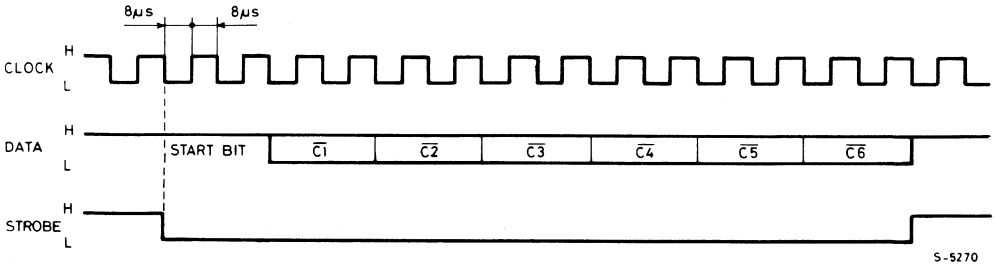
These outputs consist of open drain transistors that are switched on when commands 6 and 7 are issued. The outputs remain switched on for a time variable between 144 and 173 ms after reception of the command ($f_{ref}$= 500 kHz). They can be used for example to control fine tuning or automatic search commands of M293 (Electronic Program Memory).

| Command N° | R1 (pin 10) | R2 (pin9) |
|---|---|---|
| 6 | L | H |
| 7 | H | L |

## Pins 11-12-13 – Serial Data Bus

DATA (pin 11)
STROBE (pin 12)
CLOCK (pin 13)

Each signal, either remote or local, is released on this serial data bus to control external circuits (Teletext, Viewdata, Videorecorder, Hi-Fi, etc.).
The serial data bus has the following configuration:




All outputs have open drain configuration. See also description of pin 4 for subsystem mode operation.

### Pin 14 – $V_{DD}$

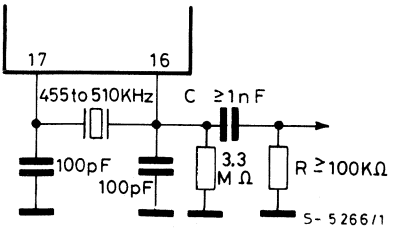
The supply voltage has to be 5V ± 5%.

### Pin 15 – Test

This pin is used for testing and has to be connected to $V_{SS}$.

### Pins 16-17 – Clock oscillator

The frequency of the clock oscillator should be between 445 and 510 kHz using a cheap ceramic resonator. In these conditions the value of the reference frequency of the transmitter can be in the same range. In other words the transmitter and the receiver can operate with different reference frequencies. The clock signal can be used to drive the clock of other ICs through a capacitor connected at pin 16.



## Pins 18 to 21 – Analogue control outputs

These outputs are provided to control four analogue values (for example volume, brightness, colour saturation and contrast in TV sets).
The outputs deliver square wave signals of 7.8 kHz with a duty cycle variable in 63 steps.
In the case of a continuous command for varying the analogue information, the duty cycle is changed at the rate of the transmitted signal (approximately every 102 ms with $f_{ref}$ = 500 KHz).
Local controls are varied every 115 ms ($f_{ref}$ = 500 kHz).
The circuits is provided with underflow and overflow protection.
At supply on reset the volume output (pin 18) is set at duty cycle 21/64 (pulse = H). All other outputs are set at 31/64.
The normalization command sets all the outputs except volume to mid position (31/64).
The volume output can be switched to $V_{SS}$ and reset to the previous level by means of command 2 (mute). It is also reset by means of the normalization command, volume + and mains off command.
The volume output is muted at each mains on and off command for approximately 0.5 sec.
It is also muted at supply on/off. The analogue outputs cannot be modified in the standby condition (mains off).

## Pin 22 – Memory 1 (PE)

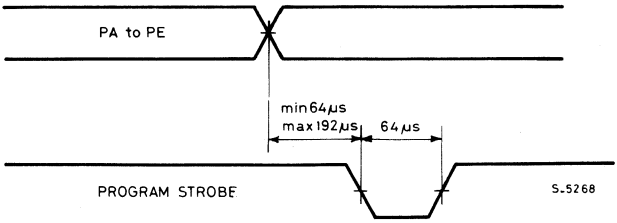
This output can be used as shift command for selection of up to 32 programs.
The output is set at power on to a low level. It can be controlled using commands 13 and 14. In the case of program +/– commands the output is automatically switched if the receiver operates with the address 1 (pin 3 = L) and if the program commands are accepted (see pins 23 to 26 and 4).
Otherwise this output is not affected by the program +/– commands and can be used for general applications. It has open drain configuration.

## Pins 23-24-25-26 – PD, PC, PB, PA Program outputs

Open drain, binary coded, static outputs. At power on reset the outputs are set to program 1 (PA to PD = L L L L).
The program selection can be sequential or direct. If the TV set is in the standby condition the program step-by-step ± commands (8, 9) or the direct program selection commands (16 to 31) can be used to switch on the set.
In the first case the program can be stepped only if the command has been interrupted and a continuous sequential program change command causes program stepping in the up or down direction every 0.57 sec. (every 0.5 sec. if issued from R.C. transmitter).
Direct program selection is possible only by remote control.
The selection of up to 32 programs is possible using the memory 1 output (pin 22) that is put low and high by transmitting the commands 13 and 14 respectively.
All the program and shift commands are blocked when one of the commands from 56 to 62 is issued. This "subsystem mode" condition is reset by commands 2, 12 and 63.

## Pin 27 – Program strobe output

The program strobe signal is generated each time the content of the memory has to be read and each time the mains output is switched off or on. It is therefore generated at direct program selection (16 to 31) program ± stepping (8, 9) and shift commands (13, 14) with address 1.
The strobe signal is not available when the M104 is in the subsystem mode; the output has open drain configuration.




At direct program selection and shift commands, the strobe is available only once.
This output has open drain configuration.

## Pin 28 – Mains on/off

This active low output, is provided to control the on/off switching of the TV set via a transistor and a relay.
When the supply voltage is applied to the device, the output transistor is automatically biased off.
In this "standby" condition, only the mains on commands are accepted.
A mains on command can be given in one of the following ways:

a) – by commands 8, 9 (program +/–)
   – by command 12
   – by commands 16 to 31

All these commands are accepted only when received 5 times (about 0.4 sec).
The "end of transmission" code resets the associated counter.

b) – connecting pin 28 to $V_{SS}$ (GND) for at least 10 µs.

This feature is provided for automatic switch on of the set using a temporarily active slide contact in parallel with the master power on switch.
The command is accepted only when the supply voltage $V_{DD}$ has risen above approximately 4V.
The set can be put in standby by means of command 2. This command also has to be received 5 times.

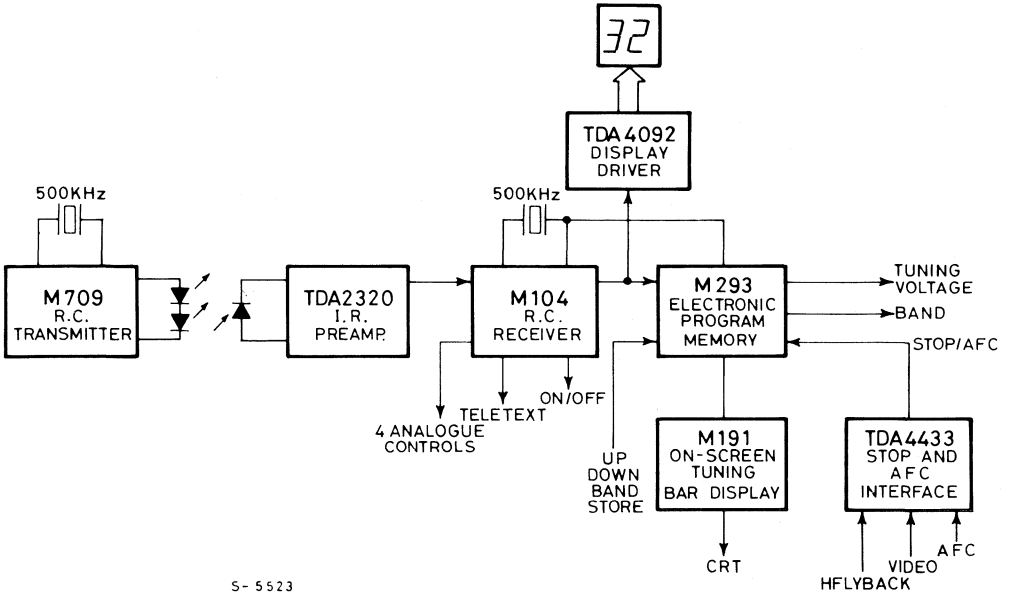
## M104 truth table

| Command No. | I.R. code C1 | C2 | C3 | C4 | C5 | C6 | Local controls A | B | C | D | Data bus code C1 | C2 | C3 | C4 | C5 | C6 | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | L | L | L | L | L | L | End of transmission. |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | | | | | H | L | L | L | L | L | Mute on/off |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | L | L | L | L | L | H | L | L | L | L | Mains off/Mute off/Subsyst. off (pin 4 H) |
| 3 | 1 | 1 | 0 | 0 | 0 | 0 | | | | | H | H | L | L | L | L | |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | | | | | L | L | H | L | L | L | |
| 5 | 1 | 0 | 1 | 0 | 0 | 0 | | | | | H | L | H | L | L | L | |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | | | | | L | H | H | L | L | L | Control 1 L |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | | | | | H | H | H | L | L | L | Control 2 L |
| 8 | 0 | 0 | 0 | 1 | 0 | 0 | L | H | H | H | L | L | L | H | L | L | Program +/Mains on |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | H | L | H | H | H | L | L | H | L | L | Program −/Mains on |
| 10 | 0 | 1 | 0 | 1 | 0 | 0 | L | L | L | H | L | H | L | H | L | L | Normalization/Mute off |
| 11 | 1 | 1 | 0 | 1 | 0 | 0 | | | | | H | H | L | H | L | L | |
| 12 | 0 | 0 | 1 | 1 | 0 | 0 | | | | | L | L | H | H | L | L | Mains on/Subsystem off (pin 4 H) |
| 13 | 1 | 0 | 1 | 1 | 0 | 0 | H | H | L | L | H | L | H | H | L | L | Memory 1 L |
| 14 | 0 | 1 | 1 | 1 | 0 | 0 | H | H | H | L | L | H | H | H | L | L | Memory 1 H |
| 15 | 1 | 1 | 1 | 1 | 0 | 0 | | | | | H | H | H | H | L | L | |
| 16 | 0 | 0 | 0 | 0 | 1 | 0 | | | | | L | L | L | L | H | L | Program 16/Mains on |
| 17 | 1 | 0 | 0 | 0 | 1 | 0 | | | | | H | L | L | L | H | L | Program 1/Mains on |
| 18 | 0 | 1 | 0 | 0 | 1 | 0 | | | | | L | H | L | L | H | L | Program 2/Mains on |
| 19 | 1 | 1 | 0 | 0 | 1 | 0 | | | | | H | H | L | L | H | L | Program 3/Mains on |
| 20 | 0 | 0 | 1 | 0 | 1 | 0 | | | | | L | L | H | L | H | L | Program 4/Mains on |
| 21 | 1 | 0 | 1 | 0 | 1 | 0 | | | | | H | L | H | L | H | L | Program 5/Mains on |
| 22 | 0 | 1 | 1 | 0 | 1 | 0 | | | | | L | H | H | L | H | L | Program 6/Mains on |
| 23 | 1 | 1 | 1 | 0 | 1 | 0 | | | | | H | H | H | L | H | L | Program 7/Mains on |
| 24 | 0 | 0 | 0 | 1 | 1 | 0 | | | | | L | L | L | H | H | L | Program 8/Mains on |
| 25 | 1 | 0 | 0 | 1 | 1 | 0 | | | | | H | L | L | H | H | L | Program 9/Mains on |
| 26 | 0 | 1 | 0 | 1 | 1 | 0 | | | | | L | H | L | H | H | L | Program 10/Mains on |
| 27 | 1 | 1 | 0 | 1 | 1 | 0 | | | | | H | H | L | H | H | L | Program 11/Mains on |
| 28 | 0 | 0 | 1 | 1 | 1 | 0 | | | | | L | L | H | H | H | L | Program 12/Mains on |
| 29 | 1 | 0 | 1 | 1 | 1 | 0 | | | | | H | L | H | H | H | L | Program 13/Mains on |
| 30 | 0 | 1 | 1 | 1 | 1 | 0 | | | | | L | H | H | H | H | L | Program 14/Mains on |
| 31 | 1 | 1 | 1 | 1 | 1 | 0 | | | | | H | H | H | H | H | L | Program 15/Mains on |
| 32 | 0 | 0 | 0 | 0 | 0 | 1 | L | H | L | H | L | L | L | L | L | H | Volume +/Mute off |
| 33 | 1 | 0 | 0 | 0 | 0 | 1 | L | L | H | H | H | L | L | L | L | H | Volume − |
| 34 | 0 | 1 | 0 | 0 | 0 | 1 | H | L | L | H | L | H | L | L | L | H | Analogue 2 + |
| 35 | 1 | 1 | 0 | 0 | 0 | 1 | L | H | H | L | H | H | L | L | L | H | Analogue 2 − |
| 36 | 0 | 0 | 1 | 0 | 0 | 1 | H | L | H | L | L | L | H | L | L | H | Analogue 3 + |
| 37 | 1 | 0 | 1 | 0 | 0 | 1 | L | L | H | L | H | L | H | L | L | H | Analogue 3 − |
| 38 | 0 | 1 | 1 | 0 | 0 | 1 | L | H | L | L | L | H | H | L | L | H | Analogue 4 + |
| 39 | 1 | 1 | 1 | 0 | 0 | 1 | H | L | L | L | H | H | H | L | L | H | Analogue 4 − |
| 40 | 0 | 0 | 0 | 1 | 0 | 1 | | | | | L | L | L | H | L | H | |
| 41 | 1 | 0 | 0 | 1 | 0 | 1 | | | | | H | L | L | H | L | H | |
| 42 | 0 | 1 | 0 | 1 | 0 | 1 | | | | | L | H | L | H | L | H | |
| 43 | 1 | 1 | 0 | 1 | 0 | 1 | | | | | H | H | L | H | L | H | |
| 44 | 0 | 0 | 1 | 1 | 0 | 1 | | | | | L | L | H | H | L | H | |
| 45 | 1 | 0 | 1 | 1 | 0 | 1 | | | | | H | L | H | H | L | H | |
| 46 | 0 | 1 | 1 | 1 | 0 | 1 | | | | | L | H | H | H | L | H | |
| 47 | 1 | 1 | 1 | 1 | 0 | 1 | | | | | H | H | H | H | L | H | |
| 48 | 0 | 0 | 0 | 0 | 1 | 1 | | | | | L | L | L | L | H | H | |
| 49 | 1 | 0 | 0 | 0 | 1 | 1 | | | | | H | L | L | L | H | H | |
| 50 | 0 | 1 | 0 | 0 | 1 | 1 | | | | | L | H | L | L | H | H | |
| 51 | 1 | 1 | 0 | 0 | 1 | 1 | | | | | H | H | L | L | H | H | |
| 52 | 0 | 0 | 1 | 0 | 1 | 1 | | | | | L | L | H | L | H | H | |
| 53 | 1 | 0 | 1 | 0 | 1 | 1 | | | | | H | L | H | L | H | H | |
| 54 | 0 | 1 | 1 | 0 | 1 | 1 | | | | | L | H | H | L | H | H | |
| 55 | 1 | 1 | 1 | 0 | 1 | 1 | | | | | H | H | H | L | H | H | |
| 56 | 0 | 0 | 0 | 1 | 1 | 1 | | | | | L | L | L | H | H | H | Subsystem mode on |
| 57 | 1 | 0 | 0 | 1 | 1 | 1 | | | | | H | L | L | H | H | H | Subsystem mode on |
| 58 | 0 | 1 | 0 | 1 | 1 | 1 | | | | | L | H | L | H | H | H | Subsystem mode on |
| 59 | 1 | 1 | 0 | 1 | 1 | 1 | | | | | H | H | L | H | H | H | Subsystem mode on (pin 4 L) |
| 60 | 0 | 0 | 1 | 1 | 1 | 1 | | | | | L | L | H | H | H | H | Subsystem mode on |
| 61 | 1 | 0 | 1 | 1 | 1 | 1 | | | | | H | L | H | H | H | H | Subsystem mode on |
| 62 | 0 | 1 | 1 | 1 | 1 | 1 | | | | | L | H | H | H | H | H | Subsystem mode on |
| 63 | 1 | 1 | 1 | 1 | 1 | 1 | | | | | H | H | H | H | H | H | Subsystem mode off (pin 4 H) |

Note : All the program and shift commands (13, 14) are blocked when one of the commands from 56 to 62 is issued. This condition is reset by commands 2, 12 and 63.

## TYPICAL APPLICATION

Remote controlled voltage synthesizer (up to 32 stations) for TV and Radio.




**Note:** For 16 program display, M192 can be used in place of TDA4092.

## PCM REMOTE CONTROL RECEIVER

- 5—BIT BINARY STATIC OUTPUTS (UP TO 32 PROGRAMS)
- 4 ANALOGUE CONTROLS/63 STEPS
- 445 TO 510 kHz REFERENCE OSCILLATOR
- 5V SUPPLY VOLTAGE
- LOCAL CONTROLS AVAILABLE
- INTEGRATED DIGITAL POWER ON RESET
- TO BE USED IN CONJUNCTION WITH M709 OR M710 R.C. TRANSMITTERS (FLASH TRANSMISSION MODE)
- TECNICAL NOTE TN 155 AVAILABLE

The M105 is a simplified version of the M104 (no serial data bus is provided) and it has been developed for remote control of TV or radio sets in conjunction with M709/M710 R.C. transmitters. The receiver decodes the transmitted commands only if the transmitted address matches the address code selected at the receiver. 2 addresses are available for this purpose.

The frequency of the clock oscillator can be in the range 445 to 510 kHz and no synchronization is required with the transmitter clock.

The M105 is produced with N-channel silicon gate technology and is assembled in a 24 pin dual in-line plastic package.

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | −0.3 to 7 | V |
| $V_I$ | Input voltage (except pin 2) | −0.3 to 7 | V |
| | Input voltage pin 2 | −0.3 to 14 | V |
| $V_{O(off)}$ | Off-state output voltage (pins 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24) | 14 | V |
| | Off-state output voltage (pins 8, 9, 13) | 7 | V |

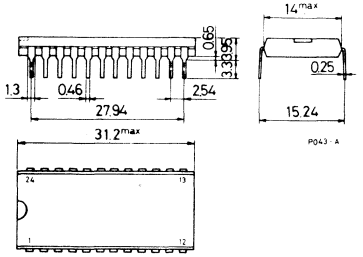
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ORDERING NUMBER:** M105 B1

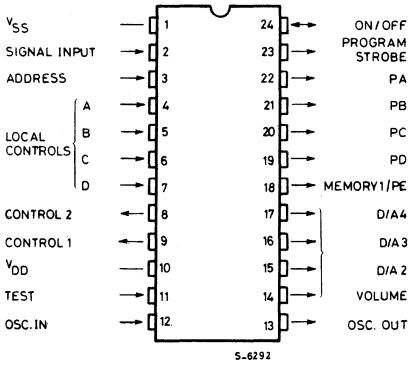
# M105

## MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package

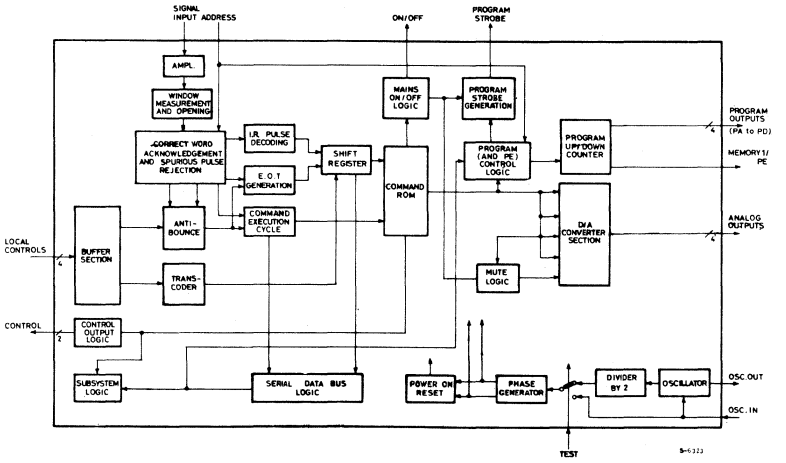



## PIN CONNECTIONS




NOTE: THE TEST PIN MUST BE CONNECTED TO $V_{SS}$

## BLOCK DIAGRAM




## RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | 4.75 to 5.25 | V |
| $V_I$ | Input voltage (except pin 2) | 0 to 5.25 | V |
| | Input voltage pin 2 | 0 to 13.2 | V |
| $V_{O(off)}$ | Off-state output voltage (pins 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24) | max 13.2 | V |
| | Off-state output voltage (pins 8, 9, 13) | max 5.5 | V |

Note: Test pin and unused open drain outputs must be connected to $V_{SS}$.

**STATIC ELECTRICAL CHARACTERISTICS** (over recommended operating conditions)
Typical values are at 5V, $T_{amb} = 25°C$

| Parameter | | Pins | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{IL}$ | Input low voltage | 3 - 24 | | | | 0.8 | V |
| | | 4 - 5 - 6 - 7 | | | | 1.5 | |
| $V_{IH}$ | Input high voltage | 3 - 24 | | 2.5 | | | V |
| | | 4 - 5 - 6 - 7 | | 4 | | | |
| $V_{IPP}$ | Peak to peak voltage | 2 | | 0.5 | | 13.2 | V |
| $V_{OL}$ | Output low voltage | 8 - 9 - 14 - 15<br>16 - 17 - 18 - 19<br>20 - 21 - 22 - 24 | $V_{DD} = 4.75V$<br>$I_{OL} = 1.6$ mA | | | 0.4 | V |
| | | 23 | $V_{DD} = 4.75V$<br>$I_{OL} = 1.6$ mA | | | 0.4 | |
| $I_{IL}$ | input low current | 3 - 4 - 5 - 6 - 7 | $V_{DD} = 5.25V$<br>$V_{IL} = 0.4V$ | | | −0.4 | mA |
| $I_{IH}$ | Input high current | 3 - 24 | $V_{DD} = 5.25V$<br>$V_{IH} = 5.25V$ | | | 25 | μA |
| $I_{O(off)}$ | Output leakage current | 14 - 15 - 16 - 17<br>18 - 19 - 20 - 21<br>22 - 23 - 24 | $V_{DD} = 5.25V$<br>$V_{O(off)} = 13.2V$ | | | 50 | μA |
| | | 8 - 9 | $V_{DD} = 5.25V$<br>$V_{O(off)} = 5.25V$ | | | 25 | |
| $I_{DD}$ | Supply current | 10 | $V_{DD} = 5.25V$<br>all outputs open | | | 50 | mA |

## DESCRIPTION

### Pin 1 — $V_{SS}$

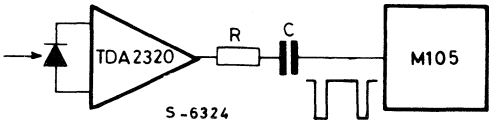
The substrate of the ICs is connected to this pin. It is the reference pin for all parameters of the ICs.

### Pin 2 — Signal input

The minimum signal to be applied is 0.5V peak to peak.
The receiver input section performs the folowing tests on the incoming signal to achieve the necessary noise immunity:

- measurement of the pulse distance (time base synchronization)
- check of the position of the received bits opening window at the time bases
- check of the parity bit
- check of the absence of pulses between the parity bit and the stop-pulse
- check of noise level; the receiver checks parasitic transient inside and outside the time windows.

If the above test conditions are not fulfilled, the received word is rejected and not decoded. If the received signal is acknowledged as a valid word it is stored and decoded. The received coded word is also released on the serial data bus.
The ned of transmission will be acknowledged by receiving the end of transmission code or by means of an internal timer if the transmission remains interrupted for more than about 550 ms.




| SUPPLY VOLTAGE OF TDA 2320 | R | C |
|---|---|---|
| 5 | 2.2K | 4.7 nF |
| 12 | 10K | 4.7 nF |

## Pin 3 — Address input

The receiver decodes only signals transmitted by M709/M710 with address 1 and 2. This input as an integrated pull-up resistor of 50 KΩ (max).

| Address | Pin 3 |
|---|---|
| 1 | Low |
| 2 | High |

## Pins 4-5-6-7 — Local control inputs LOC-A, LOC-B, LOC-C, LOC-D (see table 1)

These inputs are provided for emergency operations. Therefore only a few controls are provided.
Local input commands and I.R. commands have the same priority.
If a complete I.R. command has been received, the local inputs are blocked until the commands has been executed and the "end of transmission code" generated.
Viceversa an I.R. signal cannot be decoded until an issued local command has been executed and the "end of transmission" released.
All these inputs have integrated pull-up resistor of 50 KΩ (max).
Each command is accepted after it has been present continuosly for about 40 ms.

## Pins 8-9 — Control output R2, R1

These outputs consist of open drain transistors that are switched on when commands 6 and 7 are issued. The outputs remain switched on for a time variable between 144 and 173 ms after reception of the command ($f_{ref}$ = 500 kHz). They can be used for example to control fine tuning or automatic search commands of M293 (Electronic Program Memory).

| Command N° | R1 (pin 9) | R2 (pin 8) |
|---|---|---|
| 6 | L | H |
| 7 | H | L |

Table 1

| Inputs | | | | Function |
|---|---|---|---|---|
| A | B | C | D | |
| H | H | H | H | |
| L | H | H | H | Program + |
| H | L | H | H | Program – |
| L | L | H | H | Volume – |
| H | H | L | H | |
| L | H | L | H | Volume + |
| H | L | L | H | A 2 + |
| L | L | L | H | Normalization |
| H | H | H | L | Memory 1 H |
| L | H | H | L | A 2 – |
| H | L | H | L | A 3 + |
| L | L | H | L | A 3 – |
| H | H | L | L | Memory 1L |
| L | H | L | L | A 4 + |
| H | L | L | L | A 4 – |
| L | L | L | L | Mains off |

### Pin 10 – $V_{DD}$

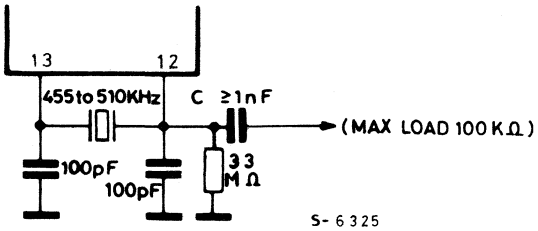
The supply voltage has to be 5V $\pm$ 5%.

### Pin 11 – test

This pin is used for testing and has to be connected to $V_{SS}$.

### Pins 12-13 – Clock oscillator

The frequency of the clock oscillator should be between 445 and 510 kHz using a cheap ceramic resonator. In these conditions the value of the reference frequency of the transmitter can be in the same range. In other words the transmitter and the receiver can operate with different reference frequencies.
The clock signal can be used to drive the clock of other ICs through a capacitor connected at pin 12.



### Pins 14 to 17 — Analogue control outputs

These outputs are provided to control four analogue values (for example volume, brightness, colour saturation and contrast in TV sets).
The outputs deliver square wave signals of 7.8 kHz with a duty cycle variable in 63 steps.
In the case of a continuous command for varying the analogue information, the duty cycle is changed at the rate of the transmitted signal (approximately every 102 ms with $f_{ref} = 500kHz$).
Local controls are varied every 115 ms ($f_{ref} = 500$ kHz).
The circuits is provided with underflow and overflow protection.
At supply on reset the volume output (pin 4) is set at duty cycle 21/64 (pulse = H). All other outputs are set at 31/64.
The normalization command sets all the outputs except volume to mid position (31/64).
The volume output can be switched to $V_{SS}$ and reset to the previous level by means of command 2 (mute).
It is also reset by means of the normalization command, volume + and mains off command.
The volume output is muted at each mains on and off command for approximately 0.5 sec.
It is also muted at supply on/off. The analogue outputs cannot be modified in the standby condition (mains off).

### Pin 18 — Memory 1 (PE)

This output can be used as shift command for selection of up to 32 programs.
The output is set at power on to a low level. It can be controlled using commands 13 and 14. In the case of program +/— commands the output is automatically switched if the receiver operates with the address 1 (pin 3 = L).
Otherwise this output is not affected by the program +/— commands and can be used for general applications. It has open drain configuration.

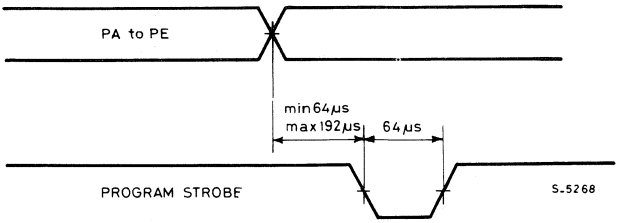
### Pins 19-20-21-22 — PD, PC, PB, PA Program outputs

Open drain, binary coded, static outputs. At power on reset the outputs are set to program 1 (PA to PD = L L L L).
The program selection can be sequential or direct. If the TV set is in the standby condition the program step-by-step ± commands (8, 9) or the direct program selection commands (16 to 31) can be used to switch on the set.
In the first case the program can be stepped only if the command has been interrupted and a continuous sequential program change command causes program stepping in the up or down direction every 0.57 sec. (every 0.5 sec. if issued from R.C. transmitter).
Direct program selection is possible only by remote control.
The selection of up to 32 programs is possible using the memory 1 output (pin 18) that is put low and high by transmitting the comands 13 and 14 respectively.

**Note:** All the program and shift commands are blocked when one of the commands from 56 to 62 is issued. This condition is reset by commands 2, 12 and 63.

## Pin 23 — Program strobe output

The program strobe signal is generated each time the content of the memory has to be read and each time the mains output is switched off or on. It is therefore generated at direct program selection (16 to 31), program ± stepping (8, 9) and shift commands (13, 14) with address 1.




At direct program selection and shift commands, the strobe is available only once.
This output has open drain configuration.

**Note:** The strobe signal is not available when the M105 is in the subsystem mode; the output has open drain configuration.

## Pin 24 — Mains on/off

This active low output, is provided to control the on/off switching of the TV set via a transistor and a relay.
When the supply voltage is applied to the device, the output transistor is automatically biased off.
In this "standby" condition, only the mains on commands are accepted.
A mains on command can be given in one of the following ways:

a) — by commands 8, 9 (program + / —)
— by command 12
— by commands 16 to 31

All these commands are accepted only when received 5 times (about 0.4 sec).
The "end of transmission" code resets the associated counter.
b) — connecting pin 24 to $V_{SS}$ (GND) for at least 10 µs.

This feature is provided for automatic switch on of the set using a temporarily active slide contact in parallel with the master power on switch.
The command is accepted only when the supply voltage $V_{DD}$ has risen above approximately 4V.
The set can be put in standby by means of command 2. This commands also has to be received 5 times.

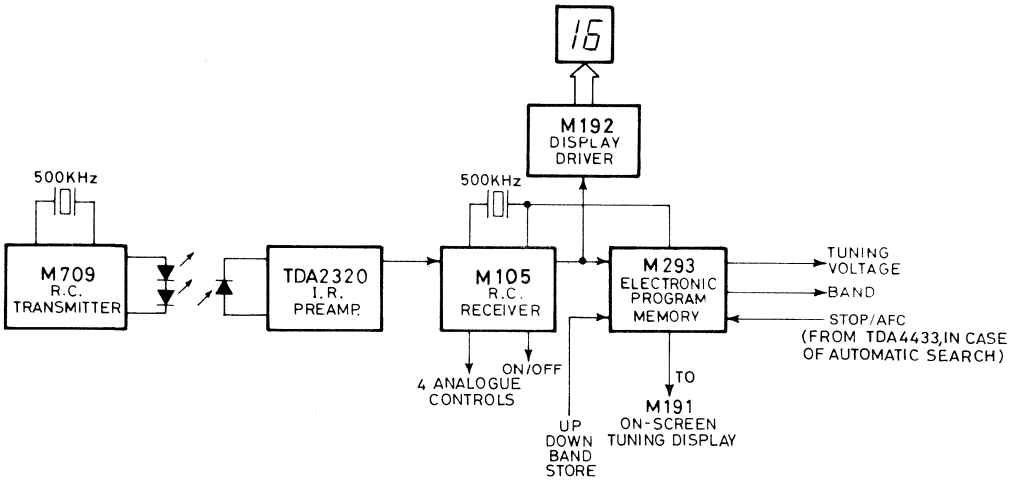
## M105 truth table

| Command No. | I.R. code C1 | C2 | C3 | C4 | C5 | C6 | Local controls A | B | C | D | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | End of transmission. |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | | | | | Mute on/off |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | L | L | L | L | Mains off/Mute off/ |
| 3 | 1 | 1 | 0 | 0 | 0 | 0 | | | | | |
| 4 | 0 | 0 | 1 | 0 | 0 | 0 | | | | | |
| 5 | 1 | 0 | 1 | 0 | 0 | 0 | | | | | |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | | | | | Control 1 L |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | | | | | Control 2 L |
| 8 | 0 | 0 | 0 | 1 | 0 | 0 | L | H | H | H | Program +/Mains on |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | H | L | H | H | Program −/Mains on |
| 10 | 0 | 1 | 0 | 1 | 0 | 0 | L | L | L | H | Normalization/Mute off |
| 11 | 1 | 1 | 0 | 1 | 0 | 0 | | | | | |
| 12 | 0 | 0 | 1 | 1 | 0 | 0 | | | | | Mains on |
| 13 | 1 | 0 | 1 | 1 | 0 | 0 | H | H | L | L | Memory 1 L |
| 14 | 0 | 1 | 1 | 1 | 0 | 0 | H | H | H | L | Memory 1 H |
| 15 | 1 | 1 | 1 | 1 | 0 | 0 | | | | | |
| 16 | 0 | 0 | 0 | 0 | 1 | 0 | | | | | Program 16/Mains on |
| 17 | 1 | 0 | 0 | 0 | 1 | 0 | | | | | Program 1/Mains on |
| 18 | 0 | 1 | 0 | 0 | 1 | 0 | | | | | Program 2/Mains on |
| 19 | 1 | 1 | 0 | 0 | 1 | 0 | | | | | Program 3/Mains on |
| 20 | 0 | 0 | 1 | 0 | 1 | 0 | | | | | Program 4/Mains on |
| 21 | 1 | 0 | 1 | 0 | 1 | 0 | | | | | Program 5/Mains on |
| 22 | 0 | 1 | 1 | 0 | 1 | 0 | | | | | Program 6/Mains on |
| 23 | 1 | 1 | 1 | 0 | 1 | 0 | | | | | Program 7/Mains on |
| 24 | 0 | 0 | 0 | 1 | 1 | 0 | | | | | Program 8/Mains on |
| 25 | 1 | 0 | 0 | 1 | 1 | 0 | | | | | Program 9/Mains on |
| 26 | 0 | 1 | 0 | 1 | 1 | 0 | | | | | Program 10/Mains on |
| 27 | 1 | 1 | 0 | 1 | 1 | 0 | | | | | Program 11/Mains on |
| 28 | 0 | 0 | 1 | 1 | 1 | 0 | | | | | Program 12/Mains on |
| 29 | 1 | 0 | 1 | 1 | 1 | 0 | | | | | Program 13/Mains on |
| 30 | 0 | 1 | 1 | 1 | 1 | 0 | | | | | Program 14/Mains on |
| 31 | 1 | 1 | 1 | 1 | 1 | 0 | | | | | Program 15/Mains on |
| 32 | 0 | 0 | 0 | 0 | 0 | 1 | L | H | L | H | Volume +/Mute off |
| 33 | 1 | 0 | 0 | 0 | 0 | 1 | L | L | H | H | Volume − |
| 34 | 0 | 1 | 0 | 0 | 0 | 1 | H | L | L | H | Analogue 2 + |
| 35 | 1 | 1 | 0 | 0 | 0 | 1 | L | H | H | L | Analogue 2 − |
| 36 | 0 | 0 | 1 | 0 | 0 | 1 | H | L | H | L | Analogue 3 + |
| 37 | 1 | 0 | 1 | 0 | 0 | 1 | L | L | H | L | Analogue 3 − |
| 38 | 0 | 1 | 1 | 0 | 0 | 1 | L | H | L | L | Analogue 4 + |
| 39 | 1 | 1 | 1 | 0 | 0 | 1 | H | L | L | L | Analogue 4 − |
| 40 | 0 | 0 | 0 | 1 | 0 | 1 | | | | | |
| 41 | 1 | 0 | 0 | 1 | 0 | 1 | | | | | |
| 42 | 0 | 1 | 0 | 1 | 0 | 1 | | | | | |
| 43 | 1 | 1 | 0 | 1 | 0 | 1 | | | | | |
| 44 | 0 | 0 | 1 | 1 | 0 | 1 | | | | | |
| 45 | 1 | 0 | 1 | 1 | 0 | 1 | | | | | |
| 46 | 0 | 1 | 1 | 1 | 0 | 1 | | | | | |
| 47 | 1 | 1 | 1 | 1 | 0 | 1 | | | | | |
| 48 | 0 | 0 | 0 | 0 | 1 | 1 | | | | | |
| 49 | 1 | 0 | 0 | 0 | 1 | 1 | | | | | |
| 50 | 0 | 1 | 0 | 0 | 1 | 1 | | | | | |
| 51 | 1 | 1 | 0 | 0 | 1 | 1 | | | | | |
| 52 | 0 | 0 | 1 | 0 | 1 | 1 | | | | | |
| 53 | 1 | 0 | 1 | 0 | 1 | 1 | | | | | |
| 54 | 0 | 1 | 1 | 0 | 1 | 1 | | | | | |
| 55 | 1 | 1 | 1 | 0 | 1 | 1 | | | | | |
| 56 | 0 | 0 | 0 | 1 | 1 | 1 | | | | | |
| 57 | 1 | 0 | 0 | 1 | 1 | 1 | | | | | |
| 58 | 0 | 1 | 0 | 1 | 1 | 1 | | | | | |
| 59 | 1 | 1 | 0 | 1 | 1 | 1 | | | | | |
| 60 | 0 | 0 | 1 | 1 | 1 | 1 | | | | | |
| 61 | 1 | 0 | 1 | 1 | 1 | 1 | | | | | |
| 62 | 0 | 1 | 1 | 1 | 1 | 1 | | | | | |
| 63 | 1 | 1 | 1 | 1 | 1 | 1 | | | | | |

Note : All the program and shift commands (13, 14) are blocked when one of the commands from 56 to 62 is issued. This condition is reset by commands 2, 12 and 63.

## TYPICAL APPLICATION

Remote controlled voltage synthesizer for TV.




S-6326

**Note:** For 32 program display, TDA4092 can be used in place of M192.

## 16 KEY KEYBOARD ENCODER AND LATCH

- ANTIBOUNCE AND ANTINOISE CIRCUITRY
- INTERLOCK PREVENTS INCORRECT SELECTION
- OPERATES WITH SINGLE POLE PUSH-BUTTONS
- SELECTION OF PROGRAM 1 AT POWER ON
- MUTING OUTPUT AVAILABLE DURING PROGRAM CHANGES AND POWER SUPPLY SWITCHING
- STEP-BY-STEP PROGRAM CHANGE INPUT
- KEYBOARD LOCKING
- OUTPUTS DIRECTLY COMPATIBLE WITH M 193 (ELECTRONIC PROGRAM MEMORY), M 192 (7-SEGMENT DECODER DRIVER).

The M 190 is a monolithic integrated circuit which automatically scans an up to 16 Key keyboard, generating continuous sequential pulses on X outputs and detecting key closure on Y inputs.
A key closure is retained as valid when the key remains closed for all the time corresponding to one scan pulse (i.e. when the bounce is over).
When it occurs an internal flip-flop is set but the key closure is accepted only if it is detected on a second scan cycle. At this point a 4 bit word corresponding to the key closed is internally latched and a pulse is available on the Muting output.
During the time this pulse lasts, no other key closure will be recognized. The new output code follows the Mute signal with a delay.
All the timing for the circuits is determined by the clock oscillator whose frequency is externally fixed by an RC network.
The M 190 also includes a "step-by-step" program change input that, when connected to $V_{SS}$ (GND), advances by one the selected channel and a Lock which blocks the circuit on the last selected channel.
The circuit is produced in N-channel silicon gate technology and is available in a 18 pin dual in-line plastic package.

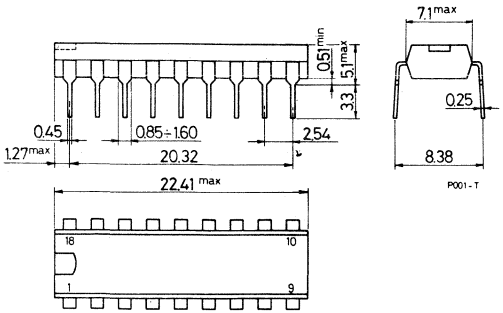
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.5 to 20 | V |
| $V_I$ | Input voltage | -0.5 to 20 | V |
| $V_{O(off)}$ | Off state output voltage (pins 1-2-3-4-11) | 20 | V |
| $I_O$ | Output current | \|5\| | mA |
| $P_{tot}$ | Total package power dissipation | 500 | mW |
| $T_{stg}$ | Storage temperature | -65 to 125 | °C |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

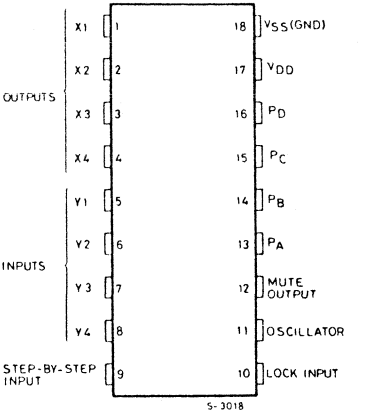
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ORDERING NUMBER:** M 190 B1

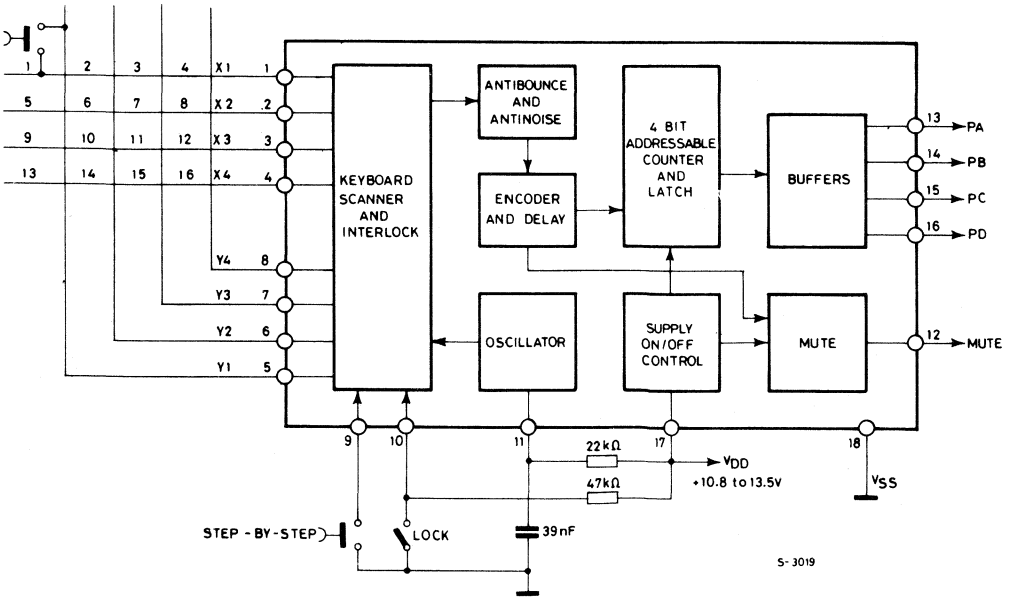
## MECHANICAL DATA (dimensions in mm)




## PIN CONNECTIONS




## BLOCK DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | 10.8 to 13.5 | V |
| $V_I$ | Input voltage | 0 to 13.5 | V |
| $V_{O(off)}$ | Off state output voltage (pins 1-2--3-4-11) | max 13.5 | V |
| $I_O$ | Output current | max \|2\| | mA |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |
| $R_t$ | Timing resistor | 8 to 47 | KΩ |
| $C_t$ | Timing capacitor | 1 to 330 | nF |

## STATIC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

| Parameter | | Test conditions | Values at 25°C | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{IH}$ | High level input voltage | pins 5, 6, 7, 8, 9, 10 | 3.5 | | | V |
| $V_{IL}$ | Low level input voltage | pins 5, 6, 7, 8, 9, 10 | | | 0.8 | V |
| $I_{IH}$ | High level input current | $V_{DD}$= 13.5V, $V_{IH}$= 13.5V pins 5, 6, 7, 8, 9, 10 | | | 10 | μA |
| $I_{IL}$ | Low level input current | $V_{DD}$= 13.5V, $V_{IL}$= 0.8V pins 5, 6, 7, 8, 9, 10 | 0.1 | | 0.8 | mA |
| $V_{OH}$ | High level output voltage | $V_{DD}$= 10.8V $I_{OH}$= -1 mA, pin 12 | 2.4 | | | V |
| | | $V_{DD}$= 10.8V $I_{OH}$= -1 mA, pins 13. 14, 15, 16 | 4 | | | |
| $V_{OL}$ | Low level output voltage | $V_{DD}$= 10.8V $I_{OL}$= 0.8 mA pins 1, 2, 3, 4, 11 | | | 0.4 | V |
| | | $V_{DD}$= 10.8V $I_{OL}$= 2 mA, pins 13, 14, 15, 16 | | | 0.4 | |
| $I_{O(off)}$ | Output leakage current | $V_{DD}$= $V_{O(off)}$= 13.5V, pins 1, 2, 3, 4, 11 | | | 20 | μA |
| $I_{DD}$ | Supply current | $V_{DD}$= 13.5V (all inputs and outputs open) | | | 18 | mA |

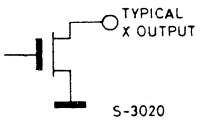
## TRUTH TABLE

| Key | Connection | Output code (positive logic) | | | |
|---|---|---|---|---|---|
| | | PA | PB | PC | PD |
| 1 | $X_1 - Y_1$ | L | L | L | L |
| 2 | $X_1 - Y_2$ | H | L | L | L |
| 3 | $X_1 - Y_3$ | L | H | L | L |
| 4 | $X_1 - Y_4$ | H | H | L | L |
| 5 | $X_2 - Y_1$ | L | L | H | L |
| 6 | $X_2 - Y_2$ | H | L | H | L |
| 7 | $X_2 - Y_3$ | L | H | H | L |
| 8 | $X_2 - Y_4$ | H | H | H | L |
| 9 | $X_3 - Y_1$ | L | L | L | H |
| 10 | $X_3 - Y_2$ | H | L | L | H |
| 11 | $X_3 - Y_3$ | L | H | L | H |
| 12 | $X_3 - Y_4$ | H | H | L | H |
| 13 | $X_4 - Y_1$ | L | L | H | H |
| 14 | $X_4 - Y_2$ | H | L | H | H |
| 15 | $X_4 - Y_3$ | L | H | H | H |
| 16 | $X_4 - Y_4$ | H | H | H | H |

## DESCRIPTION

### Pins 1, 2, 3, 4 - $X_1$, $X_2$, $X_3$, $X_4$ outputs

The internal open drain transistors on these outputs are sequentially switched on.

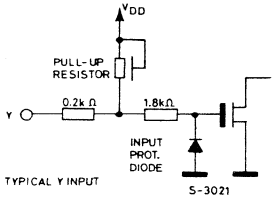



### Pins 5, 6, 7, 8 - $Y_1$, $Y_2$, $Y_3$, $Y_4$ inputs

These inputs correspond to the columns of the keyboard matrix. When a key is pushed, one of the X output signal is present on one of the 4 rows, putting a low level on the Y input.
An interlock circuit rejects more than one key pressed at the same time.
To increase the noise immunity of the system and to avoid bouncing problems, the key closure is considered valid only when it is present for all the time corresponding to the scan pulse. With this system spurious noise signals are also rejected.
Another increase in the noise immunity is given by detecting key closure over two consecutive scanning cycles.

## DESCRIPTION (continued)

After the key bounce time, the acceptance time of a command is between 35T and 63T, where T is the period of the clock pulse.
When any input is open it is pulled-up to logic H by an integrated MOS load of about 50 KΩ and protected by a diode.




### Pin 9 - Step-by-step program change

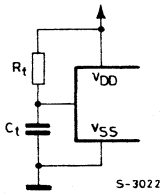
This input advances by one the previously selected channel every time ti is connedted to ground.
This input can be considered as a 17th key and follows all the rules of command acceptance time and partially of interlock.
The unput is pulled-up to logic H by an integrated resistor of about 50 KΩ ; if the input is not used, it should be connected to $V_{DD}$.

### Pin 10 - Lock

If this input is connected to $V_{SS}$ (GND) the circuit is locked on the selected channel.
If the input is not used, it must be connected to $V_{DD}$.

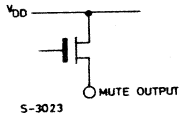
### Pin 11 - RC network (clock oscillator input)

An internal clock provides all the timing for the circuits.
The frequency of the clock oscillator is controlled by two external components, resistor $R_t$ and capacitor $C_t$.
The period of the clock pulse is approximately given by $T = R_tC_t$.
The oscillator works in the following way: assuming the capacitor $C_t$ is discharged, the resistor $R_t$ charges the capacitor till an internal threshold is reached. At this point the capacitor is discharged by an internal transistor.
Afterwards the internal transistor is switched off and the cycle can restart.
With $R_t$= 22 KΩ and $C_t$= 39 nF a clock frequency of about 800 Hz is obtained, corresponding to a scan cycle of the keyboard of about 40 ms.
In these conditions the mute signal will be present for about 100 ms before the program changing and will last 300 ms.

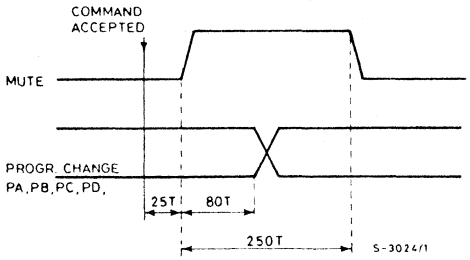


## Pin 12 - Mute

The mute signal is available as a high level output (source follower transistor).
It is present during power ON/OFF and program changes.



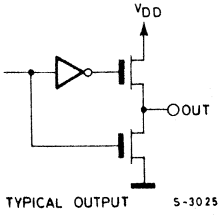

When a command is given the Mute signal and the program information are available in the following way:




The Mute signal is not available when the same program is selected again.

## Pins 13, 14, 15, 16 - PA, PB, PC, PD outputs

These static outputs select the program according to the truth table.
They interface directly with the inputs of M 193 (Electronic Program Memory), M 192 (7 segment Decoder/Driver), H 770/1/2/3 (Quad Analog Switches).
The program 1 is internally selected at power ON.



## 4-BIT BINARY 7-SEGMENT DECODER DRIVER

- 4-BIT BINARY CODE INPUT GENERATES 1 TO 16 NUMBERS ON OUTPUT
- DIRECT DRIVING OF 1 AND 1/2 DIGIT 7-SEGMENT (COMMON CATHODE) LED DISPLAY
- WIDE SUPPLY VOLTAGE RANGE
- TTL COMPATIBLE INPUTS
- SMALL QUIESCENT SUPPLY CURRENT
- SPECIFICALLY DESIGNED FOR TV OR RADIO APPLICATIONS

The M 192 is a monolithic integrated circuit which direct drives a 1 and 1/2 digit 7-segment LED (communicathode) display to present the numbers 1 to 16. The inputs accept a 4-bit binary code having TTL levels. This device is especially designed to show the program number in TV or radio sets in conjunction with M 190 keyboard encoder, M 104, M 105 remore control receives, M 193 or M 293 electronic program memory. All outputs are designed to supply and sink current, except the additional "r" output (pin 1) which is designed for a brightness control in a current generator configurations. The circuit is produced in CMOS tecnology and is supplied in a 16-pin dual in-line plastic package.

## ABSOLUTE MAXIMUM RATINGS

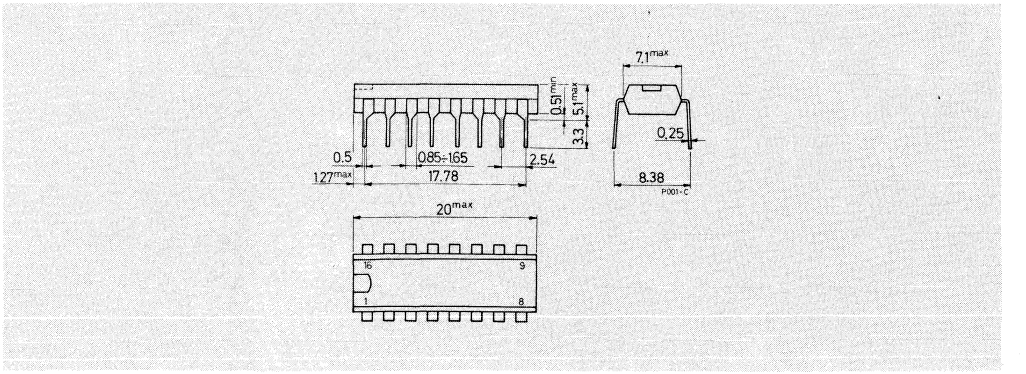
| | | | | |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.5 to | 16.5 | V |
| $V_I$ | Input voltage | -0.5 to $V_{DD}$ | +0.5 | V |
| $V_O$ | Output voltage (pin 1) | | $V_{DD}$ +0.5 | V |
| $I_{OH}$ | Output source current | | -25 | mA |
| $I_{OL}$ | Output sink current (except pin 1) | | 10 | mA |
| $P_{tot}$ | Total package power dissipation | | 400 | mW |
| $T_{stg}$ | Storage temperature | -65 to | 150 | °C |
| $T_{op}$ | Operating temperature | 0 to | 70 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

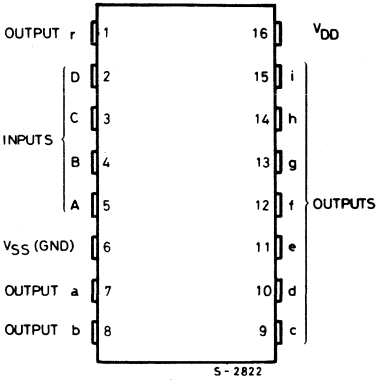
**ORDERING NUMBER:** M 192 B1

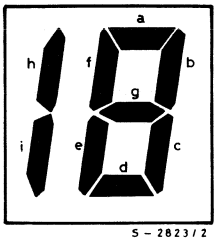
## MECHANICAL DATA

Dimensions in mm



## PIN CONNECTIONS

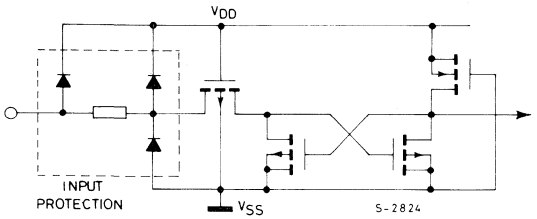


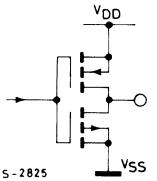

## TRUTH TABLE

| INPUTS | | | | Number displayed | OUTPUTS | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | | a | b | c | d | e | f | g | h | i | r |
| L | L | L | L | 1 | L | H | H | L | L | L | L | L | L | H |
| H | L | L | L | 2 | H | H | L | H | H | L | H | L | L | H |
| L | H | L | L | 3 | H | H | H | H | L | L | H | L | L | H |
| H | H | L | L | 4 | L | H | H | L | L | H | H | L | L | H |
| L | L | H | L | 5 | H | L | H | H | L | H | H | L | L | H |
| H | L | H | L | 6 | H | L | H | H | H | H | H | L | L | H |
| L | H | H | L | 7 | H | H | H | L | L | L | L | L | L | H |
| H | H | H | L | 8 | H | H | H | H | H | H | H | L | L | H |
| L | L | L | H | 9 | H | H | H | H | L | H | H | L | L | H |
| H | L | L | H | 10 | H | H | H | H | H | H | L | H | H | H |
| L | H | L | H | 11 | L | H | H | L | L | L | L | H | H | H |
| H | H | L | H | 12 | H | H | L | H | H | L | H | H | H | H |
| L | L | H | H | 13 | H | H | H | H | L | L | H | H | H | H |
| H | L | H | H | 14 | L | H | H | L | L | H | H | H | H | H |
| L | H | H | H | 15 | H | L | H | H | L | H | H | H | H | H |
| H | H | H | H | 16 | H | L | H | H | H | H | H | H | H | H |

## INPUT CONFIGURATION




## OUTPUT CONFIGURATION



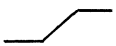

Note: pin 1 has not the pull down N-channel transistor.

## RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | 10.8 to 15 | V |
| $V_I$ | Input voltage | 0 to $V_{DD}$ | V |
| $V_O$ | Output voltage (pin 1) | $V_{DD}$ | V |
| $I_{OH}$ | Output source current | max -10 | mA |
| $I_{OL}$ | Output sink current | max 0.5 | mA |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

## ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

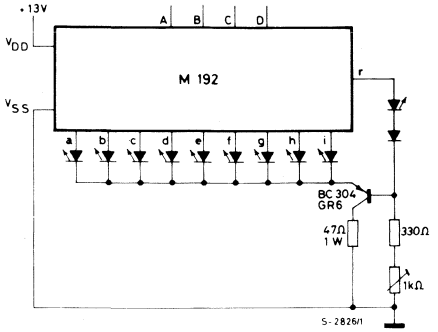
typical values are at $T_{amb}$= 25°C unless otherwise specified

| Parameter | | Test conditions | | Values | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{IH}$ | High level input voltage | | | 3.5 | | $V_{DD}$ | V |
| $V_{IL}$ | Low level input voltage | | | 0 | | 0.8 | V |
| $I_{IH}$ | High level input current | $V_{DD}$= 15V | $V_{IH}$= 15V | | | 10 | μA |
| $I_{T+}$ | Input current at positive threshold | $V_{DD}$= 15V |  | | | 200 | μA |
| $V_{OH}$ | High level output voltage | $I_{OH}$= -10 mA | $V_{DD}$= 10.8V<br>$V_{DD}$= 13V<br>$V_{DD}$= 13V, $T_{amb}$= 70°C<br>$V_{DD}$= 15V | $V_{DD}$ -3 | $V_{DD}$-3<br>$V_{DD}$-2<br>$V_{DD}$-2.5<br>$V_{DD}$-1.5 | | V<br>V<br>V<br>V |
| $V_{OL}$ | Low level output voltage (except pin 1) | $V_{DD}$= 13V | $I_{OL}$= 0.5 mA | | 1 | 1.5 | V |
| $I_{DD}$ | Supply current<br>Input to $V_{DD}$<br>Outputs open | $V_{DD}$= 15V | | | 2 | 2,4 | mA |

## APPLICATION INFORMATION

Fig. 1 - Light emitting diode readout

a - Current generator configuration




b - Standard configuration

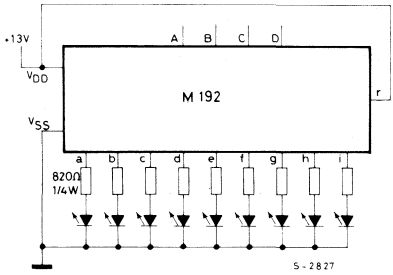



Fig. 2 - Liquid crystal readout

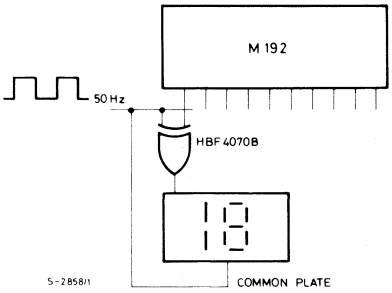



Fig. 3 - Fluorescent readout

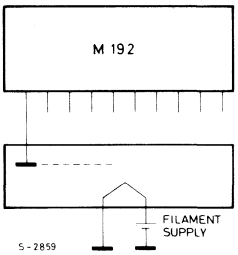



Fig. 4 - Incandescent redout

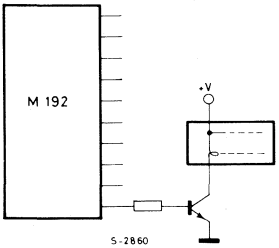
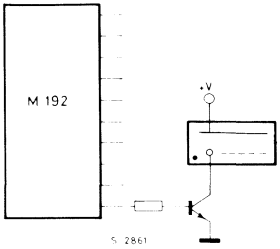



Fig. 5 - Gas discarge readout



**NOT FOR NEW DESIGNS**

## EPM 16-ELECTRONIC PROGRAM MEMORY (16 STATIONS)

- ONE CHIP SOLUTION INCLUDING CONTROL AND NON VOLAT. MEMORY FOR 16 PROGR.
- 10 YEARS MEMORY RETENTION
- UNLIMITED NUMBERS OF READ CYCLES
- AUTOMATIC AND MANUAL STATION SEARCH
- EXTERNALLY ADJUSTABLE SEARCH SPEED
- FINE TUNING IN 8 STEPS, STORABLE FOR EACH PROGRAM SEPARATELY
- MUTE OUTPUT
- 4.43 MHz QUARTZ REFERENCE FREQUENCY

The M193 is a monolithic integrated circuit constructed in N-channel silicon gate technology, designed to control digitally via a D/A converter, with a resolution of 8192 steps, a TV or Radio varicap tuner. A 17 bit x 16 words NVRAM is also integrated in the chip. Each memory word contains information for 1 program, i.e. band (2 bit), tuning voltage (12 bit) and fine tuning offset (3 bit). The circuit is able to operate either in automatic or manual search. The search speed is externally controlled by a simple RC network. In the automatic mode the M193 works in conjunction with the TDA 4431, which provides TV station recognition and converts the AFC-S-curve into a digital command. This command controls the 13 bit up/down counter in the M193, whose position determines the tuning voltage. A mute output is provided to avoid noise on the audio during automatic search, program change or when the supply voltage is switched on/off. The circuit accepts standard program selection on 4 bus lines. 7-segment program display is possible using the M192 circuit connected at the same lines. A serial information output is provided to display on the screen, via the M191 integrated circuit, the varicap voltage in the form of a linear tuning bar and the band. The M193 is available in a 28 lead dual in-line plastic package. Three different types are available which differ as specified below.
M193A - The automatic search is implemented with two commands which provide to scan the bands I + UHF and III + S respectively.
M193C - The search, either automatic or manual, is done only in the selected band. The band can be changed with a separate step-by-step command.
M193D - Same search function characteristics of the C type. The only difference consists in the threshold of discrimination of pulses applied at pin 4 (fine tuning from remote control). This version interfaces with the "T" output of the SAA 1251 remote control receiver.

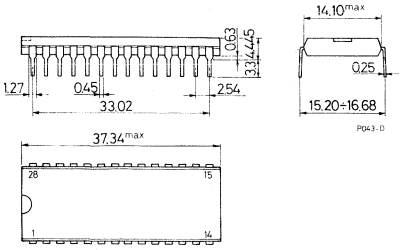
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD1}$, $V_{DD2}$ | Supply voltages | -0.3 to 20 | V |
| $V_{PP}$ | Memory supply voltage (pin 9) | -0.3 to 31 | V |
| $V_I$ | Input voltage | -0.3 to 20 | V |
| $V_{O\,(off)}$ | Off-state output voltage (except pin 14) | 20 | V |
| | (pin 14) | 31 | V |
| $I_{OL}$ | Output current (except pins 15-19) | 5 | mA |
| | (pins 15-19) | 15 | mA |
| $I_{OH}$ | Output current (pin 27) | -5 | mA |
| $P_{tot}$ | Total package power dissipation | 1 | W |
| $T_{stg}$ | Storage temperature | -25 to 125 | °C |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

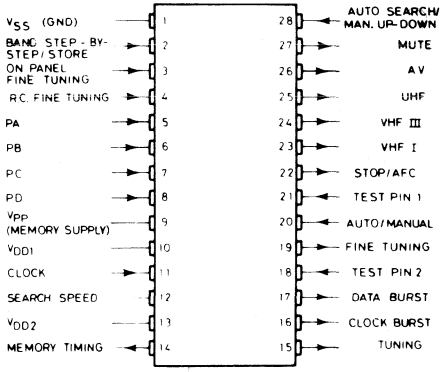
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ORDERING NUMBERS:** M193A B1
M193C B1
M193D B1

## MECHANICAL DATA (dimensions in mm)




## PIN CONNECTIONS




NOTE : TEST PINS must be connected to $V_{SS}$ (GND)

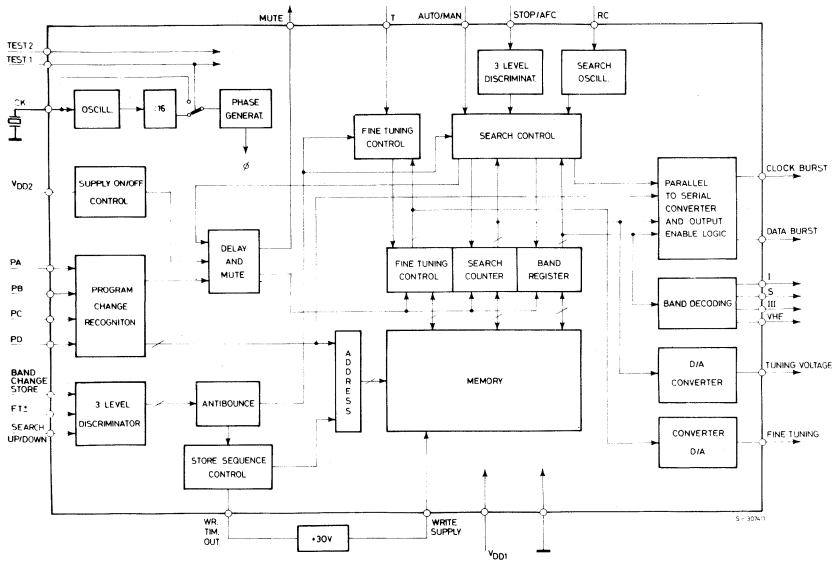
5-3215/1

## RECOMMENDED OPERATING CONDITIONS

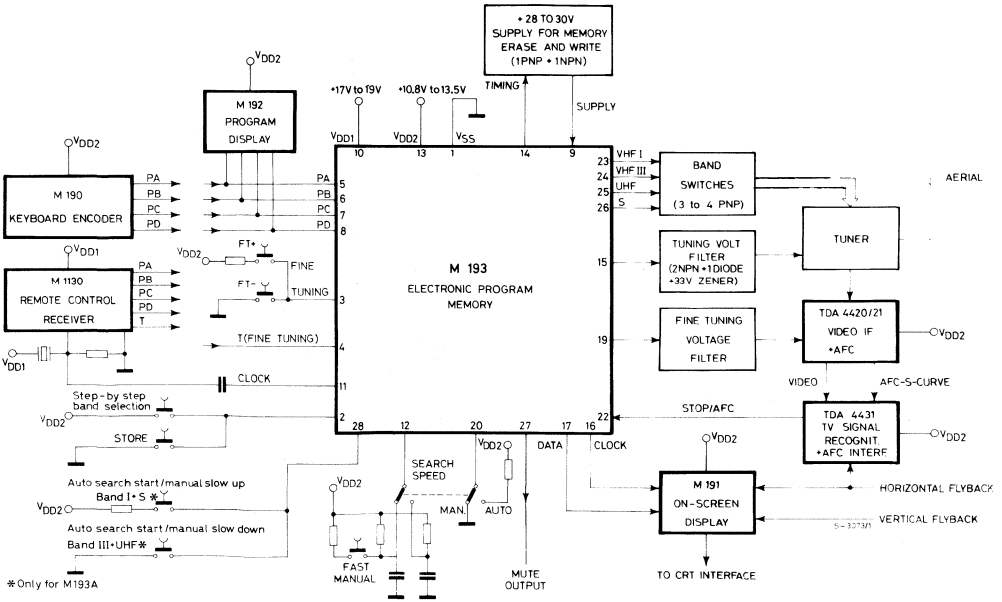
| | | | | |
|---|---|---|---|---|
| $V_{DD1}$ | Supply voltage | | 17 to 19 | V |
| $V_{DD2}$ | Supply voltage | | 10.8 to 13.5 | V |
| $V_{PP}$ | Memory supply voltage (pin 9) | | 28 to 30 | V |
| $V_I$ | Input voltage | | 0 to 19 | V |
| $V_{O(off)}$ | Off-state output voltage (except pin 14) | | max. 19 | V |
| | Off-state output voltage (pin 14) | | max. 30 | V |
| $I_{OL}$ | Output current (except 15--19) | | max. 2.5 | mA |
| | (pins 15-19) | | max. 10 | mA |
| $I_{OH}$ | Output current (pin 27) | | max. -2.5 | mA |
| $t_{pd}$ | Delay between memory timing and memory supply pulses | | max. 5 | $\mu$s |
| $f$ | Clock frequency | | 4.4 | MHz |
| $R_s$ | Serial resistance of the quartz | | max. 50 | $\Omega$ |
| $C_d$ | Dynamic capacitance of the quartz | | max. 20 | fF |
| $C_p$ | Total parallel capacitance of the quartz | | max. 8 | pF |
| $R_p$ | Total parallel resistance of the quartz | | min. 10 | M$\Omega$ |
| $t_{w1}$ | Fine tuning + pulse width (pin 4) | M193A, C | > 1.8 | ms |
| | | M193D | > 120 | $\mu$s |
| $t_{w2}$ | Fine tuning - pulse width (pin 4) | M193A, C | < 1.7 | ms |
| | | M193D | < 80 | $\mu$s |
| $T_{op}$ | Operating temperature | | 0 to 70 | °C |
| $R_{12}$ | Search speed resistance (pin 12) | | 18 to 330 | K$\Omega$ |
| $C_{12}$ | Search speed capacitor (pin 12) | | max. 100 | nF |

Notes: 1) The oscillator of the M193 cannot be used to drive external circuits.
2) See the "General information" at the end of this data as far as the power-on supply sequence is concerned.

## BLOCK DIAGRAM




## EPM SYSTEM CONFIGURATION



## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at $T_{amb}$= 25°C, $V_{DD1}$= 18V, $V_{DD2}$= 12V unless otherwise specified

| Parameter | | Pins | Test conditions | | | Values | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Typ. | Max. | |
| $V_{IL}$ | Low level input voltage | 4-5-6-7-8 | | | | | | 0.8 | V |
| | | 2-3-20-22-28 | | | | | | 1.3 | |
| $V_{IH}$ | High level input voltage | 4-5-6-7-8 | | | | 3.5 | | | V |
| | | 2-3-28-20 | | | | $V_{DD2}$-2 | | | |
| | | 22 | | | | $V_{DD2}$-1 | | | |
| $V_{IM}$ | Middle level input voltage | 22 | $V_{DD2}$= 10.8V | | | 4,5 | | 7.5 | V |
| | | | $V_{DD2}$= 13.5V | | | 5 | | 9 | |
| $V_{OL}$ | Low level output voltage | 23-24-25-26 | $V_{DD2}$= 10.8V | $I_{OL}$= 1 mA | | | | 3 | V |
| | | 15-19 | $V_{DD2}$= 10.8V | $I_{OL}$= 10 mA | | | | 1 | |
| | | 16-17 | $V_{DD2}$= 10.8V | $I_{OL}$= 1 mA | | | | 0.5 | |
| | | 14 | $V_{DD1}$= 17V<br>$V_{DD2}$= 10.8V | $I_{OL}$= 2.5 mA | | | | 8 | |
| $V_{OH}$ | High level output voltage | 27 | $V_{DD2}$= 10.8V | $I_{OH}$= -1 mA | | 2.4 | | | V |
| $I_{O(off)}$ | Output leakage current | 27 | $V_{DD2}$= 13.5V | $V_{O(off)}$= $V_{SS}$ | | | | -50 | µA |
| | | 23-24-25-26 | $V_{DD2}$= 13.5V | $V_{O(off)}$= 19V | | | | 100 | |
| | | 15-16-17-19 | $V_{DD2}$= 13.5V<br>$V_{O(off)}$= 13.5V | | | | | 50 | |
| | | 14 | $V_{DD1}$= 19V<br>$V_{O(off)}$= 30V | $V_{DD2}$= 13.5V | | | | 100 | |
| $I_I$ | Input current | 4-5-6-7-8-22 | $V_I$ = 0 to 19V | | | | | \|25\| | µA |
| $I_{DD1}$ | Supply current | 10 | $V_{DD1}$= 19V | | | | | 3 | mA |
| $I_{DD2}$ | Supply current | 13 | $V_{DD2}$= 13.5V | | | | 32 | 45 | mA |
| $I_{PP}$ | Memory supply current | 9 | $V_I$= 30V | write | peak | | | 65 | mA |
| | | | | | average | | | 16 | |
| | | | | erase | peak | | | 1 | |
| | | | | | average | | | 0.5 | |
| $R_I$ | Input resistance | 2-3-28 | See Fig. 1a | | | | 0.5 | | MΩ |

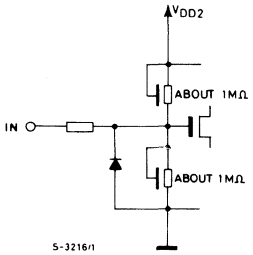
## DYNAMIC ELECTRICAL CHARACTERISTICS ($f_{clock}$ = 4.43 MHz)

| Parameter | | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $f_o$ | Fine tuning output repetition rate | Pin 19 (see also fig. 9) | | 17305 | | Hz |
| D | Fine tuning output duty cycle | | 1/8 | | 8/8 | |
| $t_{w3}$ | Width of erase pulses | Pin 14 | | 115 | | µs |
| $T_3$ | Period of erase pulses | See also fig. 3 and 6 | | 231 | | µs |
| $t_3$ | Total time for one erase cycle (about 500 pulses) | | | 115 | | ms |
| $t_{w4}$ | Width of write pulses | Pin 14 | | 115 | | µs |
| $T_4$ | Period of,write pulses | See also fig. 2 and 5 | | 462 | | µs |
| $t_4$ | Total time for one write cycle about 950 pulses) | | | 440 | | ms |
| $t_{w5}$ | Width of clock pulses | Pin 16 | | 1.3 | | µs |
| $T_5$ | Period of data and clock pulses | Pin 17 See also fig. 8 | | 3.6 | | µs |
| $t_5$ | Total time for one display burst (15 pulses) | | | 54 | | µs |
| $t_6$ | Burst repetition time | | | 3.69 | | ms |
| $t_7$ | Acceptance time of the commands | Pins 2-3-28 | | 31 | | ms |
| $t_8$ | Acceptance time of the commands | Pin 20 | | 3.6 | | µs |

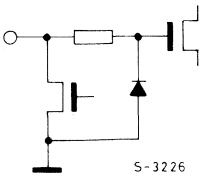
**Input and output configurations**
All outputs (except the Mute one) have open drain configuration.
The Mute output has a source follower.
Inputs have the following configurations:

Fig. 1

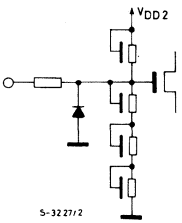
a) Pins 2, 3, 28



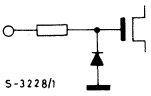

b) Search speed (pin 12)




c) Clock input (pin 11)




d) Other inputs (pin 4-5-6-7-8-12-20-21-22)



## DESCRIPTION

The circuit description will be made following both pin sequence and pin function.

### Pin 1 - $V_{SS}$ (GND)

The substrate of the integrated circuit is connected to this pin. It is the reference point for all voltage parameters of the device and must be connected to the lowest potential of the supply voltage, normally ground.

### Pin 2 - Store/sequential band change input

If this input pin is briefly connected to $V_{SS}$ the 12 bits of the digitized tuning voltage, the 2 bits for band selection and the 3 bits of fine tuning information are stored.
The command is disabled during search and the execution of the store cycle.
The store cycle consists of two operations: at first the old word is cancelled and afterwards the new content is written.
If this input pin is briefly connected to $V_{DD}$, the selected band output changes in the sequence written below, to obtain a step-by-step band selection.

VHF III
UHF
VHF I
S
VHF III and so on

### Pin 3 - Fine tuning +/— (on panel)

This input accepts the Fine tuning +/— commands given from the panel.
The commands are accepted according to the following rules:

| Input levels | Command |
|---|---|
| M (input floating) | No command |
| H | FT + |
| L | FT — |

Each command corresponds to one step change; to have more changes the key must be released and the command repeated.

### Pin 4 - T input (fine tuning +/— from remote control)

The Fine tuning +/— commands given from Remote control are applied to this input in the form of a series of positive pulses. The threshold of discrimination of the pulses is different for the M193A, C and the M193D.

| Type | $t_{w1}$ (FT +) | $t_{w2}$ (FT -) |
|---|---|---|
| M193A and C | > 1.8 ms | < 1.7 ms |
| M193D | > 120 $\mu$s | < 80 $\mu$s |

The M193A and C are compatible with the M1130 remote control receiver.
The M193D interfaces with either the M1130 and the SAA 1251 receivers.
When the Fine tuning command is given, the duty cycle of the output of pin 19 (Fine tuning output) is changed at the rate of one step every 0.56 sec.
If the pulses are present for less than 0.56 sec. step-by-step operation can be obtained.
If this input is not used it must be connected to $V_{SS}$ (GND).

## Pins 5-6-7-8 - Program inputs

This 4-line bus selects the program according to the truth table given below:

| Program | PA | PB | PC | PD |
|---|---|---|---|---|
| 1 | L | L | L | L |
| 2 | H | L | L | L |
| 3 | L | H | L | L |
| 4 | H | H | L | L |
| 5 | L | L | H | L |
| 6 | H | L | H | L |
| 7 | L | H | H | L |
| 8 | H | H | H | L |
| 9 | L | L | L | H |
| 10 | H | L | L | H |
| 11 | L | H | L | H |
| 12 | H | H | L | H |
| 13 | L | L | H | H |
| 14 | H | L | H | H |
| 15 | L | H | H | H |
| 16 | H | H | H | H |

## Pin 9 - $V_{PP}$ - Memory supply

A series of pulses is applied to this pin during the store cycle. The timing of these pulses is given by the output of pin 14 and it is different during erase and write cycle as shown in fig. 2 and 3.
During a store cycle the old word is at first cancelled and the new one is written afterwards.

Fig. 2 - Memory Erase supply

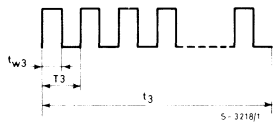
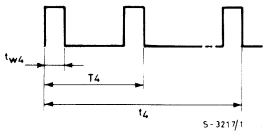



Fig. 3 - Memory Write supply



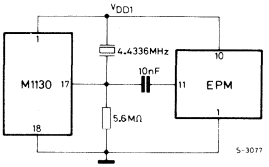

## Pin 10 - $V_{DD1}$

This pin has to be connected to a power supply with the characteristics shown in the recommended operating conditions.

## Pin 11 - Clock input

When the device is used alone the internal oscillator operates with a 4.43 MHz crystal connected between pin 11 and ground.
It can also operate with a single crystal together with M1130 as shown in fig. 4.
It is not suggested to use the oscillator of the M193 to drive external circuits.

Fig. 4



## Pin 12 - Search speed

An external RC network is connected to this pin in order to set the frequency of the internal oscillator which, in turn, sets the scan speed during Search mode.
The scan speed can be adjusted over a wide range.
The relationship of search speeds between UHF, VHF and S is a follows:

**Automatic:**

FAST UP VHF = the frequency externally fixed
FAST UP UHF = S = 1/2 FAST UP VHF
MEDIUM DOWN VHF = 1/4 FAST UP VHF
MEDIUM DOWN UHF = S = 1/4 FAST UP UHF (1/8 FAST UP VHF)
SLOW UP VHF = UHF = S = 67.7 Hz
SLOW DOWN VHF = UHF = S = 8.4 Hz

**Manual:** UP or DOWN UHF = S = 1/2 UP of DOWN VHF

The manual Fast up or down speed is obtained by changing the frequency of the oscillator. The maximum capacitance which should be connected to this pin is 100 nF.

## Pin 13 - $V_{DD2}$

This pin has to be connected to a power supply with the characteristics indicated in the recommended operating conditions.

## Pin 14 - Memory write timing output

This output gives the timing for the pulses to be applied on pin 9 during the store cycle. The output consists of an open drain transistor.
The waveforms are shown in fig. 5 and 6, and are different during erase and write cycle, as already described for pin 9.

Fig. 5 - Memory Erase Current

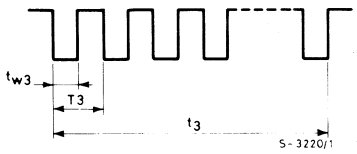
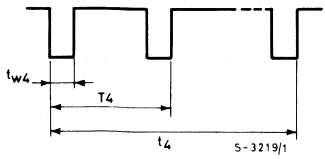


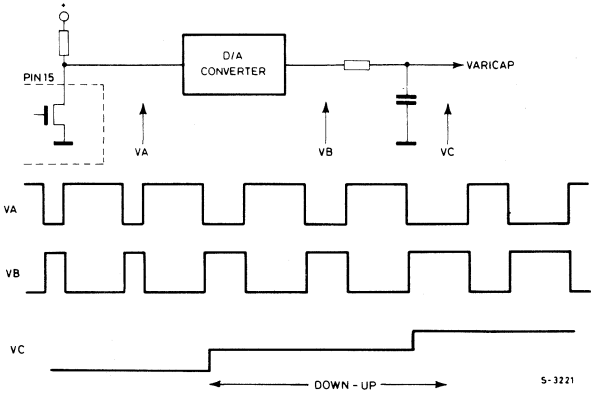

Fig. 6 - Memory Write Current



## Pin 15 - Digitized tuning voltage output

The output consists of a variable frequency/variable width pulse train which, after filtering, provides the tuning voltage to the varicaps.
This signal carries 13 bits of information (only 12 bits however are stored in the memory).
The output circuit consists of an open drain transistor which offers a low impedance to ground when in the on state.
The output waveforms are shown in fig. 7.

Fig. 7



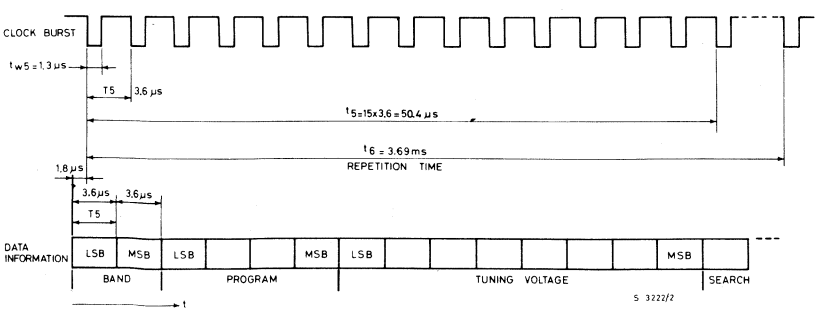

## Pin 16 - Clock output for external display

A burst containing 15 clock pulses is available on this pin. These clock pulses are synchronized with Data Information as described in fig. 8.

## Pin 17 - Data output for external display

A 15 bit burst is available on this pin.
In contains the 8 most significant bits of the digitized tuning voltage, 2 bits for band information, 4 bits for program information and 1 bit which indicates whether the system is in the Search mode (both in automatic and manual). This data is in complementary form (see fig. 8).
These two outputs (pins 16 and 17) work in connection with the M191 (On screen tuning bar display).
When the burst is not transmitted, the output transistor is in the off position.

Fig. 8



## Pins 18 - 21 - Test pins

These pins must be connected to $V_{SS}$ (GND).

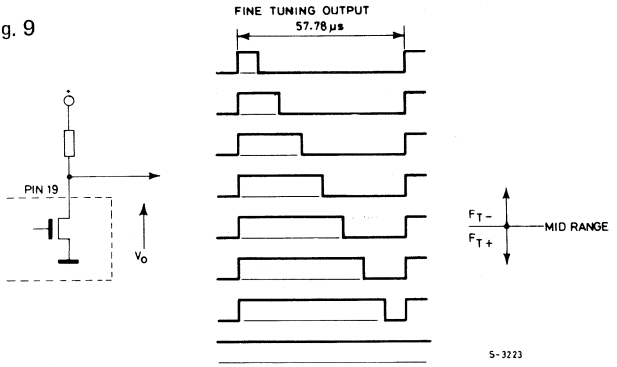
## Pin 19 - Fine tuning output

Fine tuning information is available on this pin in the form of a square wave having a frequency of 17305 Hz and duty cycle variable in 8 positions as indicated in fig. 9.
The voltage generated after filtering is fed to the AFC loop and detunes the receiver by a small $\Delta f$ while maintaining the action of the AFC.
The Fine tuning function operates as follows:

- during the search the output is set at mid-range (see fig. 9).
- when the search has been completed it is possible to operate on the Fine tuning +/— commands (pin 3 for Remote control operation or pin 4 for panel operation). The Store command memorizes this information together with the 12 bit tuning voltage and 2 bit band information
- when a memorized program is recalled it is still possible to act on the Fine tuning commands.

Any change in Fine tuning is only memorized by the Store command.

Fig. 9




## Pin 20 - Automatic/manual selection

This pin is used to change the Search mode. When it is connected to $V_{DD}$ the system operates in Automatic mode; when it is at $V_{SS}$ (GND) the system works manually. The change Auto-manual or viceversa can be made at every time without precluding the right operation of the system.

## Pin 22 - Stop/afc input

This pin is used only in automatic search mode.
When the EPM is in manual operation this pin is internally disabled.
The Stop/afc is also internally disabled during any program change for the time the Mute signal lasts. This input can have three different levels: high (H), middle (M), low (L). The middle level, unlike the other three level inputs of the circuit, is not internally generated and has to be externally determined according to the recommended operating conditions. If this input is not used it has to be connected to $V_{SS}$ (GND) or to $V_{DD2}$.

The input has two different functions depending on whether the system is in the search or in normal operation (AFC control).

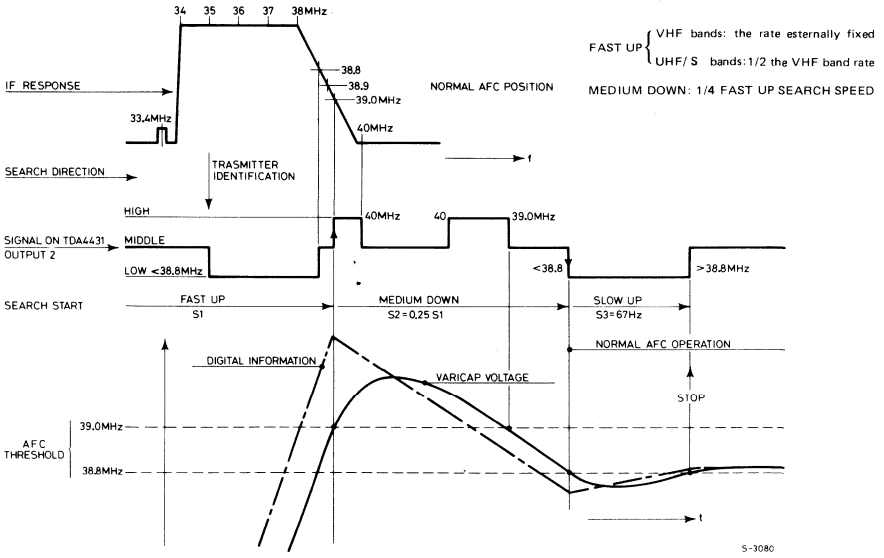
A) **Search mode:** after depressing the Search start key, the transitions and levels of the signals coming from the TDA 4431, applied to this pin, control the search function and determine when the search must stop, i.e. a TV station has been recognized.
The circuit operates with the following sequence (see fig. 10 for reference and explanation of pin 12 for speed definition):

1 - after pressing the search start key the search occurs in the Fast up mode

2 - subsequent transitions on pin 22 Stop/afc input are ignored during the first 15 search steps. After that the first M-H transition on the input preceded by at least one M-L transition will set the search into the Medium down (fast up/4) mode.
The acceptance delay of 15 search steps has been introduced to avoid the condition where the system could stop on the previous station (for example in the case the search start command has been given just before an AFC control command).

3 - the next M-L transition will switch the search to Slow up speed (67.7 Hz).
At this point the system is in normal AFC operation.

Fig. 10 - Automatic station capture diagram



B) **AFC operation:** when a station is perfectly tuned, the input signal coming from TDA 4431 is at middle level.
If the tuning moves lower than the threshold (below 38.9 MHz), the pin 22 goes low and the 13 bit internal counter is moved with Slow up speed to determine an increasing of the varicap voltage. When a detuning occurs in the opposite direction the input will go high and the tuning voltage is decreased with Slow down speed (8.4 Hz).
The increase or decrease of the tuning voltage is stopped as soon as the input returns to M level. Therefore during normal operation pin 22 acts as AFC control command.

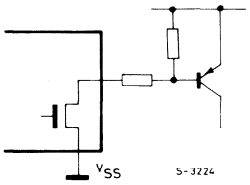
C) **Recall from memory:** when the circuit is in automatic operation mode and a pre-memorized program is recalled from Memory, a fixed value of 8 steps (≅ 31.2 mV) is subtracted from the tuning voltage. This corresponds to a detuning of about 0.6 MHz (UHF) and of 0.3 MHz in VHF III into that part of the IF response curve which corresponds to the fully transmitted sideband.
At this point the AFC operation takes over as described in point B) above and the exact tuning is reached in about 0.2 sec.
Due to this feature the AFC capture ratio will be increased and the requirements for stability of the tuner, of the reference voltage sources and of stability of the D/A converter are less severe.
In manual operation mode the memory content is instead read without any change.

## Pins 23-24-25-26 - Band drive outputs

The information for band selection is present on these outputs, consisting of open drain transistors, one of which, in connection with the selected band, is conducting (see fig. 11).
The relations between pins and bands are as follows:

Pin 23 = VHF I
Pin 24 = VHF III
Pin 25 = UHF
Pin 26 = S

Fig. 11




## Pin 27 - Mute output

A source follower transistor is provided to give a high level output during mute function.
The mute is present in the following cases:

- during automatic search. The mute is present 110 msec before the start of the search.
- during any program change for 320 msec.
  The mute is active 110 msec before the program change takes place.
- when the supply voltage $V_{DD2}$ is applied, for about 320 msec.
- when the supply voltage $V_{DD2}$ is removed.

## Pin 28 - A) Automatic operation: search start
## B) Manual operation: up/down search

This input is a three level one, i.e. it is normally in the middle level and the above mentioned functions are activated when it is connected to $V_{DD2}$ or to GND.
The input is kept at a voltage corresponding to about the half of the supply voltage by an internal divider made with two resistors of about 1 Mohm.

**A) Automatic operation**

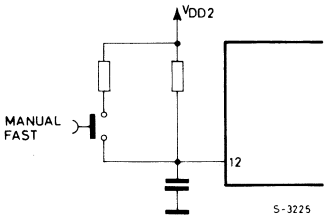
M193A - When the pin 28 is briefly connected to GND the search starts on the bands VHF III-UHF which are scanned in sequence. If it is connected to $V_{DD2}$ the search is made on band VHF I and S. If the key is kept pushed, another search can start only by releasing the key and connecting is again to GND or $V_{DD2}$. If a Search start command is given while the system is already in search operation, the search is immediately stopped and after restarted on the new group of selected bands; the band where the system will search is that which has the same search speed of the previous one.
M193C, D-When the pin 28 is briefly connected to GND or to $V_{DD2}$, the search starts and remains in the previously selected band.
All types work as follows: if the key is kept pushed, another search can start only releasing the key and connecting it again to GND or $V_{DD2}$. During the search the tuning voltage is always changing from lower to higher voltage levels. The search is automatically stopped when the first station is found. The search is also stopped whenever a program change command is given. When the upper limit of the tuning voltage is reached, the search restarts from the lower limit of another band (M193A) or of the same band (M193C, D), after 210 msec of temporary stop. The search speed is determined by the RC network connected to pin 12.

B) **Manual operation**

When the input is connected to $V_{DD2}$ the content of the internal counter is changed in such a way to have an increasing of the varicap voltage.
If the input is connected to GND the varicap voltage is decreased.
The search speed is determined by the RC network applied on pin 12.

Fast/low search speed is possible by changing the value of the same RC network (see fig. 12).
In manual operation the search is always made in the same band.
No inhibit of the search is provided when the lower or the upper limits of the varicap voltage are reached.
Step-by-step band selection is possible by temporarily connecting pin 2 to $V_{DD2}$.

Fig. 12



## GENERAL INFORMATION

**Command acceptance rules**

1) When a manual command at pin 2, 3, 28 is given, an internal counter is immediately started. The command is accepted only after about 31 msec. of its continuous presence. If the command disappears before (for example in consequence of contact bouncing), the counter is immediately reset. When a command has been accepted, no other manual command is accepted until the previous command has been released.

2) Program change commands are immediately accepted and if the circuit is in the automatic search position, the search is stopped.
Manual commands given during the execution of the program change are not accepted except the automatic search start command.
This one is internally stored and executed at the end of the program change.

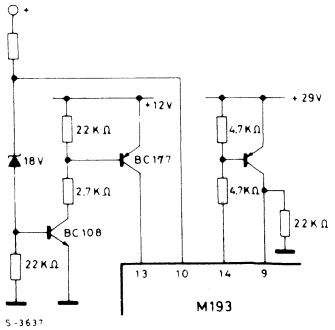
3) During the store cycle only the program change and the search start commands are accepted and executed at the end of the cycle.
The other commands are ignored.

**Power-on sequence of supply voltages**

To guarantee the correct reading of the memory at power-on the supply voltages must be applied as follows:

$$V_{DD1}\ (+18V),\ V_{DD2}\ (+12V)$$

The +18V must be higher than 16.5V 110 msec after the 12V is passed through the power-on reset threshold ($\simeq$ 6V).
From 0 to 6V the slew rate of the 12V is not important, from 6 to 10V the slew rate must not exceed 110 ms. If it is not possible to guarantee the availability of the 18V supply before the 12V we suggest using the following application.
It is recommended that the 29V is not applied when the 12V is not present. However there are no reliability problems if at power on and power off the 29V exists for a few seconds without the 12V supply being present.



## PLL TV MICROCOMPUTER INTERFACE

- HIGHLY INTEGRATED SOLUTION INCLUDING PLL SYNTHESISER, NV MEMORY, D/A CONVERTERS, BAND SELECT OUTPUTS, CLOCK OSCILLATOR, IR SIGNAL PRE-PROCESSOR AND SERIAL BUS INTERFACE
- 32x16 BITS OF NV MEMORY WITH LIFETIMES OF $10^4$ CYCLES/WORD AND MINIMUM 10 YEARS RETENTION STORES TUNING DATA FOR 30 CHANNELS PLUS PRESET VALUES FOR THE SIX ANALOG OUTPUTS
- PRE-PROCESSOR FOR INFRARED REMOTE CONTROL SIGNALS REDUCES COMPONENT COUNT
- SIX PWM D/A CONVERTERS WITH 64-STEP RESOLUTION
- FOUR OPEN-DRAIN BAND SELECT OUTPUTS RATED TO 13.2V
- ON-CHIP 4 MHz CLOCK OSCILLATOR WITH BUFFERED OUTPUT
- INTEGRATED DIGITAL POWER-ON RESET
- 3-WIRE SERIAL BUS TO LOAD/READ INTERNAL REGISTERS
- TECHNICAL NOTE TN 152 AVAILABLE

The M206 is a highly integrated, programmable LSI integrated circuit for microcomputer controlled TV applications, realized using an advanced N-channel double polysilicon gate technology (NVMOS) that allows the integration of non-volatile memory and standard logic on the same chip.

It contains a phase-locked loop (PLL) synthesiser, six pulse-width modulation (PWM) digital/analog converters, a four-bit parallel output buffer, clock oscillator with buffered output, pre-processor for infrared remote control signals and a 3-wire serial bus interface.

The M206 interfaces with a microcomputer through the three-wire serial bus and is programmed by loading thirteen internal registers - twelve of which are readable to simplify programming.

The PLL synthesiser requires an external 64 + 15/16 prescaler and divider and works with a phase comparator reference frequency of 0.9765 kHz. Outputs are provided to control the division ratio of the prescaler and to signal the out-of-lock condition to the microcomputer.

The infrared remote control signal pre-processor consists of a preamplifier, a squarer and a digital filter to separate noise from signals transmitted by the M708, M709 and 710 remote control transmitters. The output of this pre-processor is connected to the interrupt input of a microcomputer programmed to receive and decode the signal.

The M206 is supplied with two separate 5V supply inputs, each provided with internal power-on reset circuits. The first, $V_{DD1}$, supplies the remote control and clock circuits in both standby and TV set operation. The second, $V_{DD2}$, supplies the rest of the circuits and is only active during TV operation.

The M206 is packaged in a 28-pin dual in-line plastic package.

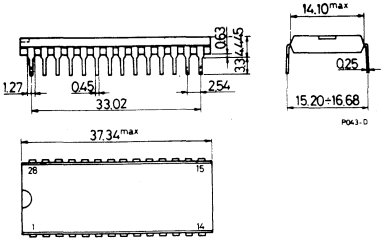
**ORDERING NUMBER:** M206 B1

## ABSOLUTE MAXIMUM RATINGS

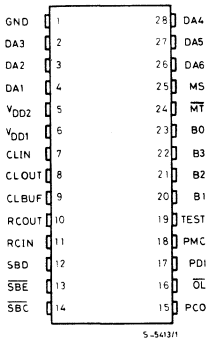
| | | | |
|---|---|---|---|
| $V_{DD1}$, $V_{DD2}$ | Supply voltage | -0.3 to 7 | V |
| $V_{PP}$ | Memory supply voltage | -0.3 to 28 | V |
| $V_I$ | Input voltage (except pin 11) | -0.3 to 7 | V |
| | pin 11 | -0.3 to 15 | V |
| $V_{O(off)}$ | Off state output voltage (except pins 2-3-4-26-27-28-20-21-22-23-24) | 7 | V |
| | pins 2-3-4-20 to 23-26 to 28 | 15 | V |
| | pin 24 | 28 | V |
| $I_{OL}$ | Output current (except pins 2-3-4-26-27-28) | 5 | mA |
| | pins 2-3-4-26-27-28 | 10 | mA |
| $I_{OH}$ | Output current (pins 15, 9) | -5 | mA |
| $P_{tot}$ | Total package power dissipation | 1 | W |
| $T_{stg}$ | Storage temperature | -25 to 125 | °C |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

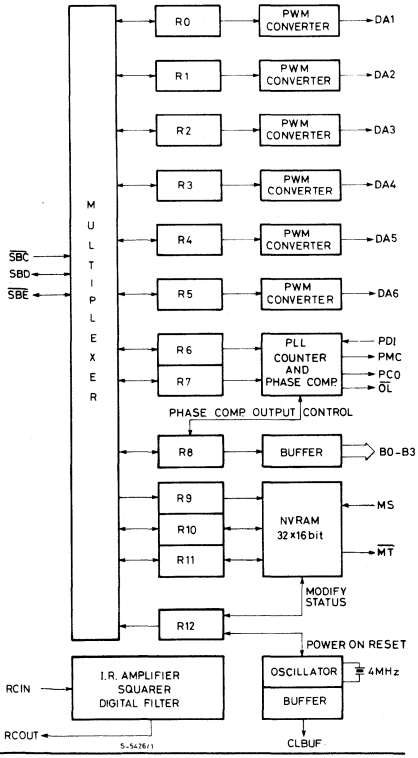
## MECHANICAL DATA (dimensions in mm)




## PIN CONNECTIONS




## BLOCK DIAGRAM



## PIN DESCRIPTION

**DA1-DA6** – Digital/Analog converter outputs (open-drain outputs)
Output from the six pulse-width modulation D/A converters.

**B0-B3** – Band drive outputs (open-drain outputs)
Outputs from the four-bit buffer used for band selection.

**SBD** – Serial Bus Data (bidirectional)
Data line for serial communication with a microcomputer.

**$\overline{\text{SBE}}$** – Serial Bus Enable (bidirectional, active low)
Enables serial bus transmissions.

**$\overline{\text{SBC}}$** – Serial Bus Clock (input, active low)
Clock for serial bus transmissions.

**RCIN** – Remote Control signal Input (analog input)
Input to the infrared remote control signal preprocessor. Connected to the output of the IR preamplifier. Minimum input level 0.5V peak-to-peak.

**RCOUT** – Remote Control signal Output
Output from the infrared remote control signal pre-processor. To be connected to the interrupt input of a microcomputer.

**PDI** – Programmable Divider Input (input)
This pin is the input of the programmable divider and is connected to the output of the prescaler.

**PCM** – Prescaler Modulo Control (output)
Control signal to set the prescaler division ratio (15 if high, 16 if low).

**$\overline{\text{OL}}$** – Out of Lock (output, active low)
Signals an out of lock condition. This output is also active during the power on reset sequence.

**PCO** – Phase Comparator Output
The output of the phase comparator. Connected to the input of a low pass filter used to generate the tuning voltage.

**TEST** – Test pin (input)
The test pin is used only to test the device and is not specified for customer use. It must be connected to ground.

**CLIN, CLOUT** – Clock oscillator connections
A 4 MHz quartz crystal is connected between these pins.

**$V_{DD1}$, $V_{DD2}$, GND** – Power Supply Connections
$V_{DD1}$ is the +5V standby supply input; $V_{DD2}$ is the main +5V supply input.

**MS** – Memory Supply Input (input)
Programming pulses for the NV memory are supplied to this pin during store cycles.

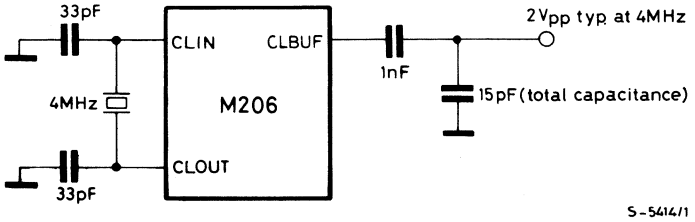
**$\overline{\text{MT}}$** – Memory Timing (output, active low)
This output supplies the timing for the memory write pulses supplied to the MS input during store cycles.

**CLBUF** – Clock Buffer (output)
This is a buffered output from the on-chip clock oscillator and can be used to drive other components (for example the microcomputer).

## FUNCTIONAL DESCRIPTION

### CLOCK

To use the internal oscillator a 4 MHz quartz crystal is connected between the pins CLIN and CLOUT. If an external clock is used this must be connected to CLIN and CLOUT left unconnected or, if required as a clock output, loaded by a capacitor up to 15 pF. The minimum external clock amplitude is 2V peak-to-peak. A buffered clock output, CLBUF, is provided which can drive up to three ± 100 μA loads.




### LOADING AND READING INTERNAL REGISTERS

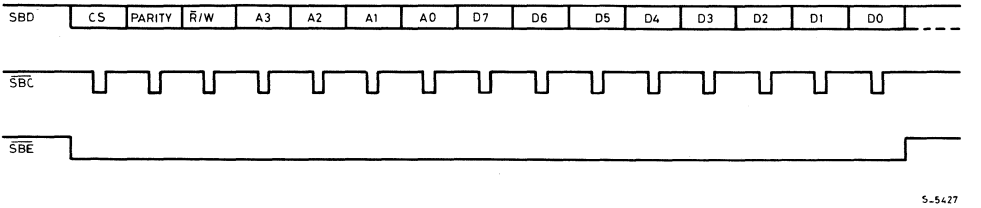
The M206 is programmed by loading a set of internal registers through a 3-wire serial bus. The functions of these registers are summarised in table 1.

TABLE 1 – Summary of internal registers

| Register Number | Address | | | | Number of bits | Function |
|---|---|---|---|---|---|---|
| | A3 | A2 | A1 | A0 | | |
| 0 | L | L | L | L | 6 | D/A converter n° 1 |
| 1 | L | L | L | H | 6 | D/A converter n° 2 |
| 2 | L | L | H | L | 6 | D/A converter n° 3 |
| 3 | L | L | H | H | 6 | D/A converter n° 4 |
| 4 | L | H | L | L | 6 | D/A converter n° 5 |
| 5 | L | H | L | H | 6 | D/A converter n° 6 |
| 6 | L | H | H | L | 7 | PLL counter (MSB) |
| 7 | L | H | H | H | 8 | PLL counter (LSB) |
| 8 | H | L | L | L | 7 | Buffer outputs/Phase comp. output control |
| 9 | H | L | L | H | 5 | NV Memory address |
| 10 | H | L | H | L | 8 | NV Memory DATA |
| 11 | H | L | H | H | 8 | NV Memory DATA |
| 12 | H | H | L | L | 2 | NV Memory modify control/ Reset control |

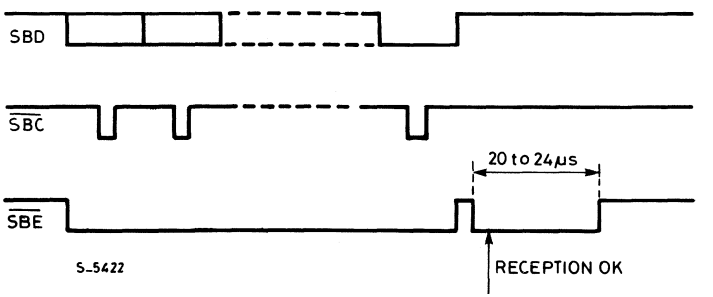
The 3-wire serial bus consists of the signals SBD (Serial Bus Data), $\overline{\text{SBE}}$ (Serial Bus Enable) and $\overline{\text{SBC}}$ (Serial Bus Clock). The enable and data pins, SBD and $\overline{\text{SBE}}$, are bidirectional.
Data is accepted when the clock is low (active) and latched into the M206 on the low-high transition of the clock. All bus transfers are controlled by $\overline{\text{SBE}}$.

**Register Loading**
Serial data transferred from the microprocessor to the M206 has the following format:

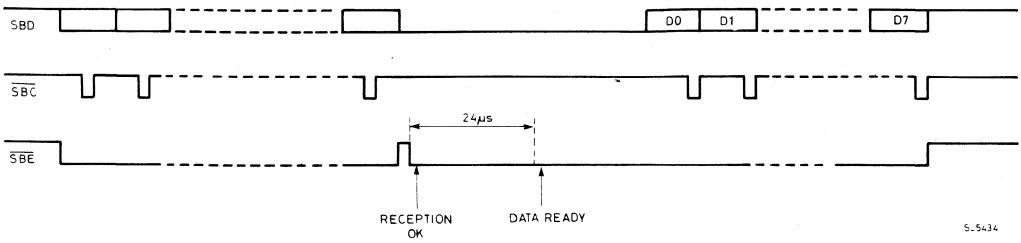



| Bit | Description |
|---|---|
| CS | Chip select (always low) |
| PARITY | Parity bit (the number of "H" bits transmitted is odd) |
| R̄/W | Read/Write. High for register load; low for register read |
| A0-A3 | Register address (see Table 1) |
| D0-D7 | Data to be loaded into register (load operation only) |

The received data word is checked – length, CS and parity – immediately after the low-high transition of $\overline{SBE}$. If the received word is valid this is signalled to the microprocessor by forcing the $\overline{SBE}$ line low for 20-24 $\mu$s.




**Register Reading**
M206 registers are read by transmitting a 15 bit word as shown in fig. 4 with $\overline{R}/W$ low and the address of the register to be read in A0, A1, A2, A3. Bits D0-D7 can be high or low except when register 9 is addressed.
If this word is received correctly the $\overline{SBE}$ line is immediately pulled low by the M206 and after 24 $\mu$s the contents of the addressed register will be available to be read. The microprocessor reads this data by sending eight clock pulses. Data is output on the low-high transition of $\overline{SBC}$ and the first data bit is available before the first clock pulse.




**Loading the Non-Volatile Memory**

Data is stored in the 32 x 16-bit NV memory by loading the new contents into registers 10 and 11 then the address into register 9. The memory modify cycle begins when the address has been loaded and successful completion is indicated by a logic "1" in bit zero of register 12.

The time for a modify cycle varies from a few milliseconds to several hundred milliseconds during the device lifetime and is not internally limited. The storage operation should be aborted after one second if it proves unsuccessful. This is done by setting bit zero of register 12.

**Reading the Non-Volatile Memory**

The NV memory is read by loading the address into register 9. The contents of the addressed word are automatically loaded into registers 10 and 11 and can be read by two register read operations. The data is ready 200 μs after the address load.

## PLL COUNTER

The PLL counter consists of a single counter that acts as the program counter (11 bit) and is swallow counter (4 bit) alternately. Data for the PLL counter is loaded into registers 6 and 7. Register 6 must be loaded first because the register 7 load operation initiates the data transfer to the PLL counter.

The reference frequency is produced by dividing the clock frequency by 4096. With a 4 MHz clock this gives a reference frequency of 976.5 Hz.

An out-of-lock signal is generated (output $\overline{OL}$) when the phase error between the reference frequency and the input frequency exceeds 0.72° (2 μs).

The phase comparator output, PCO, has a three-state push pull configuration with a high level of 5V and a low level of 0V (with zero current sink or pump). The output impedance (both states) is typically 200Ω (400Ω maximum). The phase comparator output can be set to a high impedance state (both sink and pump transistors off) by setting bit 4 of register 8. The output is held in the high impedance state until this bit is reset. The phase comparator output should be set to high impedance when changing band.

**Recovering lock**

The phase comparator output can also be set to high and low levels to restore normal operation when the oscillator stops or the prescaler functions incorrectly at high frequency.

In the first condition (oscillator off) the prescaler sometimes oscillates, at high frequency. The loop reacts by reducing the varicap voltage in an attempt to reduce the frequency, thus worsening the situation. This out-of-lock condition is signalled to the microprocessor (by the $\overline{OL}$ output) which can set the phase comparator output to low level, forcing the varicap voltage up and restarting the oscillator. The phase comparator output is forced low by setting bit 5 of register 8. After about 1 ms this bit is automatically reset and the loop should lock again.

When the out-of-lock condition is caused by a failure of the prescaler to operate correctly at high frequencies the loop reacts by increasing the voltage, hence the frequency, again worsening the situation. To recover from this condition the phase comparator output is set high. This is done by setting bit 6 of register 8 which, as in the previous case, resets itself after 1 ms.

The out-of-lock condition could also be caused by unwanted changes in band or PLL counter contents provoked by external interference (spikes on supply etc.). For this reason it is always advisable to reload the band and PLL counter registers before attempting to recover lock as described above. If the phase comparator output is in the high impedance state, the $\overline{OL}$ output signals the reset condition but not the out-of-lock condition.

**Calculating PLL Counter Values**

a) F = video carrier.

b) IF = 38.9 MHz.

c) The frequency to be synthesized is Fs = F + IF.

d) The Ref. frequency of the phase comparator is

$$F_{ref} = \frac{4.000\ MHz}{4096} = 0.97656\ kHz$$

e) Using the prescaler 64 + 15/16 the minimum frequency steps is

$$F_{ref} \times 64 = 62.5\ kHz$$

f) The modulo of division N is given by the ratio between the frequency to be synthesized and the reference frequency multiplied by 64. The result has to be rounded.

$$N_S = \text{Integer rounded } [\frac{F_S}{F_{ref} \cdot 64}]$$

g) With the 64 + 15/16 prescaler and the particular counter of the M206 the division by N is given by

$$N_S = (I_S + 1) \cdot 15 + (R_S + 1) \cdot 16$$

where I (integer part) controls the division by 15 (program counter) and R (rest) controls the division by 16 (swallow counter). For ease of calculation we decrement $N_S$ by one getting $N_C = N_S - 1$.
The numbers $I_C$ and $R_C$ are given by: $N_C = (I_C + 1) \cdot 15 + (R_C + 1) \cdot 16$

$$N_C - 31 = I_C \cdot 15 + R_C \cdot 16$$

using the formulas:

$$R_C = N_C - 31 - 15 \cdot \text{Integer } [\frac{N_C - 31}{15}]$$

$$I_C = \frac{N_C - 31 - R_C \cdot 16}{15}$$

$$R_S = R_C + 1$$

$$I_S = I_C - 1$$

**Example:**

Channel 21 $F = 471.25\ MHz$

$F_S = F + IF$ $\quad F_S = 471.25 + 38.9 = 510.15\ MHz$

$N_S = \text{Integer rounded } [\frac{510.15 \times 10^6}{62.5 \times 10^3}] = \text{Integer rounded } [8162.4] = 8162$

$N_C = N_S - 1 = 8161$

$R_C = N_C - 31 - 15 \cdot \text{Integer } [\frac{N_C - 31}{15}] = 8161 - 31 - 15 \cdot \text{Integer } [\frac{8161 - 31}{15}] =$

$= 8130 - 15 \cdot \text{Integer } [542] = 8130 - 15 \cdot 542 = 8130 - 8130 = 0$

$I_C = \frac{N_C - 31 - R_C \cdot 16}{15} = \frac{8161 - 31}{15} = 542$

$R_S = R_C + 1 = 0 + 1 = 1$

$I_S = I_C - 1 = 542 - 1 = 541$

R and I have to be translated into binary code.

## DIGITAL/ANALOG CONVERTERS

The six pulse-width modulation (PWM) D/A converters have a resolution of 64 steps and an output frequency of 16 kHz (with 4 MHz clock). At power on reset they are set to a duty cycle of zero.

## POWER ON RESET

The $V_{DD1}$ and $V_{DD2}$ supplies have an integrated digital power on reset with a duration of 250 ms. The reset condition is signalled by a low level on the out-of-lock output, $\overline{OL}$. The microprocessor can test this condition by reading bit 1 of register 12. This bit is zero during power on reset and the $\overline{OL}$ output remains active until it is read. Reading this bit automatically restores it to a high state.

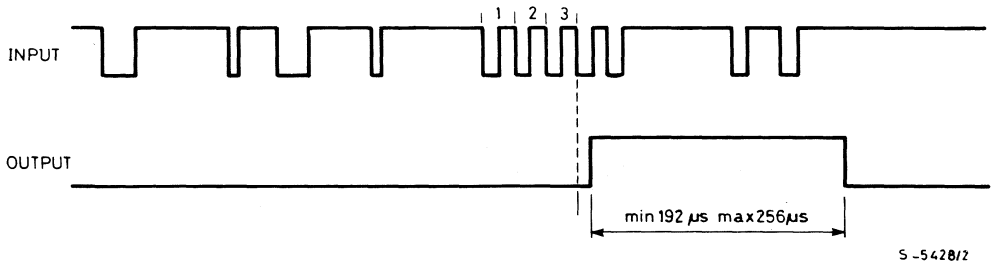
During power on reset time commands from the microprocessor are not acknowledged. Power on reset also sets the phase comparator output to a high impedance,state. It is restored by resetting bit 4 of register 8.

## REMOTE CONTROL SIGNAL PRE-PROCESSOR

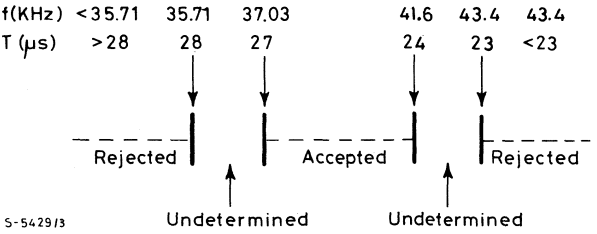
This section contains a preamplifier, squarer, digital filter and a pulse generator. The digital filter enables the pulse generator only if three successive negative going pulses (4 edges) are detected. The distance between these pulses must be in the range 24-27 $\mu$s (about 37-41 kHz with a 4 MHz clock). The input is not tested for the duration of the output pulse (192-256 $\mu$s).

If this pre-processor is used in conjunction with M709 or M710 remote control transmitters valid signals can be recognised in the presence of extreme noise conditions. Separating the signals from the noise externally in this way reduces the number of interrupts that the microcomputer has to handle thus allowing it to concentrate on other tasks. To take advantage of this section the M708, 709, 710 trasmitters must operate with a clock frequency in the range 492-508 kHz.

The input can be DC or AC compled to the I.R. preamplifier.
In case of DC coupling the quiescent input level is suggested to be 1.5 V.

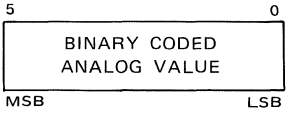



Response of the digital filter as a function of the input frequency (in kHz)



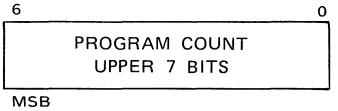
## M206 PROGRAMMING SUMMARY

Registers 0-5 – D/A Convertors 1-6



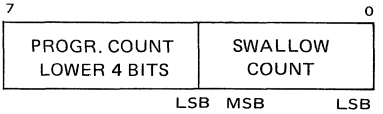

R0-R5
6 bits

Register 6 – PLL Program Counter



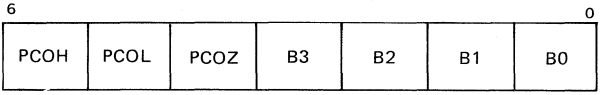

7 bits

Register 7 – PLL Program/Swallow Counter




8 bits

Register 8 – Band Drive Outputs/Phase Comparator Output Control



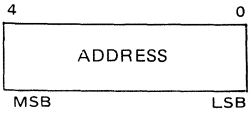

B0-B3 Band drive outputs B0-B3
PCOZ Phase Comparator Output High Impedance
PCOL Phase Comparator Output Low Level
PCOH Phase Comparator Output High level

| PCOH | PCOL | PCOZ | Phase comparator output |
|---|---|---|---|
| L | L | L | Normal PLL operation |
| L | L | H | High impedance state |
| L | H | L | Low for 1 ms then returns automatically to normal PLL operation |
| L | H | H | Low for 1 ms then returns to high impedance state |
| H | L | L | High for 1 ms then returns to normal PLL operation |
| H | L | H | High for 1 ms then returns to high impedance |
| H | H | L | Normal Operation * |
| H | H | H | High impedance * |

* These combinations are not accepted and PCOL, PCOH are automatically reset low after 1 ms.

## M206 PROGRAMMING SUMMARY (continued)

Register 9 – NV Memory Address

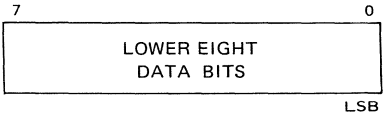



5 bits

Registers 10 & 11 – NV Memory Data

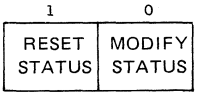



R10
8 bits




R11
8 bits

Register 12 – NV Modify Status/Reset Status




2 bits

| FLAG | L | H |
|---|---|---|
| MODIFY STATUS | Modify in progress | Modify over |
| RESET STATUS | Reset activated | Reset not activated |

## STATIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 0 to 70°C; typical values are at $T_{amb}$ = 25°C)

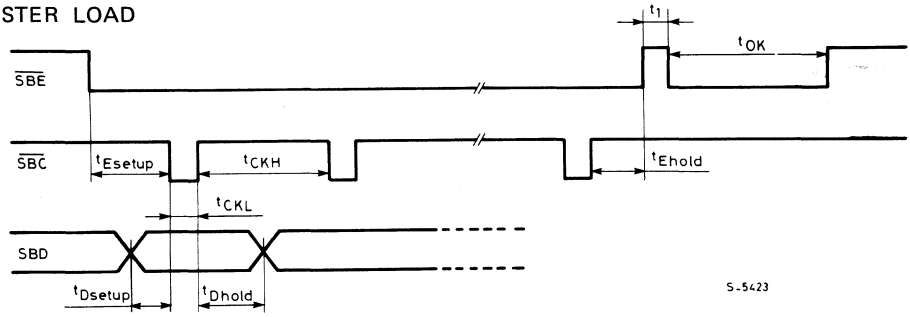
| Parameter | | Pins | Test conditions | | | Values | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Min. | Typ. | Max. | |
| $V_{DD1}$, $V_{DD2}$ | Supply voltage | 5-6 | | | | 4.75 | 5 | 5.25 | V |
| $V_{PP}$ | Memory supply voltage | 25 | | | | 24 | 25 | 26 | V |
| $V_{IL}$ | Input low voltage | 12-13-14-17 | | | | 0 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | 12-13-14-17 | | | | 2.4 | | 5.25 | V |
| $V_{IPP}$ | Peak to peak signal | 11 | AC COUPLING | | | 0.5 | | 13.2 | V |
| $V_{TH}$ | Threshold voltage | 11 | DC COUPLING | | | | 1.25 | | V |
| $V_{OL}$ | Output low voltage | 10-12-13 16-18-20 21-22-23 | $V_{DD}$= 4.75V $I_{OL}$= 1.6 mA | | | | | 0.4 | V |
| | | 9 | $V_{DD}$= 4.75V $I_{OL}$= 0.2 mA | | | | | 0.4 | |
| | | 15 | $V_{DD}$= 4.75V $I_{OL}$= 1 mA | | | | 0.2 | 0.4 | |
| | | 2-3-4-26 27-28 | $V_{DD}$= 4.75V | $I_{OL}$= 5 mA | | | | 1 | |
| | | 24 | $V_{DD}$= 4.75V | $I_{OL}$= 2.5 mA | | | | 8 | |
| $V_{OH}$ | | 9-18 | $V_{DD}$= 4.75V $I_{OH}$= -0.2 mA | | | | | 2.4 | V |
| | | 15 | $I_{OH}$= -1 mA | | | | $V_{DD2}$ -0.2 | $V_{DD2}$ -0.4 | |
| $I_{O(off)}$ | Output leakage current | 2-3-4-10-16 20-21-22-23 26-27-28 | $V_{DD}$= 4.75V | $V_{o(off)}$= 5.25V | | | | 10 | µA |
| | | 24 | $V_{DD}$= 4.75V | $V_{o(off)}$= 26V | | | | 100 | µA |
| $I_{IL}$ | Input low current | 12-13 | $V_{DD}$= 5.25V $V_{OL}$= 0.4V | | | | 50 | 200 | µA |
| $I_{OZ}$ | High impedance output current | 15 | $V_O$= 0 to $V_{DD2}$ | | | | ± 20 | | nA |
| $I_{DD1}$ | Supply current | 6 | $V_{DD1}$= 5.25V | | | | | 8 | mA |
| $I_{DD2}$ | Supply current | 5 | $V_{DD2}$= 5.25V | | | | | 30 | mA |
| $I_{PP}$ | Memory supply current | 25 | $V_{PP}$= 26V | Write | peak | | | 40 | mA |
| | | | | | average | | | 11 | |
| | | | | Erase | peak | | | 7 | |
| | | | | | average | | | 4.5 | |
| | | | | Read | peak | | | 6 | |
| | | | | | average | | | 2 | |

## DYNAMIC ELECTRICAL CHARACTERISTICS

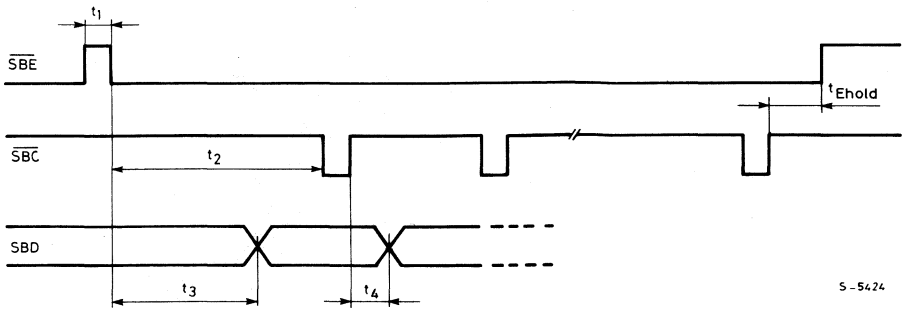
| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{CKL}$ | $\overline{SBC}$ LOW time | | 2 | | 50 | |
| $t_{CKH}$ | $\overline{SBC}$ HIGH time | | 4 | | | |
| $t_{Esetup}$ | $\overline{SBE}$ Set-up to $\overline{SBC}$ falling edge time | | 0.5 | | | |
| $t_{Ehold}$ | $\overline{SBE}$ hold time from $\overline{SBC}$ rising edge | | 3 | | | |
| $t_{Dsetup}$ | Data setup time | | 1 | | | |
| $t_{Dhold}$ | Data hold time | | 1 | | | |
| $t_1$ | Time between $\overline{SBE}$ rising edge and OK of reception | | | | 3 | µs |
| $t_{OK}$ | OK of reception time | | | 22 | 26 | |
| $t_2$ | Minimum $\overline{SBC}$ delay time from OK of reception | | 26 | | | |
| $t_3$ | Data valid time from OK of reception | | | 20 | 25 | |
| $t_4$ | Data valid time from $\overline{SBC}$ pulse | | | | 4 | |
| $t_5$ | Propagation delay of PMC | | | | 0.9 | |

## TIMING WAVEFORMS

### REGISTER LOAD

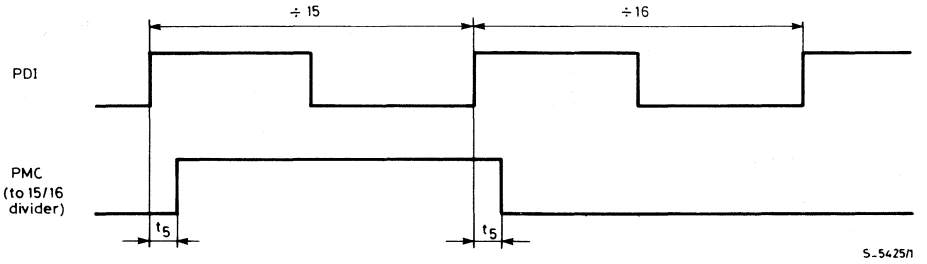



### REGISTER READ



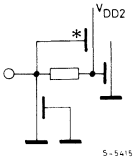
## TIMING WAVEFORMS (continued)

PRESCALER MODULO CONTROL TIMING

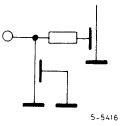



## INPUT AND OUTPUT CONFIGURATIONS

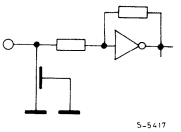
$\overline{SBC}$



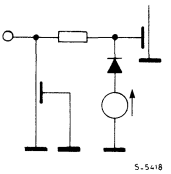

PDI



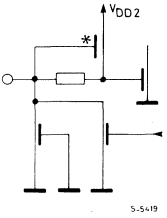

CLIN



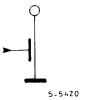

RCIN



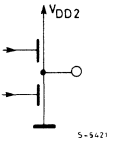

SBD, $\overline{SBE}$



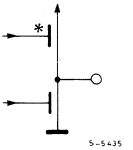

DA1-DA6, B0-B3
$\overline{OL}$, RCOUT




PCO



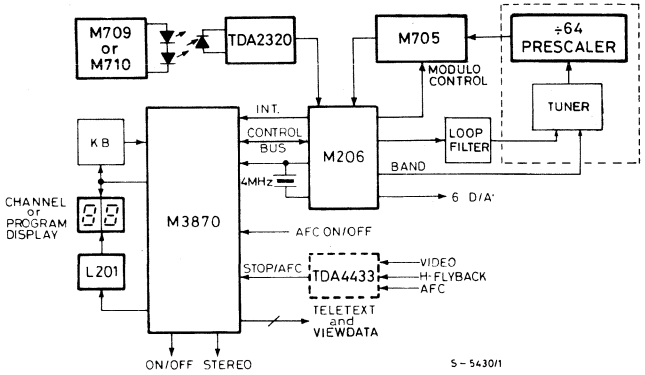

PMC, CLOUT
CLBUF




* Depletion transistors.

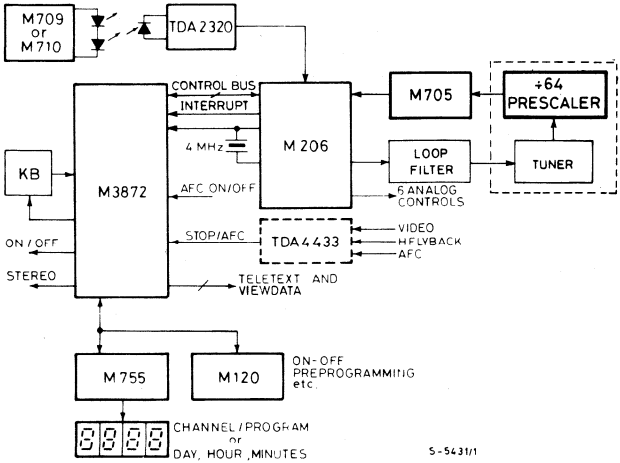
## TYPICAL APPLICATIONS

Remote controlled TV frequency synthesizer




- Remote Control Decoding by Microprocessor.
- 32 Station Non-Volatile Memory or 30 Station Memory + Normalized D/A Positions.
- Flexible System Operation.
- Frequency Synthesis of all Standard and CATV Channels.
- Direct Channel Selection.
- ± 4 MHz Fine Tuning (62.5 kHz per Step).
- Automatic Search within Channel (using TDA4433).
- AFC Operation (using TDA4433).
- 6 D/A Converters.
- Teletext and Viewdata Data Bus Conversion.

Remote controlled TV frequency synthesizer and clock timer




Frequency Synthesis as described in the Basic Configuration with the addition of:
- Further Station Memory, using M120, 1K NV MEMORY
- Clock and programmable timer for automatic switch ON/OFF, using M755.

## EPM 32 ELECTRONIC PROGRAM MEMORY FOR 32 STATIONS

- ONE CHIP INCLUDING CONTROL AND NV MEMORY
- SUPPLY VOLTAGE $V_{DD}$ = 5V ± 5% $V_{PP}$ = 25V ± 1V (ONLY FOR STORAGE AND READING)
- AUTOMATIC, SEMIAUTOMATIC AND MANUAL SEARCH MODES
- MANUAL SEARCH CONTROLLED BY ONLY TWO KEYS (UP AND DOWN). THE SEARCH SPEED IS AUTOMATICALLY INCREASED SMOOTHLY WITH THE TIME
- 4 BAND OUTPUTS WITH STEP-BY-STEP SELECTION AND THE POSSIBILITY OF SKIPPING UNWANTED BANDS
- MEMORY ADDRESSING AND COPY CAPABILITY
- EXTERNALLY ADJUSTABLE SEARCH SPEED
- 445 TO 510 kHz CLOCK OSCILLATOR
- VOLTAGE SYNTHESIZER, 8192 STEP RESOLUTION
- FINE TUNING IN 8 STEPS, STORABLE FOR EACH PROGRAM SEPARATELY
- MINIMUM EXTERNAL COMPONENTS
- INTEGRATED DIGITAL POWER-ON RESET (1 SECOND)
- TECHNICAL NOTE TN 153 AVAILABLE

The M293 is a monolithic integrated circuit constructed in N-channel silicon gate technology, designed to control a varicap tuner with a resolution of 8192 steps (13 bits) via a D/A converter, using the principle of voltage synthesis.
The device also includes a 544 bit NV Memory for storage of 32 stations. Each station is identified by a 17 bit word containing the information for tuning voltage (12 bits), band (2 bits) and fine tuning (3 bits). The circuit is able to operate in automatic, semiautomatic or manual modes. The search speed is controlled externally by an RC network and is adapted internally to the various bands and mode of operation. In the automatic mode the M 293 works in conjunction with the TDA 4433, which recognizes TV stations and converts the AFC-S-curve into a digital command. The stations are selected by applying a static bit binary word. A strobe input is also provide. A 7 segment decoder-driver (e.g. TDA 4092) can be connected to the same lines for Program number display.
A serial information output is provided so that using the M 191, the varicap voltage in the form of a linear bar and the selected band can be displayed on the screen.
The M 293 is available in a 28 lead dual in-line plastic package.

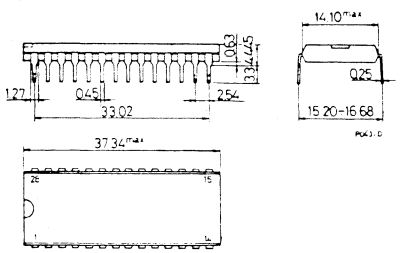
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 7 | V |
| $V_{PP}$ | Memory supply voltage | -0.3 to 28 | V |
| $V_I$ | Input voltage | -0.3 to 15 | V |
| $V_{O(off)}$ | Off state input voltage (except pin 10) | 15 | V |
| | pin 10 | 28 | V |
| $I_{OL}$ | Output current (except pins 11-19) | 5 | mA |
| | pins 11-19 | 7.5 | mA |
| $I_{OH}$ | Output current (pin 2) | -2 | mA |
| $P_{tot}$ | Total package power dissipation | 1 | W |
| $T_{stg}$ | Storage temperature | -25 to 125 | °C |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

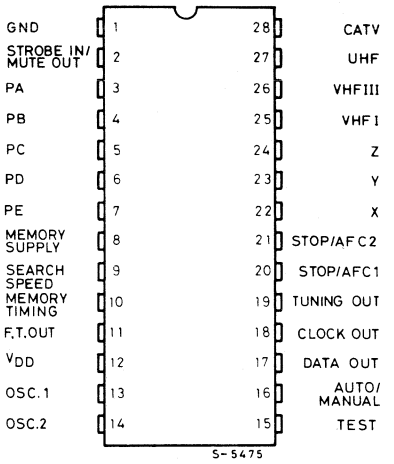
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ORDERING NUMBER:** M 293 B1

## MECHANICAL DATA (dimensions in mm)




## PIN CONNECTIONS

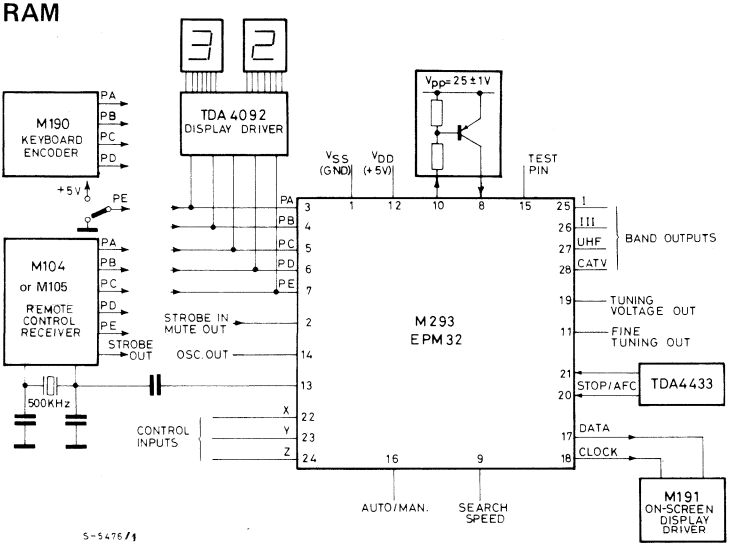



## RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | 4.75 to 5.25 | V |
| $V_{PP}$ | Memory supply voltage | 24 to 26 | V |
| $V_I$ | Input voltage | 0 to 13.2 | V |
| $V_{O(off)}$ | Off state output voltage (except pin 10) | max. 13.2 | V |
| | pin 10 | max. 26 | V |
| $I_{OL}$ | Output current (except pins 11 - 19) | max. 2.5 | mA |
| | pins 11 - 19 | max. 5 | mA |
| $I_{OH}$ | Output current (pin 2) | max. -0.25 | mA |
| $t_{pd}$ | Delay between memory timing and memory supply pulses | max. 5 | $\mu$s |
| f | Clock frequency | 500 | kHz |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |
| R9 | Search speed resistance (pin 9) | 18 to 330 | K$\Omega$ |
| C9 | Search speed capacitance (pin 9) | max. 100 | nF |
| $t_d$ | Delay of $V_{PP}$ from $V_{DD}$ at Power-on | max. 1 | sec. |
| $t_r$ | Rise time of $V_{PP}$ (during storage or reading) | 2 to 10 | $\mu$s |
| $r_s$ | Serial resistance of the ceramic resonator | max. 20 | $\Omega$ |

## BLOCK DIAGRAM

Fig. 1




## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at 5V and $T_{amb} = 25°C$

| Parameter | Pins | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{IL}$ Input Low Voltage | 2-3-4-5-6-7 | | | | 0.8 | V |
| | 25-26-27-28 | | | | 0.3 | |
| | 16-20-21-22 23-24 | | | | 1.5 | |
| $V_{IH}$ Input High Voltage | 2-3-4-5-6-7 | | 2 | | | V |
| | 25-26-27-28 | | 3 | | | |
| | 16-20-21-22 23-24 | | 3.5 | | | |
| $V_{OL}$ Output Low Voltage | 25-26-27-28 | $V_{DD}$ = 4.75V $I_{OL}$ = 1 mA | | | 3 | V |
| | 11-19 | $V_{DD}$ = 4.75V $I_{OL}$ = 5 mA | | | 1 | |
| | 2-17-18 | $V_{DD}$ = 4.75V $I_{OL}$ = 100 µA | | | 0.4 | |
| | 10 | $V_{DD}$ = 4.75V $I_{OL}$ = 2.5 mA | | | 8 | |
| $V_{OH}$ Output High Voltage | 2 | $V_{DD}$ = 4.75V $I_{OH}$ = -0.25 mA | 2.4 | | | V |
| | 17-18 | $V_{DD}$ = 4.75V $I_{OH}$ = -0.15 mA | 2.4 | | | |

## STATIC ELECTRICAL CHARACTERISTICS (continued)

| Parameter | Pins | Test conditions | | | Values Min. | Values Typ. | Values Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $I_{O(off)}$ Output Leakage Current | 25-26-27-28 | $V_{DD}$ = 5.25V $V_{O(off)}$ = 13.2V | | | | | 100 | µA |
| | 11-19 | $V_{DD}$ = 5.25V $V_{O(off)}$ = 13.2V | | | | | 50 | |
| | 10 | $V_{DD}$ = 4.75V $V_{O(off)}$ = 26V | | | | | 100 | |
| $I_{IL}$ Input Low Current | 3-4-5-6-7 16-22-23-24 | $V_{DD}$ = 5.25V $V_{IL}$ = 0.8V | | | | | -0.4 | mA |
| | 20-21 | $V_{DD}$ = 5.25V $V_{IL}$ = 1.5V | | | | | -0.4 | |
| | 2 | $V_{DD}$ = 5.25V $V_{IL}$ = 0.4V | | | | | -1.6 | |
| $I_{DD}$ Supply Current | 12 | $V_{DD}$ = 5.25V | | | | 20 | 50 | mA |
| $I_{PP}$ Memory Supply Current | 8 | $V_{PP}$ = 26V | Write | Peak | | | 40 | mA |
| | | | | Average | | | 11 | |
| | | | Erase | Peak | | | 7 | |
| | | | | Average | | | 4.5 | |
| | | | Read | Peak | | | 6 | |
| | | | | Average | | | 2 | |

## DESCRIPTION (all timings are given with $f_{ref}$ = 500 kHz)

The circuit description follows both pin sequence and pin function.

### Pin 1 – $V_{SS}$

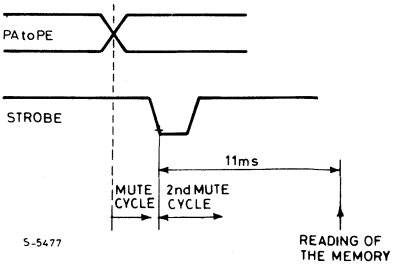
The substrate of the integrated circuit is connected to this pin.

### Pin 2 – Program strobe input/Mute input

**Program strobe input**

Although the program change is internally detected and the M 293 can also work with Remote Control receivers without any strobe output, the strobe function is useful, for example, to recall the stored tuning voltage after a search.
This input is active low and has an internal pull-up to 6 K (typ).
A second mute cycle restarts when the input goes low and the memory is read after 110 ms.

Fig. 2



**Mute output**

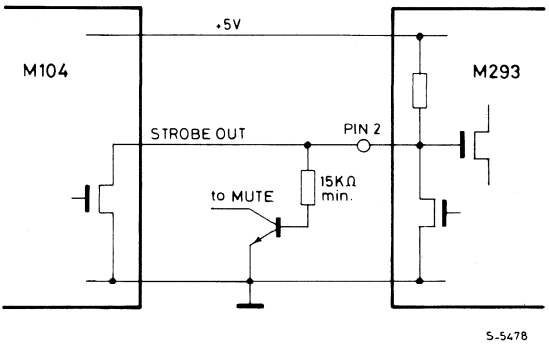
The output transistor is switched on when the Mute function is activated.
The Mute is present in the following cases:
- at band change
- at program change

} the Mute is active 110 ms before the esecution of the command and lasts 480 ms

- during automatic search

The Mute is active 110 ms before the start of the search
- when the supply voltage VDD is applied, for about 1 second
- when the supply voltage VDD is removed.

Fig. 3




## Pin 3-4-5-6-7- Program selection inputs

The programs are selected with a static 5 bit word according to the truth table given below. Input levels are TTL compatible. The inputs have an internal pull-up of 30K (typ.). The memory is read with a delay of 110 ms, after the strobe command or the program change.

| Program | PA | PB | PC | PD | PE |
|---|---|---|---|---|---|
| 1 | L | L | L | L | L |
| 2 | H | L | L | L | L |
| 3 | L | H | L | L | L |
| 4 | H | H | L | L | L |
| 5 | L | L | H | L | L |
| 6 | H | L | H | L | L |
| 7 | L | H | H | L | L |
| 8 | H | H | H | L | L |
| 9 | L | L | L | H | L |
| 10 | H | L | L | H | L |
| 11 | L | H | L | H | L |
| 12 | H | H | L | H | L |
| 13 | L | L | H | H | L |
| 14 | H | L | H | H | L |
| 15 | L | H | H | H | L |
| 16 | H | H | H | H | L |

| Program | PA | PB | PC | PD | PE |
|---|---|---|---|---|---|
| 17 | L | L | L | L | H |
| 18 | H | L | L | L | H |
| 19 | L | H | L | L | H |
| 20 | H | H | L | L | H |
| 21 | L | L | H | L | H |
| 22 | H | L | H | L | H |
| 23 | L | H | H | L | H |
| 24 | H | H | H | L | H |
| 25 | L | L | L | H | H |
| 26 | H | L | L | H | H |
| 27 | L | H | L | H | H |
| 28 | H | H | L | H | H |
| 29 | L | L | H | H | H |
| 30 | H | L | H | H | H |
| 31 | L | H | H | H | H |
| 32 | H | H | H | H | H |

## Pin 8 - Memory supply voltage

A supply voltage of 25 ± 1V has to be applied to this pin during the modify and read cycles.

### MODIFY CYCLE

A modify cycle consists of three steps:
1. All "1"s are written in the bits of the selected word.
2. All bits of the selected word are erased (all "0"s)
3. The new content is written.

In this way a constant aging of all the bits of the word is obtained.
During both write and erase cycles the memory situation is checked continuously; therefore after each write or erase pulse a read operation is carried out. The write or the erase operations are stopped as soon as the result of the read operation is valid.

#### Write cycle

The peak of the current flowing through pin 8 during a write operation is shown in fig. 4, while fig. 5 shows the envelope of the same current.
The typical write time is 3-4 ms for the first cycles and increase to about 30 ms after 1000 cycles.

Fig. 4

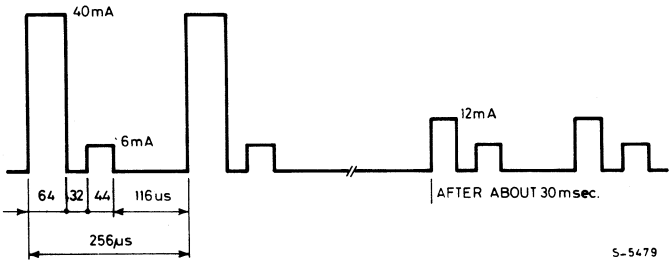
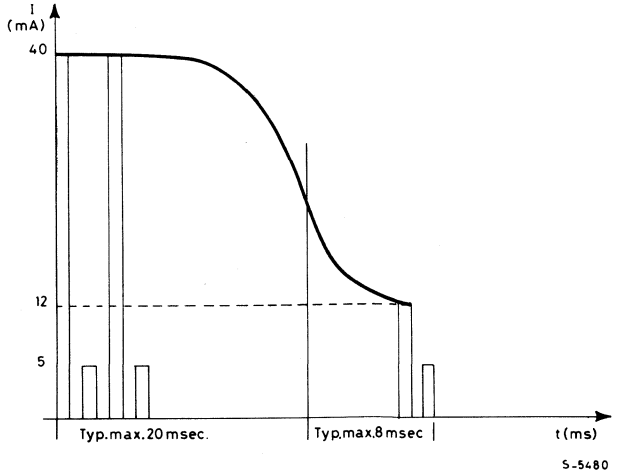


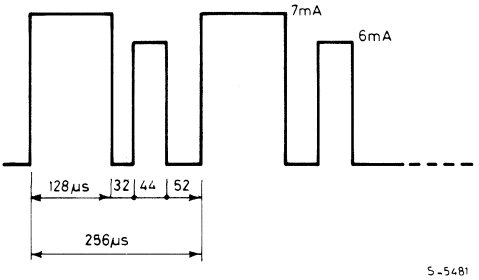

Fig. 5



**Erase cycle**

Fig.6 shows the timing and the waveform of the current flowing through pin 8 during the erase operation. The peak current is 7 mA (max) during the erase cycle and 6 mA (max) during the read cycle. The typical erase time is 10 ms for a new device and it increases with the number of modify operations up to 200 ms after 1000 cycles.

Fig. 6

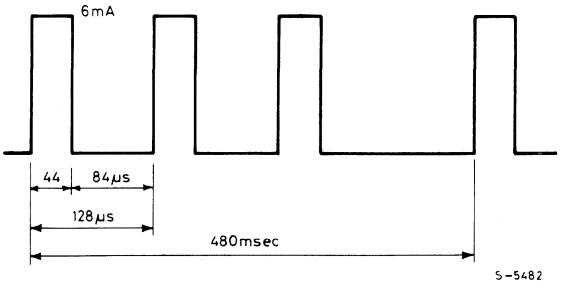



In order to protect the memory in case of failure of some bits the modify operation is stopped after 1 sec.

**READ CYCLE**

Fig. 7 shows the waveform of the current during a read operation.

Fig. 7




## Pin 9 - Search speed

An external RC network is connected to this pin in order to set the frequency of the internal oscillator which, in turn, sets the scan speed during search.
The search speed ratios in the bands are explained in the description of pins 22, 23, 24 (UP/DOWN Manual) and of pins 20 and 21.

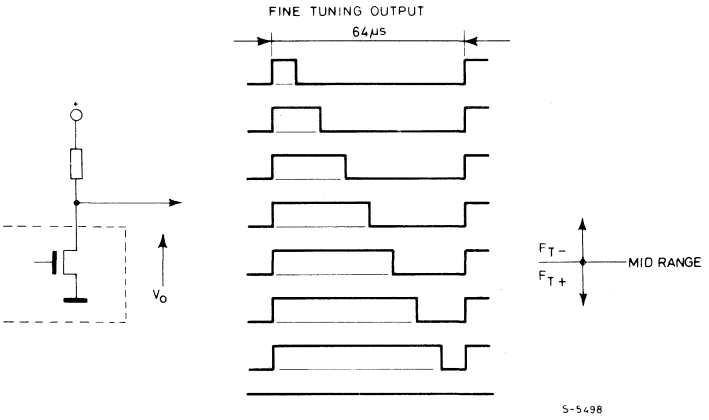
## Pin 10 - Memory timing output

This output gives the timing for the pulses to be applied at pin 8 during the modify and read cycles. The output consists of an open drain transistor.

## Pin 11 - Fine tuning out

Fine tuning information is available on this pin in the form of a square wave having a frequency of 15.625 Hz and duty cycle variable in 8 positions as indicated in fig. 8.

Fig. 8




The voltage generated after filtering is fed to the AFC loop and detunes the receiver by a small $\Delta f$ while maintaining the action of the AFC.
The Fine tuning function operates as follows:
- At the start of the search (Auto or Manual) the output is set at mid range (see fig. 8).
- When the search has been completed it is possible to operate on the FINE TUNING+/−commands. The STORE command memorizes this information together with the 12 tuning voltage and 2 bit band information.
- When a memorized channel is recalled it is possible to act on the FINE TUNING commands.

Any change in Fine tuning is memorized only by the STORE command. The output circuit consists of an open drain transistor.

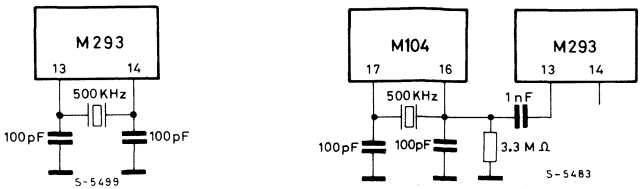
## Pin 12 - $V_{DD}$

This pin has to be connected to a 5V ± 0.25V supply.
When the $V_{DD}$ is applied to this pin an internal power on reset of 1 sec is generated: therefore, for a correct reading of the memory, the $V_{PP}$ supply voltage must reach the value of 25V within 1 sec after the presence of $V_{DD}$.

## Pin 13-14 - Oscillator

The internal oscillator operates with a cheap 445 to 510 kHz ceramic resonator connected as shown in fig. 9.
If an external oscillator is used, the signal to be applied must be 0.5 $V_{PP}$ min.

Fig. 9



## Pin 16 - Automatic/Manual search mode selection

This pin is used to change the search mode. When it is connected to $V_{DD}$ the system works in Automatic mode; when it is connected to $V_{SS}$ the system works manually.
The change Auto-Manual or viceversa can be made at any time without affecting other circuit functions.
The input has an integrated pull-up of 30 KΩ (typ).

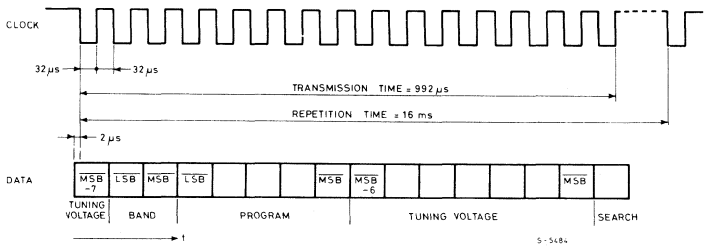
## Pin 17 - Data output for external display (M 191)

A 16 bit burst is available on this pin. It contains the 8 MSB of the digitized tuning voltage, 2 bits for band information, 5 bits for program information and 1 bit which indicates that the system is in the search mode (both Automatic or Manual). The display is also enabled at the band change.
These outputs are active low and incorporate a 10 KΩ (typ.) pull-up resistors.

## Pin 18 - Clock output for external display (M 191)

A burst containing 16 clock pulses is available on this pin. This clock pulses are synchronized with Data Information as described in fig. 10.
A pull-up of 10 KΩ (typ.) is integrated.

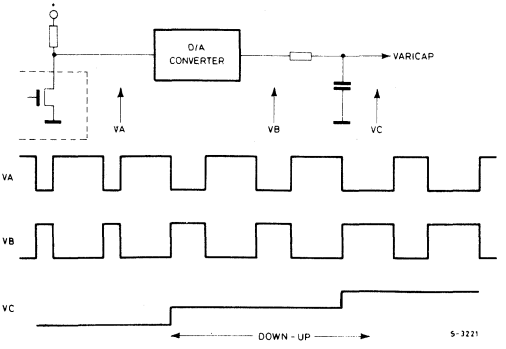
Fig. 10




## Pin 19 - Tuning voltage out

A $2^{13} = 8192$ step pulse modulated signal for the tuning voltage is available on this pin.
Pulse modulation is implemented by combination of a rate multiplier and pulse width principle.
With a tuning voltage increasing from zero, the number of pulses increases continuously up to $2^8 = 256$; starting from this point the number of pulses remains the same but the pulses get larger until they reach the maximum content of the internal counter. The output consists of an open drain transistor which offers a low impedance to ground when in the ON state.

Fig. 11



## Pin 20-21 - STOP/AFC

These pins are used only in automatic search mode.
When the M293 is in manual operation these pins are disabled internally.
The STOP/AFC inputs are also disabled internally during any program or band change for the duration of the Mute signal.
These pins work according to the truth table given below:

| M293 pin 20<br>TDA4433 pin2 | M293 pin 21<br>TDA4433 pin 6 | FUNCTION<br>(referred to the tuning voltage) |
|---|---|---|
| H | L | UP |
| L | H | DOWN |
| L | L | MIDDLE |
| H | H | NO OPERATION |

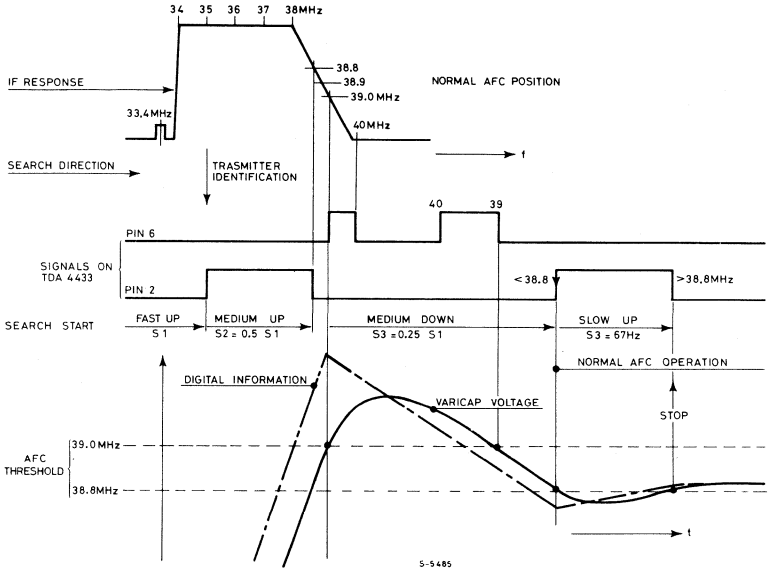
These inputs have two different functions depending on whether the system is in the search or in normal operation (AFC control).
The inputs have internal pull-up resistors of 30 KΩ typ.(10 KΩ min).

A) **Search mode:** after depressing the Search start key, the levels of the signals coming from the TDA 4433, applied to these pins, control the search function and determine when the search must stop, i.e. a TV station has been recognized.
The circuit operates in the following sequence (see fig. 12 for reference and explanation of pins 22, 23, 24 for definition):
1 – after pressing the search start key the search occurs in the FAST UP mode.
2 – eventual transitions available on these inputs are ignored during the first 15 search steps if the system is in the UHF or CATV bands.
If the system operates in VHF I and III the first 60 search steps are ignored. The acceptance delay of 15 (60) search steps has been introduced to prevent the system from stopping at the previous station (for example if the search start command has been given just before an AFC control command)
After this time the FAST UP speed is automatically reduced to half during each UP signal (MEDIUM UP = FAST UP/2).
A DOWN signal preceded by at least an UP signal will set the search to MEDIUM DOWN mode (FAST UP/4).
3 – the next UP signal will switch the search to SLOW UP speed (61 Hz).
At this point the system is in normal AFC operation.

B) **AFC operation:** when a station is perfectly tuned, the input signals coming from TDA 4433 are at tuning condition.
If the tuning moves lower than the threshold below 38.9 MHz, the pin 20 is put H and pin 21 is put L; the 13 bit internal counter is moved with SLOW UP speed to increase the varicap voltage.
When a detuning occurs in the opposite direction the input 20 goes low and 21 goes high and the tuning voltage is decreased with VERY SLOW DOWN speed (7.6 Hz).
The increase or decrease of the tuning voltage is stopped as soon as the input returns to middle conditions.
Therefore during normal operation pins 20 and 21 act as the AFC control command.

C) **Recall from memory:** when the circuit is in automatic mode and a pre-memorized program is recalled from Memory, a fixed value of 8 steps (~ 31.2 mV) is subtracted from the tuning voltage.
This corresponds to a detuning of 0.6 MHz (UHF) and of 0.3 MHz in VHF III into that part of the IF response curve which corresponds to the fully transmitted sideband.
At this point the AFC operation takes over as described in point B above and the exact tuning is achieved in about 0.2 sec.
This feature increases the AFC capture range and relaxes the stability requirements of the tuner, voltage references and the D/A converter.

Fig. 12



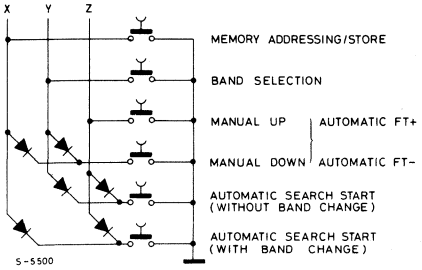

## Pins 22-23-24 Control inputs X - Y - Z

The M 293 accepts binary coded commands as follows:

| X | Y | Z | Function |
|---|---|---|---|
| H | H | H | ——————— |
| L | H | H | Memory addressing / Store |
| H | L | H | Band selection |
| H | H | L | Manual mode (pin 16L) { UP / DOWN Automatic mode (pin 16H) { FT + / FT − |
| L | L | H | |
| H | L | L | Automatic search start (without band change) |
| L | H | L | Automatic search start (with band change) |

The inputs have integrated pull-up resistors of 30 KΩ (typ.). Commands are accepted after 30 ms of continuous presence. A new command is not accepted until the previous one has been released.

Fig. 13



**Memory addressing / Store**

The normal sequence of program storage (program selection, search, store, new program selection and so on) can be changed in order to have the possibility to select the memory position (program number) after the search.
In this way the search is faster and continuous through the bands.
When the key is pressed it is possible to select the memory position. When the key is released the store function is activated (with 30 ms of acceptance time).
The proposed sequence of tuning and storage is as described below:

| Step | Operation |
|---|---|
| 1 | Tune in station (manually or automatically) |
| 2 | Press "Memory addressing / Store" key and hold it pressed |
| 3 | Select the program where the tuning is to be stored |
| 4 | Release the "Memory addressing / Store" key<br>At this moment 12 bits of the digitized tuning voltage, 2 bits for band and 3 bits relative to Fine Tuning are stored |

If this solution for memory addressing/store is not used, memorization will occur at the release of the key in the memory position previously selected.
This command is disabled during the Automatic search, During the store cycle any other operation is blocked. Only the program change command is stored internally and executed when the store cycle is over.
In order to protect the memory the store function is disabled internally after one store cycle. It is enabled after a program change or a tuning operation (it is not disabled by the AFC control).

**Band selection**

The bands can be step-by-step selected with the following sequence:

| | DATA BUS | |
|---|---|---|
| Band | MSB | LSB |
| VHF III | L | L |
| UHF | L | H |
| VHF I | H | L |
| CATV | H | H |

Only one band change is performed at each accepted command.
Disabled bands are automatically skipped. A band can be disable by connecting the corresponding output to VSS.

**Manual mode UP/DOWN**
**Automatic mode FT+/FT–**

The function of this pin depends on the search mode that is determine by pin 11.

**Manual:** when a command is accepted the search begins at low speed. One second later, the search speed is increased and it reaches the maximum value after 3 seconds

| Search speed | Time |
|---|---|
| ÷ 8 | Command accepted |
| ÷ 4 | After 1 second |
| ÷ 2 | After 2 seconds |
| ÷ 1 | After 3 seconds |

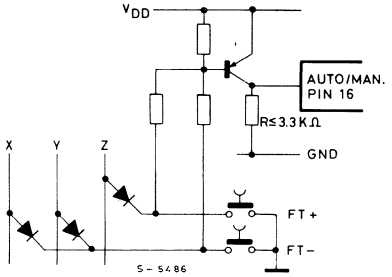
The search is correlated to the selected band as follows:
Max search speeds:

Bands VHF I and VHF III : external rate divided by 3
Bands UHF and CATV : external rate divided by 12

When the end of the band is reached the search restarts from the beginning of the same band after a delay of 480 ms.

**Automatic fine tuning** +/– : when the command is accepted, the PWM signal present at the fine tuning output (pin 11) is changed at the rate of one step every 480 ms.
at the rate of one step every 480 ms.
Fine tuning is manual mode is possible switching temporarily the system to automatic modes as shown in fig. 14.

Fig. 14




**Automatic Search** (without band change)

When the command is accepted the search starts on the selected band. When the end of the band is reached the search restarts from the beginning of the same band after a delay of 480 ms.
If the key is held depressed another search can start only if the key is released and connected again to VSS.
During the search the tuning voltage is always changing from lower to higher voltage levels. The search is automatically stopped when the first station is found.
The search is also stopped whenever a program selection command is given.
The search speed is determined by the RC network connected to pin 17 and is correlated to the band.
UHF and CATV bands are scanned with the rate fixed externally divided by 4.
VHF bands are scanned with the rate fixed externally.
During the STOP sequence the search speed is automatically reduced as defined in the explanation of pins 20 and 21.

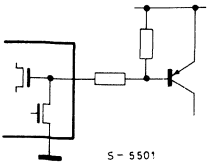
**Automatic Search** (with band change)

The search is effected starting from the tuning position.
When the end of band is reached, the band is automatically changed in the sequence described at pins 22-23-24 (Band selection command). Disabled bands are automatically skipped.

## Pins 25-26-27 - Band outputs/inputs

These outputs are provided to select up to 4 bands via external PNPs.
If one or more bands have to be skipped, the corresponding outputs have to be short-circuited to $V_{SS}$.

Fig. 15

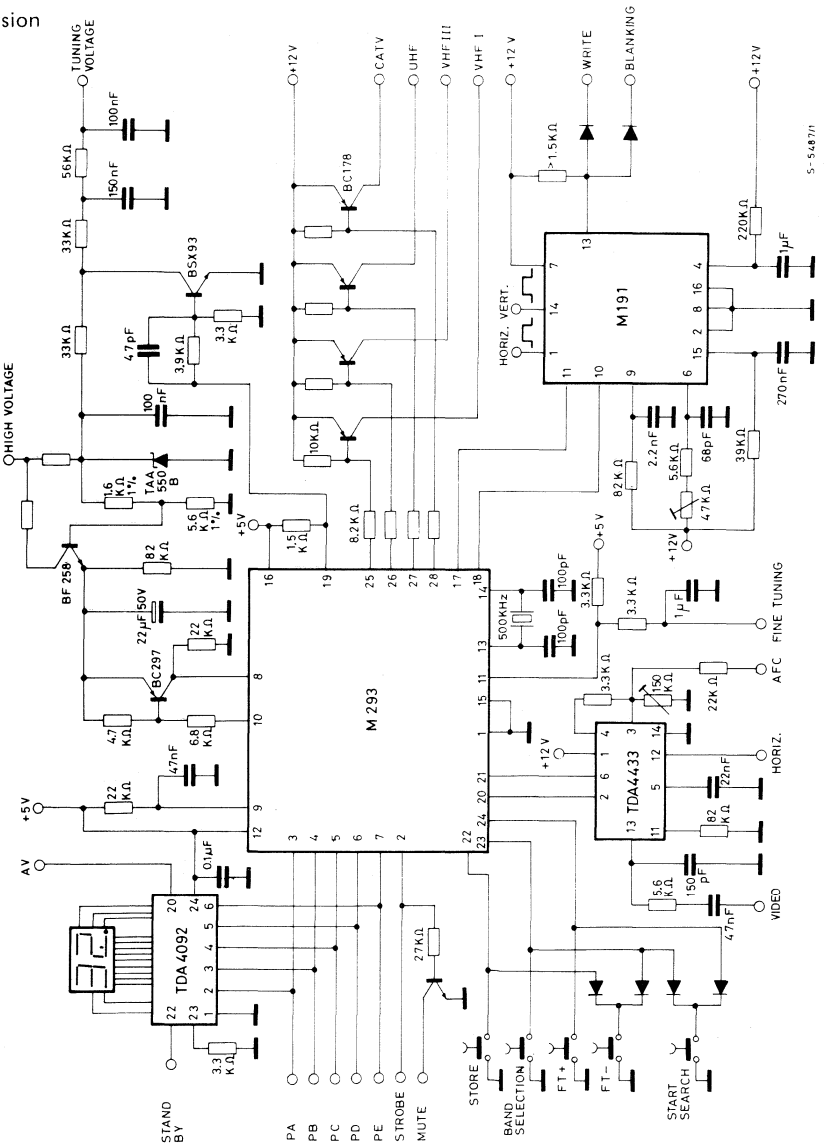



The relation between pins and bands are as follows:

pin 25 = VHF I
pin 26 = VHF III
pin 27 = UHF
pin 28 = CATV

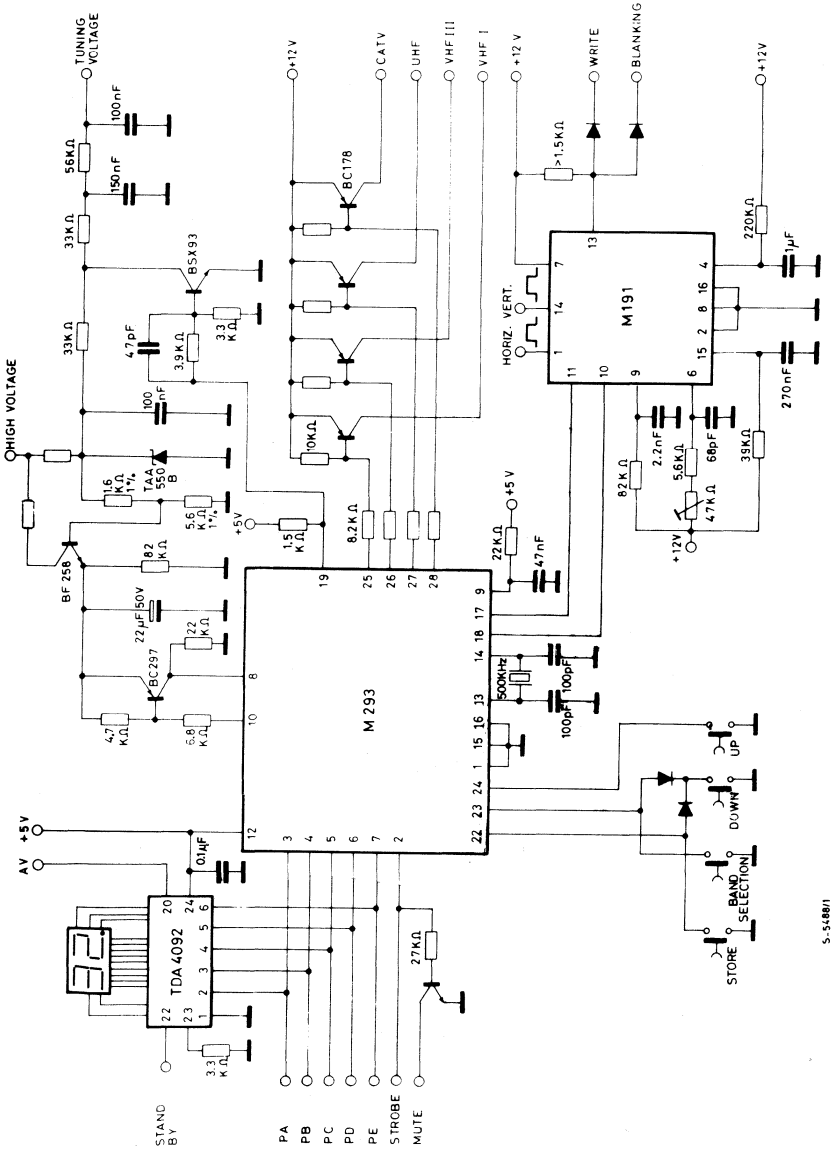
## TYPICAL APPLICATIONS

Automatic Version



## TYPICAL APPLICATIONS (continued)

Manual Version



**PRELIMINARY DATA**

## SINGLE CHIP NON VOLATILE STATION MEMORY, PCM REMOTE CONTROL RECEIVER AND DISPLAY DRIVER

- M490 16 STATION MEMORY – SINGLE DOT LED DISPLAY
- M491 16 STATION MEMORY – 7 SEGMENT LED DISPLAY
- VOLTAGE SYNTHESIZER: 13 BITS
- 4 BAND PRESET CAPABILITY
- NON VOLATILE MEMORY: 304 BITS
  - 16 WORDS OF 19 BITS FOR TUNING VOLTAGE (13 BITS) – BAND (2 BITS) – FINE DETUNING (4 BITS)
  - $10^4$ MODIFY CYCLES PER WORD
  - MIN 10 YEARS DATA RETENTION
- PCM REMOTE CONTROL RECEIVER: DECODES SIGNAL TRANSMITTED BY M708
- VOLUME D/A: 6 BIT RESOLUTION/8 KHz
- MEMORY SKIP FUNCTION
- AUTOMATIC SEARCH WITH DIGITAL AFT CONTROL
- FINE DETUNING D/A ACTING ON AFT DISCRIMINATOR (16 STEPS) WITH SEPARATE STORAGE FOR EACH MEMORY POSITION. ALTERNATIVELY IT CAN BE USED TO CONTROL BRIGHTNESS OR COLOUR SATURATION
- MANUAL SEARCH WITH DIGITAL AFT CONTROL
- MANUAL SEARCH WITH LINEAR AFT
- SWEEP SEARCH DISPLAY OUTPUT
- SUPPLY VOLTAGES: $V_{DD}$ = +5V
  $V_{PP}$ = +25V FOR THE MEMORY
- CLOCK OSCILLATOR: 445 TO 510 KHz
- INTEGRATED DIGITAL POWER ON RESET (NO EXTERNAL INITIALIZATION CIRCUITRY REQUIRED)

The M490 and M491 are monolithic N-MOS LSI circuits including a Floating-gate Non Volatile Memory for storage of up to 16 stations. Tuning of the station is performed with a 8192 step D/A converter, using the principle of voltage synthesis.
The M490 is designed to drive single dot LED displays (one LED is necessary for each used memory position). Direct and Up/Down memory selection is possible on the set or from remote control. Memory positions 11 to 16 can be skipped in case of Up/Down commands.
The M491 is designed for 7 segment LED displays. Direct memory selection is possible only from remote control while Up/Down memory scanning is possible on the set and also from remote control. An option input for 8 or 16 stations is available.
The circuits also include a PCM remote control receiver operating in conjunction with the transmitter M708. The highly reliable transmission code ensures error free signal detection even in presence of high noise conditions.
Search of the station is possible in automatic or manual modes. The circuit can operate with a Digital or Linear AFT control.
The Digital AFT mode is necessary for automatic search and requires an external circuit (TDA 4433 or equivalent, e.g. dual comparator plus TV station detector) to convert the AFC-S-curve into a Up/Down command.
Fine tuning (detuning) is also possible with different modes of operation.
The circuits are assembled in a 40 pin dual in-line plastic package.

**ORDERING NUMBERS:** M490 B1
M491 B1

# M490
# M491

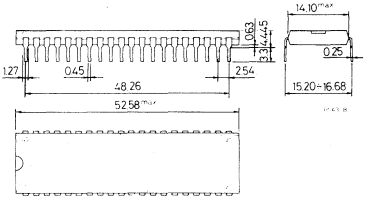
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 7 | V |
| $V_{PP}$ | Memory supply voltage | -0.3 to 28 | V |
| $V_I$ | Input voltage | -0.3 to 15 | V |
| $V_{O(off)}$ | Off state input voltage (except pin 3) | 15 | V |
| | pin 3 | 28 | V |
| $I_{OL}$ | Output low current | | |
| | Led Driver Outputs } M490 | 25 | mA |
| | Led Driver Outputs } M491 | 20 | mA |
| | Pins 6-14 | 20 | mA |
| | Pins 4-5 | 7.5 | mA |
| | All other outputs | 5 | mA |
| $t_{pd}$ | Max delay between memory timing and memory supply pulses | 5 | µs |
| $P_{tot}$ | Total package power dissipation | 1 | W |
| $T_{stg}$ | Storage temperature | -25 to 125 | °C |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

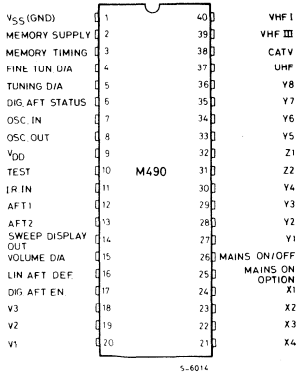
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

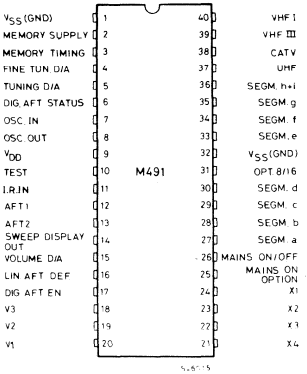
## MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package




## PIN CONNECTIONS



## BLOCK DIAGRAMS

Fig. 1

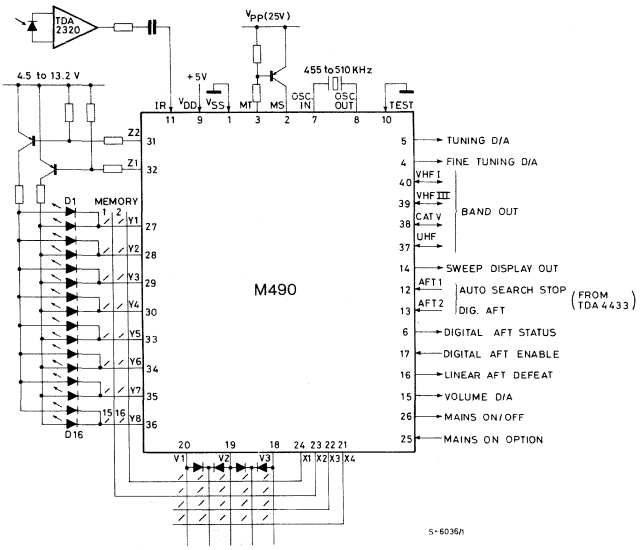
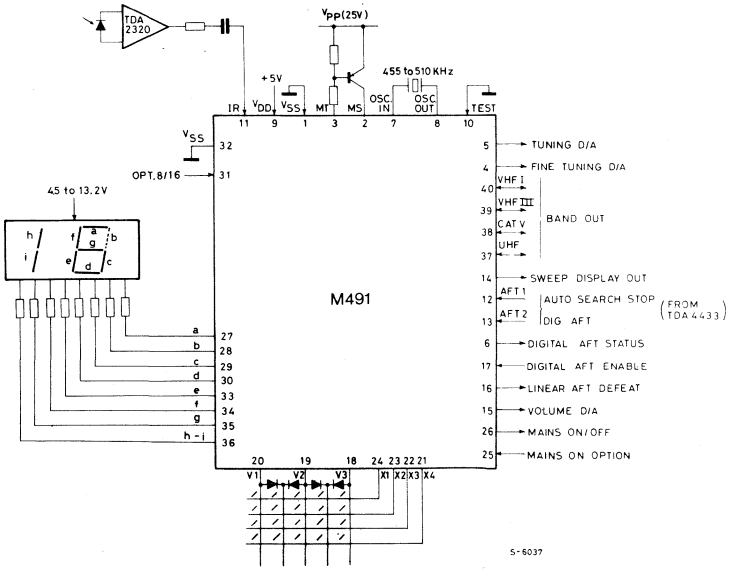



Fig. 2



## M490 STATIC ELECTRICAL CHARACTERISTICS ($T_{amb}$= 0 to 70°C, $V_{DD}$= 5V unless otherwise specified)

| Pins | Parameter | | Test conditions | | Values | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| 2 - Memory Supply | $I_{PP}$ | Memory Supply Current | $V_{PP}$= 26V | | | | | |
| | | | Write | Peak | | | 42 | mA |
| | | | | Average | | | 12 | mA |
| | | | Erase | Peak | | | 9 | mA |
| | | | | Average | | | 5 | mA |
| | | | Read | Peak | | | 8 | mA |
| | | | | Average | | | 2.5 | mA |
| | R | Pull down resistor | | | | | 25 | KΩ |
| 3 - Write Timing Out | $V_{OL}$ | Output Low Voltage | $V_{DD}$= 4.75V | $I_{OL}$= 2.5 mA | | | 8 | V |
| | $I_{O(off)}$ | Output Leakage Current | $V_{DD}$= 4.75V | $V_{OUT}$= 26V | | | 100 | µA |
| 4 - Fine Tuning D/A | $I_{O(off)}$ | | $V_{DD}$= 5.25V | $V_{O(off)}$= 13.2V | | | 50 | µA |
| 5 - Tuning D/A | $V_{OL}$ | | $V_{DD}$= 4.75V | $I_{OL}$= 5 mA | | | 1 | V |
| 6 - Digital AFT Out | $V_{OL}$ | | $V_{DD}$= 4.75V | $I_{OL}$= 20 mA | | | 1.5 | V |
| | $I_{O(off)}$ | | $V_{DD}$= 5.25V | $V_{O(off)}$= 13.2V | | | 100 | µA |
| 9 - Power Supply | $I_{DD}$ | Supply Current | $V_{DD}$= 5.25V | | | | 100 | mA |
| 11 - I.R. Input | $V_{IPP}$ | Peak to peak voltage | | | 0.5 | | 13.2 | V |
| 12 - AFT 1<br>13 - AFT 2 | $V_{IL}$ | Input Low Voltage | $V_{DD}$= 5.25V | | | | 1.5 | V |
| | $V_{IH}$ | Input High Voltage | $V_{DD}$= 5.25V | | 3.5 | | | V |
| | $I_{IL}$ | Input Low Current | $V_{DD}$= 5.25V | $V_{IL}$= 1.5V | | | -0.4 | mA |
| | R | Pull-up resistor | | | | 30 | | KΩ |
| 14 - Display Out | $V_{OL}$ | | $V_{DD}$= 4.75V | $I_{OL}$= 20 mA | | | 1.5 | V |
| | $I_{O(off)}$ | | $V_{DD}$= 5.25V | $V_{O(off)}$= 13.2V | | | 100 | µA |
| 15 - Volume D/A | $V_{OL}$ | | $V_{DD}$= 4.75V | $I_{OL}$= 4 mA | | | 1 | V |
| | $I_{O(off)}$ | | $V_{DD}$= 5.25V | $V_{O(off)}$= 13.2V | | | 50 | µA |
| 16 - Linear AFT Out | $V_{OL}$ | | $V_{DD}$= 4.75V | $I_{OL}$= 1 mA | | | 0.4 | V |
| | $I_{O(off)}$ | | $V_{DD}$= 5.25V | $V_{O(off)}$= 13.2V | | | 50 | µA |
| 17 - Digital AFT Enable | $V_{IL}$ | | | | | | 0.8 | V |
| | $V_{IH}$ | | | | 2.0 | | | V |
| | $I_{IL}$ | | $V_{DD}$= 5.25V | $V_{IL}$= 0.8V | | | -0.4 | mA |
| | R | Pull-up resistor | | | | 30 | | KΩ |

## M490 STATIC ELECTRICAL CHARACTERISTICS (continued)

| Pin | Parameter | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| 18-19-20 V3 V2 V1 Keyboard In | $V_{IL}$ | | | | 1.5 | V |
| | $V_{IH}$ | | 3.5 | | | V |
| | $I_{IL}$ | $V_{DD}$= 5.25V $V_{IL}$= 0.8V | | | -0.4 | mA |
| | R Pull-up resistor | | | 30 | | KΩ |
| 21-22-23-24 X4 X3 X2 X1 Keyboard Out | $V_{OL}$ | $V_{DD}$= 4.75V $I_{OL}$= 1 mA | | | 0.4 | V |
| | $I_{O(off)}$ | $V_{O(off)}$= 5.5V | | | 25 | μA |
| 25 - Mains on Enable | $V_{IL}$ | | | | 0.8 | V |
| | $V_{IH}$ | | 2.4 | | | V |
| | $I_{IL}$ | $V_{DD}$= 5.25V | | | -0.4 | mA |
| | R Pull-up resistor | $V_{IL}$= 0.8V | | 30 | | KΩ |
| 26 - Mains On/Off | $V_{OL}$ | $V_{DD}$= 4.75V $I_{OL}$= 100 μA | | | 0.4 | V |
| | $I_O$ | $V_{DD}$= 4.75V $V_O$= 0.7V | -1.6 | | | mA |
| 27-28-29-30-33-34-35-36 Keyboard In and Display Out | $V_{IL}$ | | | | 1.5 | V |
| | $V_{IH}$ | | 3.5 | | | V |
| | $I_{IL}$ | $V_{DD}$= 5.25V $V_{IL}$= 0.8V | | | -0.5 | mA |
| | R Pull-up resistor | | | 30 | | KΩ |
| | $V_{OL}$ | $V_{DD}$= 4.75V $I_{OL}$= 20 mA | | | 1.5 | V |
| 31 - Z2 32 - Z1 MPX for Display Out | $V_{OL}$ | $V_{DD}$= 4.75V $I_{OL}$= 1 mA | | | 0.4 | V |
| | $I_{O\ (off)}$ | $V_{DD}$= 5.25V $V_{O\ (off)}$= 13.2V | | | 50 | μA |
| 37 - UHF 38 - CATV 39 - VHFIII 40 - VHFI BAND | $V_{OL}$ | $V_{DD}$= 4.75V $I_{OL}$= 1 mA | | | 3 | V |
| | $V_{OH}$ | $V_{DD}$= 4.75V $I_{OH}$= -150 μA | 2.4 | | | V |
| | $V_{IL}$ | | | | 0.3 | V |
| | $V_{IH}$ | | 3 | | | V |
| | $I_{O\ (off)}$ | $V_{DD}$= 5.25V $V_{O\ (off)}$= 13.2V | | | 50 | μA |

### M491: ALL PINS AS FOR M490 WITH EXCEPTION OF:

| | | | | | | |
|---|---|---|---|---|---|---|
| 27-28-29-30 33-34-35 Display Out | $V_{OL}$ | $V_{DD}$= 4.75V $I_{OL}$= 20 mA | | | 1.5 | V |
| 36-Display Out | $V_{OL}$ | $V_{DD}$= 4.75V $I_{OL}$= 30 mA | | | 1.5 | V |
| 31 - Memory 8/16 | $V_{IH}$ | | 2.0 | | | V |
| | $V_{IL}$ | | | | 0.8 | V |

## DESCRIPTION (timings are with $f_{clock}$ = 500 KHz)

### Pin 1 – $V_{SS}$

The substrate of the IC is connected to this pin. It is reference pin for all parameters of the IC.

### Pin 2 – Memory supply voltage

A supply voltage of 25 ± 1V has to be applied to this pin during the modify and read cycles.

#### MODIFY CYCLE

A modify cycle consists of three steps:
1. All "1"s are written in the bits of the selected word.
2. All bits of the selected word are erased (all "0"s)
3. The new content is written.

In this way a constant aging of all the bits of the word is obtained.
During both write and erase cycles the memory situation is checked continuously; therefore after each write or erase pulse a read operation is carried out. The write or the erase operations are stopped as soon as the result of the read operation is valid.

#### Write Cycle

The peak of the current flowing through pin 2 during a write operation is shown in fig. 3, while fig. 4 shows the envelope of the same current.
The typical write time is 3-4 ms for the first cycles and increases to about 30 ms after 1000 cycles.

Fig. 3

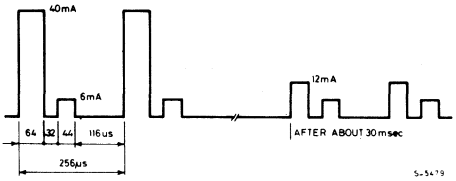
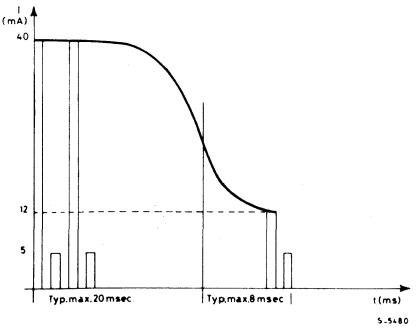


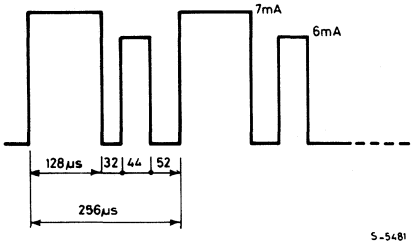

Fig. 4



**Erase Cycle**

Fig. 5 shows the timing and the waveform of the current flowing through pin 2 during the erase operation. The peak current is 7 mA (max) during the erase cycle and 6 mA (max) during the read cycle. The typical erase time is 10 ms for a new device and it increases with the number of modify operations up to 200 ms after 1000 cycles.

Fig. 5

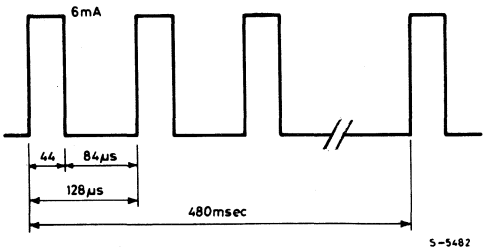



In order to protect the memory in case of failure of some bits the modify operation is stopped after 1 sec.

**READ CYCLE**

Fig. 6 shows the waveform of the current during a read operation.

Fig. 6



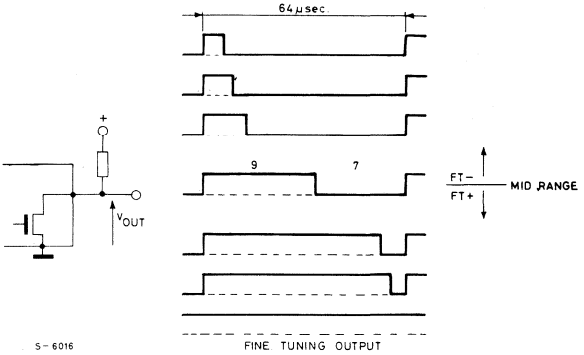

## Pin 3 – Memory timing output

This output gives the timing for the pulses to be applied at pin 2 during the modify and read cycles. The output consists of an open drain transistor.

## Pin 4 – Fine tuning D/A

A D/A converter with 16 step resolution and a frequency of 15 KHz can be used to generate a voltage which, if fed to a varicap diode in parallel to the AFC discriminator, will detune the receiver by a small $\Delta f$ while maintaining the action of the Digital AFT. This output can be used in conjunction with both Linear and Digital AFT modes of operations.

Fig. 7



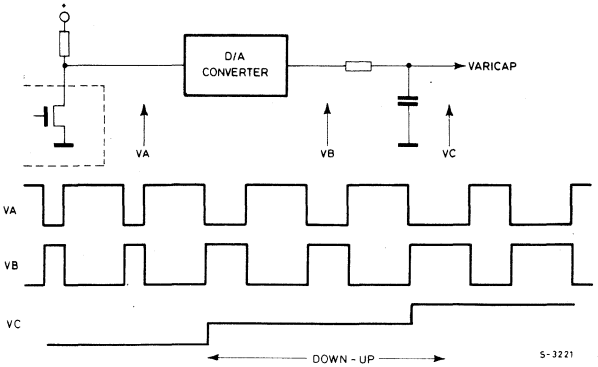

The Fine tuning function operates as follows:

- At the start of any automatic or manual search, the output is set at the mid range.
- When the search has been completed it is possible to operate on FT +/− commands. The store command memorizes this information together with the 13 tuning voltage and 2 bit and information.
- Modification time of FT D/A is of 1 step every 200 ms if issued locally or every 2 received signals from Remote control transmitter.

## Pin 5 – Tuning D/A

A $2^{13} = 8192$ step pulse modulated signal for the tuning voltage is available on this pin.
Pulse modulation is implemented by combination of a rate multiplier and pulse width principle.
With a tuning voltage increasing from zero, the number of pulses increases continuously up to $2^8 = 256$; starting from this point the number of pulses remains the same but the pulses get larger until they reach the maximum content of the internal counter. The output consists of an open drain transistor which offers a low impedance to ground when in the ON state.

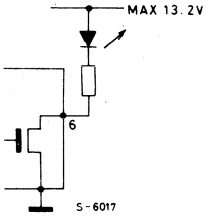
Fig. 8




## Pin 6 – Digital AFT status output

This output shows the status of the digital AFT. It is low when the digital AFT is enabled and it can directly drive a LED.
The output consists of an open drain transistor.

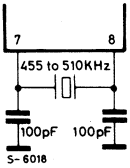
Fig. 9




## Pins 7-8 – Oscillator Input/Output

The frequency of the clock oscillator should be between 445 and 510 kHz using a cheap ceramic resonator. In these conditions the value of the reference frequency of the transmitter can be in the same range. In other words the transmitter and the receiver can operate with different reference frequencies.

Fig. 10




## Pin 9 – $V_{DD}$

The supply voltage has to be comprised in the range 4.75 to 5.25V. When it is applied an internal power on reset of 0.5 s is generated.
The memory position 1 is automatically read if the mains on option input (pin 25) is grounded.

## Pin 10 – Test

This pin is used for testing and has to be connected to $V_{SS}$.

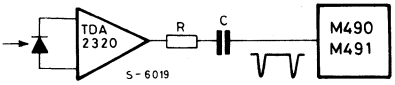
## Pin 11 – I.R. Signal Input

The integrated receiver decodes signals transmitted by M708, address 9.
The minimum signal to be applied is 0.5V peak to peak.(AC coupled).
The receiver input section performs the following tests on the incoming signal to achieve the necessary noise immunity:
- measurement of the pulse distance (time base synchronization)
- check of the position of the received bits opening window at the time bases
- check of the parity bit
- check of the absence of pulses between the parity bit and the stop-pulse
- check of noise level; the receiver checks parasitic transient inside and outside the time windows.

If the above test conditions are not fulfilled, the received word is rejected and not decoded. If the received signal is acknowledged as a valid word it is stored and decoded.

The end of transmission will be acknowledged by receiving the end of transmission code or by means of an internal timer if the transmission remains interrupted for more than about 550 ms.

Fig. 11




| SUPPLY VOLTAGE OF TDA 2320 | R | C |
|---|---|---|
| 5 | 2.2K | 4.7 nF |
| 12 | 10K | 4.7 nF |

## M490/M491 REMOTE CONTROL RECEIVER TRUTH TABLE. TRANSMITTER M708; ADDRESS CODE N° 8

| Command No. | I.R. CODE C1 | C2 | C3 | C4 | C5 | C6 | Function |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | End of Transmission |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | Power On/Off |
| 2 | 1 | 1 | 0 | 0 | 0 | 0 | Mute On/Off |
| 3 | 0 | 0 | 1 | 0 | 0 | 0 | Memory 1 |
| 4 | 1 | 0 | 1 | 0 | 0 | 0 | Memory 2 |
| 5 | 0 | 1 | 1 | 0 | 0 | 0 | Memory 3 |
| 6 | 1 | 1 | 1 | 0 | 0 | 0 | Memory 4 |
| 7 | 1 | 0 | 0 | 0 | 1 | 0 | Fine Tuning Up |
| 8 | 1 | 1 | 0 | 0 | 1 | 0 | Fine Tuning Down |
| 9 | 0 | 0 | 1 | 0 | 1 | 0 | Memory 5 |
| 10 | 1 | 0 | 1 | 0 | 1 | 0 | Memory 6 |
| 11 | 0 | 1 | 1 | 0 | 1 | 0 | Memory 7 |
| 12 | 1 | 1 | 1 | 0 | 1 | 0 | Memory 8 |
| 13 | 1 | 0 | 0 | 0 | 0 | 1 | Memory Up |
| 14 | 1 | 1 | 0 | 0 | 0 | 1 | Memory Down |
| 15 | 0 | 0 | 1 | 0 | 0 | 1 | Memory 9 |
| 16 | 1 | 0 | 1 | 0 | 0 | 1 | Memory 10 |
| 17 | 0 | 1 | 1 | 0 | 0 | 1 | Memory 11 |
| 18 | 1 | 1 | 1 | 0 | 0 | 1 | Memory 12 |
| 19 | 1 | 0 | 0 | 0 | 1 | 1 | Man. Search Up |
| 20 | 1 | 1 | 0 | 0 | 1 | 1 | Man. Search Down |
| 21 | 0 | 0 | 1 | 0 | 1 | 1 | Memory 13 |
| 22 | 1 | 0 | 1 | 0 | 1 | 1 | Memory 14 |
| 23 | 0 | 1 | 1 | 0 | 1 | 1 | Memory 15 |
| 24 | 1 | 1 | 1 | 0 | 1 | 1 | Memory 16 |
| 25 | 1 | 0 | 0 | 1 | 1 | 1 | Volume Up } Mute |
| 26 | 1 | 1 | 0 | 1 | 1 | 1 | Volume Down } Off |
| 27 | 0 | 0 | 1 | 1 | 1 | 1 | Memory Addressing 1 |
| 28 | 1 | 0 | 1 | 1 | 1 | 1 | Digital AFT On |
| 29 | 0 | 1 | 1 | 1 | 1 | 1 | Band Sequential |
| 30 | 1 | 1 | 1 | 1 | 1 | 1 | Automatic Search |

## Pin 12-13 – AFT1-AFT2 (STOP/AFT Inputs)

These pins are enabled during the automatic search and during normal operation, when the digital AFT is enabled (see description of pin 17)
The STOP/AFT inputs are also disabled internally during any program or band change for the duration of the Mute signal.
These pins work according to the truth table given below:

| M49X pin 12<br>TDA4433 pin 2 | M49X pin 13<br>TDA4433 pin 6 | FUNCTION<br>(referred to the tuning voltage) |
|---|---|---|
| H | L | UP |
| L | H | DOWN |
| L | L | MIDDLE |
| H | H | NO OPERATION |

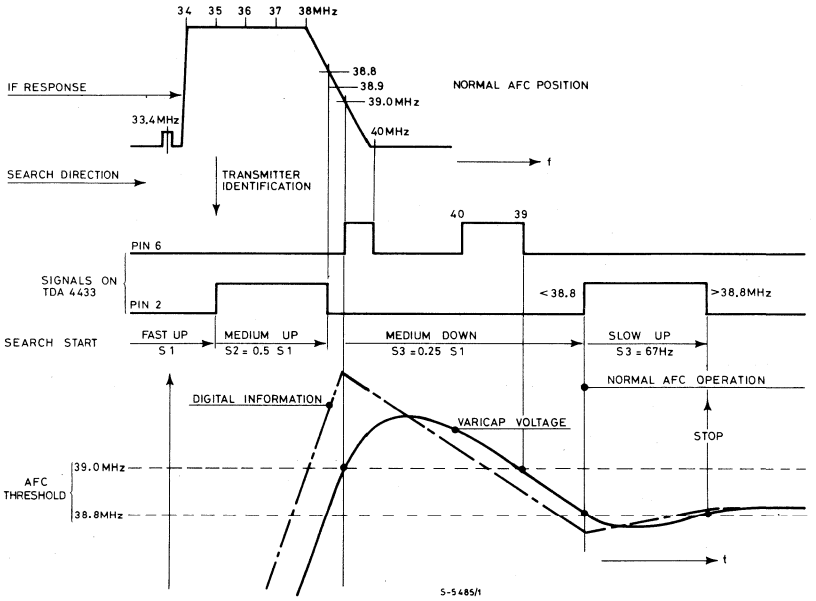
These inputs have two different functions depending on whether the system is in the search or in normal operation (AFT control).
The inputs have internal pull-up resistors of 30 KΩ typ.

A) **Search mode:** after depressing the Automatic search or preset keys, the levels of the signals coming from the TDA 4433, applied to these pins, control the search function and determine when the search must stop, i.e. a TV station has been recognized.
The circuit operates in the following sequence (see fig. 12 for reference):
1 – after pressing the search start key the search occurs in the FAST UP mode.
2 – eventual transitions available on these inputs are ignored during the first 15 search steps if the system is in the UHF or CATV bands.
If the system operates in VHF I and III the first 60 search steps are ignored. The acceptance delay of 15 (60) search steps has been introduced to prevent the system from stopping at the previous station.
After this time the FAST UP speed is automatically reduced to half during each UP signal (MEDIUM UP = FAST UP/2).
A DOWN signal preceded by at least an UP signal will set the search to MEDIUM DOWN mode (FAST UP/4).
3 – the next UP signal will switch the search to SLOW UP speed (61 Hz).
At this point the system is in normal AFT operation.

B) **Digital AFT operation:** when a station is perfectly tuned, the input signals coming from TDA 4433 are at middle condition.
If the tuning moves lower than the threshold below 38.9 MHz, the pin 12 is put H and pin 13 is put L; the 13 bit internal counter is moved with SLOW UP speed to increase the varicap voltage.
When a detuning occurs in the opposite direction the input 12 goes Low and 13 goes High and the tuning voltage is decreased with VERY SLOW DOWN speed (7.6 Hz).
The increase or decrease of the tuning voltage is stopped as soon as the input returns to middle conditions.
Therefore during normal operation pins 12 and 13 act as digital AFT control command.

C) **Recall from memory:** when the digital AFT is enabled and an information is recalled from Memory, a fixed value of 8 steps (~ 31.2 mV) is subtracted from the tuning voltage.
This corresponds to a detuning of 0.6 MHz (UHF) and of 0.3 MHz in VHF III into that part of the IF response curve which corresponds to the fully transmitted sideband.
At this point the AFT operation takes over as described in point B above and the exact tuning is achieved in about 0.2 sec.
This feature increases the AFT capture range and relaxes the stability requirements of the tuner, voltage references and the D/A converter.
If the Digital AFT is disable (pin 17 at $V_{SS}$), the memory content is read without any change.

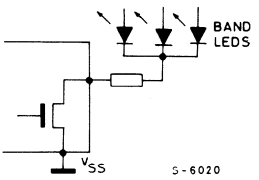
Fig. 12




## Pin 14 — Sweep search display output

This output, which is normally Low, goes High during automatic search automatic preset et intervals of 160 ms for about 40 ms to blank the LED of band display.

Fig. 13



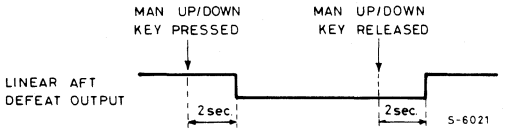

## Pin 15 — Volume D/A output

This output delivers a square wave signal of 7.8 kHz and duty cycle variable in 63 steps. In case of a continuous command for varying the volume, the duty cycle is changed at the rate of the transmitted signal (approximately every 102 ms with $f_{ref}$ = 500 kHz) or every 112 ms if issued locally.
Overflow and underflow protection are provided.
The volume output can be switched to $V_{SS}$ and reset to the previous level by means of the mute on/off command. It is also reset by the volume Up/Down and the mains on/off commands.
The volume is muted at each mains on and off command for about 1 s during the power on reset time (0.5 s) and program change.
At the first power on reset of $V_{DD1}$ the volume D/A is set at the level 21/64. The last level is preserved until $V_{DD}$ is not removed.

## Pin 16 — Linear AFT defeat output

This output is normally High and goes Low when a Man Up/Down command is issued.
The output goes Low with a 2 second delay to allow a small detuning operation. It returns High with a 2 second delay from the release of the key, in order to give the user the possibility of a tuning adjustment without the AFT intervent. It goes Low for 0.5 s during program change.

Fig. 14

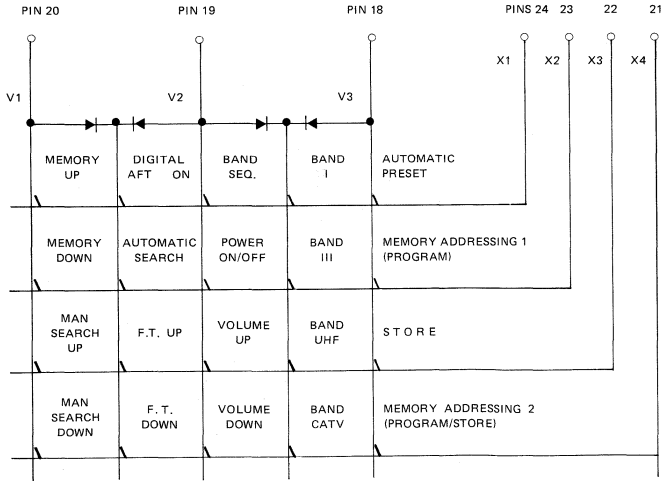



## Pin 17 — Digital AFT enable input

If this input is connected to $V_{SS}$ (GND), the digital AFT loop is always disabled. If pin 17 is left open or is connected to $V_{DD}$, the digital AFT is automatically enabled at power on. When a manual up/down search command is issued, the digital AFT loop is disabled and the digital AFT status output is switched off.
The digital AFT loop is restored by the commands: Digital AFT on/Automatic search/Automatic preset.

## Pins 18 - 19 - 20 - 21 - 22 - 23 - 24 — (keyboard matrix)

Fig. 15




A command is accepted if the corresponding contact has been closed for a minimum time of 30 ms. Local input commands and I.R. commands have the same priority.
If a complete I.R. command has been received, the local inputs are blocked until the command has been executed and the "end of transmission code" generated.
Viceversa an I.R. signal cannot be decoded until an issued local command has been executed.

## MEMORY UP/DOWN

Depressing one of these two commands, the memory position is stepped in the UP or DOWN direction. If the key is kept closed, the channels are stepped UP/DOWN every 0.5 second or every 5 commands from the transmitter.
In the M490 the locations from 11 to 16 can be skipped in groups of 2 connecting the relevant Y input to GND.
In the M491 the memory locations 9 to 16 are jumped if pin 31 is at GND.

## BAND SELECTION

The bands can be directly selected or with a step-by-step command with the following sequence:

VHF I
CATV
VHF III
UHF
VHF I and so on

Only one band change is performed at each accepted command.
Disabled bands are automatically skipped. A band can be disabled connecting the corresponding output to $V_{SS}$.

## SEARCH MODES

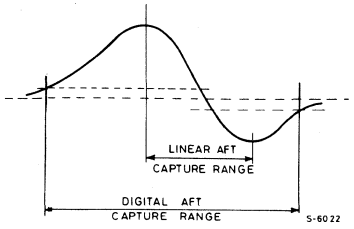
4 modes are available:

a) automatic search
b) automatic preset } (digital AFT)
c) man up/down (digital and linear AFT)
d) man up/down (linear AFT)

a) AUTOMATIC SEARCH

The search starts from the actual tuning and band position. During the search the tuning voltage is always changing from lower to higher voltage levels. When the end of the band is reached the search restarts from the beginning of the next band after a 480 ms interruption with the sequence of step by step band selection. Disable bands are automatically skipped.
The search is stopped when the first station is found or if a channel selection command is given.
Stop of the automatic search is determined by the STOP/AFT inputs controlled by the TDA 4433 which converts the AFC-S-curve into an up/down command.
At the end of the search the up/down command controls the correct tuning acting on the counter of the voltage synthesizer (Digital AFT).
It is important to call the attention to the Digital AFT capture range which is larger than the normal linear AFT as shown in fig. 16.

Fig. 16



Additionally the use of the Digital AFT allows storage of the tuning information corresponding to the zero point of the AFC-S-curve. This cannot be guaranteed using the Linear AFT method only. The latter is a cheaper system, because it does not require the use of the TDA 4433 but it cannot guarantee what described above.
As a result of the use of the Digital AFT, the requirements for stability of the tuner, of the reference voltage source and of stability of the D/A converter are less critical.
Tuning speed in automatic search, if no station is found is:

| | |
|---|---|
| VHF I | 8 second |
| VHF III | 8 second |
| UHF | 32 second |
| CATV | 32 second |

The tuning and band information can be stored using the store/memory addressing command.
The search can be stopped by a memory selection command.

b) AUTOMATIC PRESET

The search starts from the lowest memory address, tuning voltage and VHF I band as described in automatic search mode.
When an active station is encountered, the corresponding tuning and band information is automatically stored in the Non Volatile Memory.
Afterwards the system starts to search for the next station. The cycle is repeated until all bands have been swept or the tuning information have been stored into all address locations. After completing this cycle the system reads out the tuning information of the lowest address.

c) MAN UP/DOWN WITH DIGITAL AND LINEAR AFT (pin 17 at $V_{DD}$)

Holding one of these commands pressed, the tuning voltage is increased or decreased.
During this operation, the Digital AFT is automatically defeated and can only be reconnected with the "AFT on" command or by an Automatic search or preset command.
The Man up/down controls have a progressive speed variable with the time as follows:

| Search Speed (normalized) | Time |
|---|---|
| : 8 | Command accepted |
| : 4 | After 1 second |
| : 2 | After 2 seconds |
| : 1 | After 3 seconds (fast speed) |

Sweep time for each band (fast speed) is:

| | |
|---|---|
| VHF I | 16 second |
| VHF III | 16 second |
| UHF | 64 second |
| CATV | 64 second |

In case of command received from remote control, the counter is increased/decreased every two received commands.
No band switching is provided at the upper or lower tuning position.
The volume is automatically muted 3 second after the key pressure and is immediately restored at the release of the key.

d) MANUAL UP/DOWN WITH LINEAR AFT (pin 17 at $V_{SS}$)

When this control is used the Digital AFT is disabled.
The Linear AFT output goes low 2 second after an up or down command is pressed.
The output remains low 2 second after the release of the key.
The volume is automatically muted 3 second after the key pressure and is immediately restored at the release of the key.
Tuning speeds are as described at point 3 above.
This is the cheapest search mode.

**FINE TUNING UP/DOWN**
See description of pin 4.

**DIGITAL AFT ON**
See description of pin 17.

**VOLUME UP/DOWN**
See description of pin 15.

**MAINS ON/OFF**
See description of pins 25 and 26.

**STORE COMMANDS**
3 modes of operations are available:

a) store
b) memory addressing 1 (memory)
c) memory addressing 2 (memory/store)

In order to protect the memory, the store function is internally disabled after one store cycle.
It is enabled after a program change or a tuning operation (it is not disabled by the Digital AFT control).

a) STORE

The tuning information (Tuning D/A, Fine tuning D/A and band) is stored in a previously selected memory address when this command is issued.

b) MEMORY ADDRESSING 1 (MEMORY)

The tuning information can also be stored with this command followed by the memory position selection.
When this command is accepted all the memory LEDs are blanked.
Selection of the memory position initiates the store operations and restores the display.

c) MEMORY ADDRESSING 2 (MEMORY/STORE)

The sequence for storage operation is:

- Memory Addressing 2 command. The previously selected memory position is flashing.
- The memory position can be changed with direct or up/down memory commands. The display is still flashing.
- The display is stable and the tuning information is stored by the "store" command.

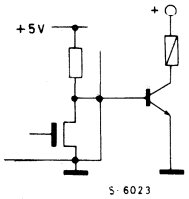
## Pin 25 – Mains on option input

If connected to $V_{SS}$ (GND) the Mains output is automatically switched on when $V_{DD}$ is applied and memory 1 is read.
If it is connected to $V_{DD}$ the circuit goes in stand by condition.

## Pin 26 – Mains on/off output

Switch on of the set is controlled by the Mains on command issued for more than 0.3 s. The output transistor if set in the off condition to drive through an integrated pull-up resistor an external NPN transistor.

Fig. 17



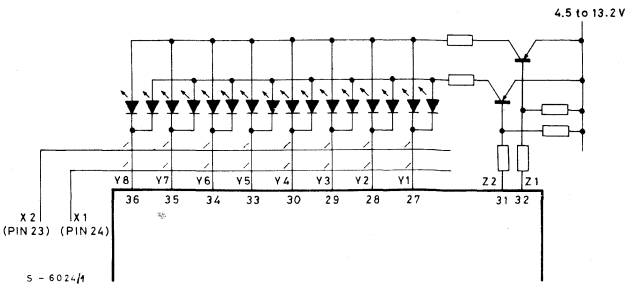

At each Mains on command a memory read out occurs. As $V_{PP}$ (+25V) is required for this operation, a 1 second delay starts when the mains output is switched off. For a correct reading of the memory the $V_{PP}$ supply voltage must reach the value of 25V within 1 second after a Mains on command.
In case of automatic switch on at power on caused by pin 25 at GND, the total delay is of 1.5 second (0.55 s for $V_{DD}$ power on reset plus 1 second for mains on).
The Mains on/off command, if repeated, will switch the output on (set off).
The last address information is preserved until $V_{DD}$ is present.
Next Mains on command will switch the set at the previously selected memory address and a read operation will be performed.

## Pins 27 - 28 - 29 - 30 - 33 - 24 - 35 - 36 – Memory Address Input/Output

### M490

Up to 16 Memory locations can be selected.
When $V_{DD}$ is applied to the circuit the address is automatically preset to the first memory location. Selection of a memory location is provided connecting one address input line with an X scanning line for more than 30 ms; this condition is internally latched and the corresponding output buffer is switched on to drive the LED.
Max drive capacity is of 20 mA with $V_{OL}$= 1.5V.
8 output are provided and 16 channel display is achieved multiplexing the LEDs with the control outputs "Z".
If pins 34, 35, 36 are connected to $V_{SS}$, the corresponding memory locations are skipped in case of up/down memory commands.

Fig. 18



**M491**

These pins operate as output only for display of the selected memory location. Max drive capability is of 15 mA/1.2V with the exception of pin 36 that is of 30 mA/1.5V.
Direct memory selection is only possible by remote control. A local memory up/down command is available in case of emergency.
Pin 32 must be grounded.
If pin 31 is grounded, the memory position 9 to 16 are skipped in case of memory up/down commands.
For normal operation pin 31 can be left open or, better, connected to $V_{DD}$.

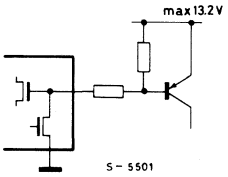
## Pins 31-32

See description of pins 27 to 30 and 33 to 36.

## Pins 37 - 38 - 39 - 40 — Band Input/output

These outputs are provided to select up to 4 bands via external PNPs.
If one or more bands have to be skipped, the corresponding outputs have to be short-circuited to $V_{SS}$.

Fig. 19

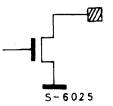



The relation between pins and bands are as follows:

pin 37 = UHF
pin 38 = CATV
pin 39 = VHF III
pin 40 = VHF I

**INPUT/OUTPUT CONFIGURATION**

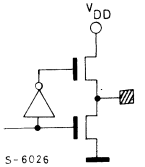
Outputs open drain




Pins 3, 4, 5, 6, 14, 15, 16, 31, 32 (M490).

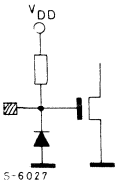
Pins 3, 4, 5, 6, 14, 15, 16, 27, 28, 29, 30, 33, 34, 35, 36 (M491).

Output push-pull



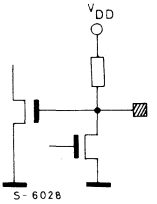

Pin 26.

Inputs with pull-up load



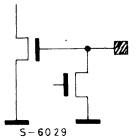

Pins 12, 13, 17, 18, 19, 20, 25 (M490 and M491)
Pin 31 (M491 only).

Inputs/Outputs with pull-up resistor (M490 only)



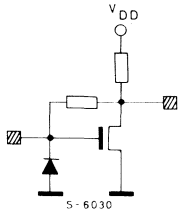

Pins 27, 28, 29, 30, 33, 34, 35, 36.

Inputs/Outputs (std)



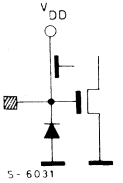

Pins 37, 38, 39, 40, 21, 22, 23, 24 (21, 22, 23, 24 are used only for testing purposes).

Oscillator




Pin 8

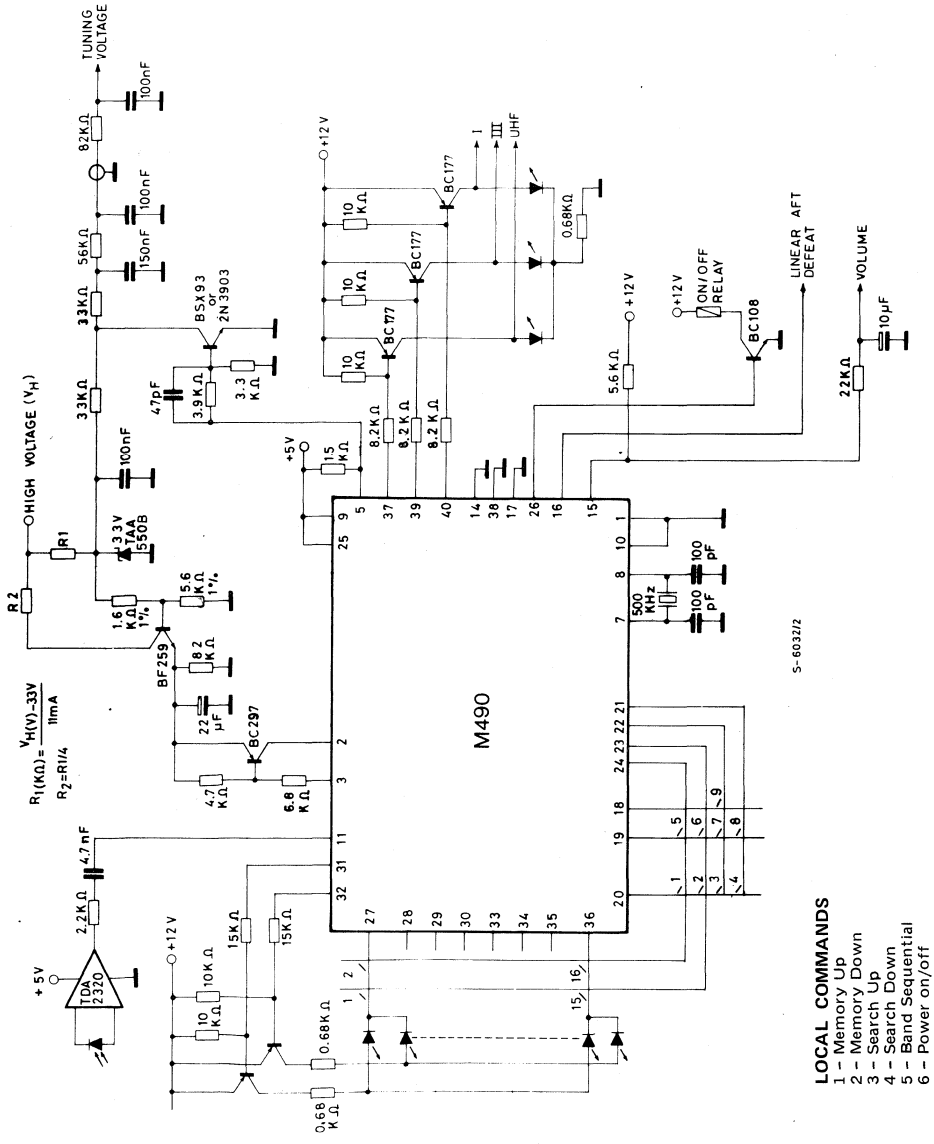
IR input




Pin 11.

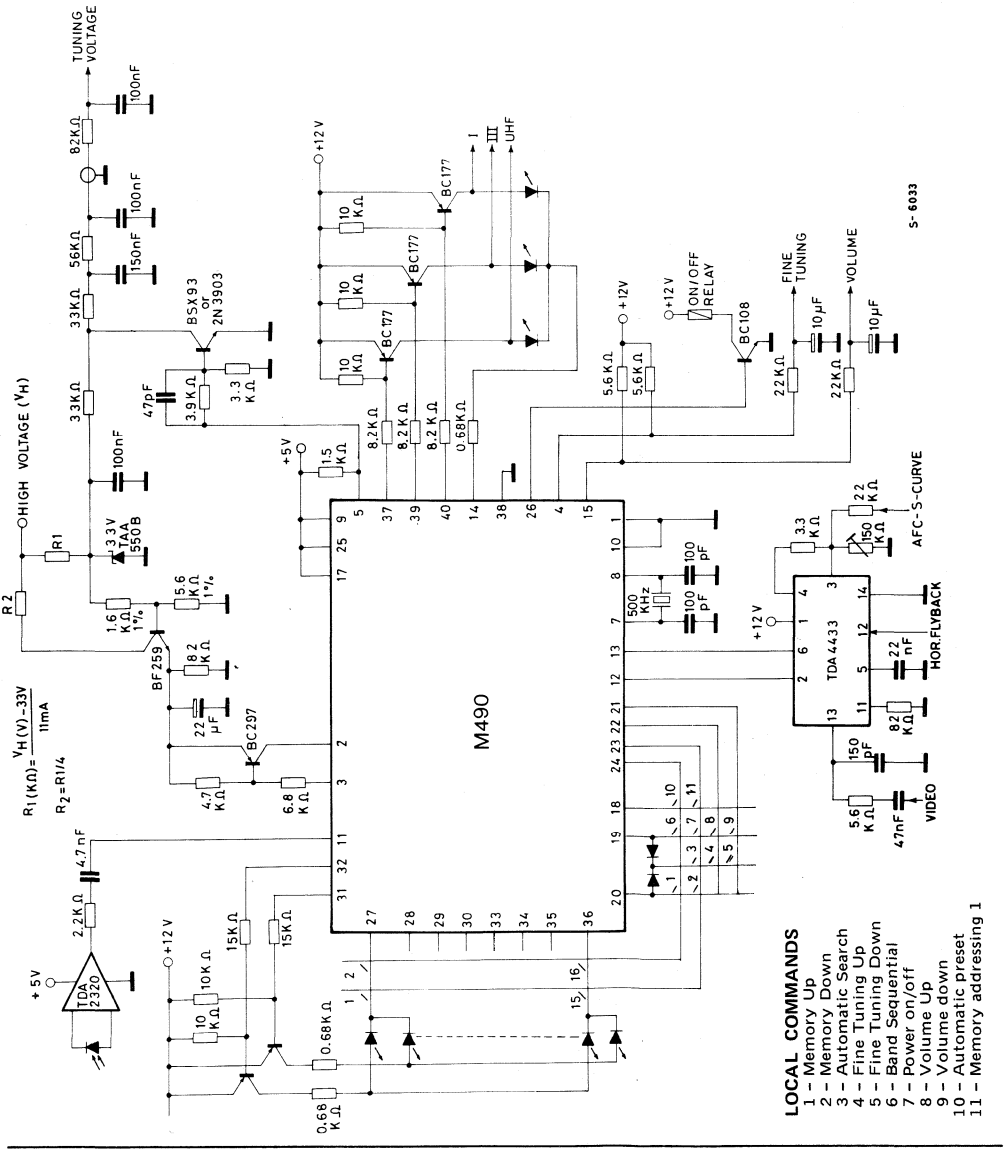
## TYPICAL APPLICATIONS

Manual search with linear AFT



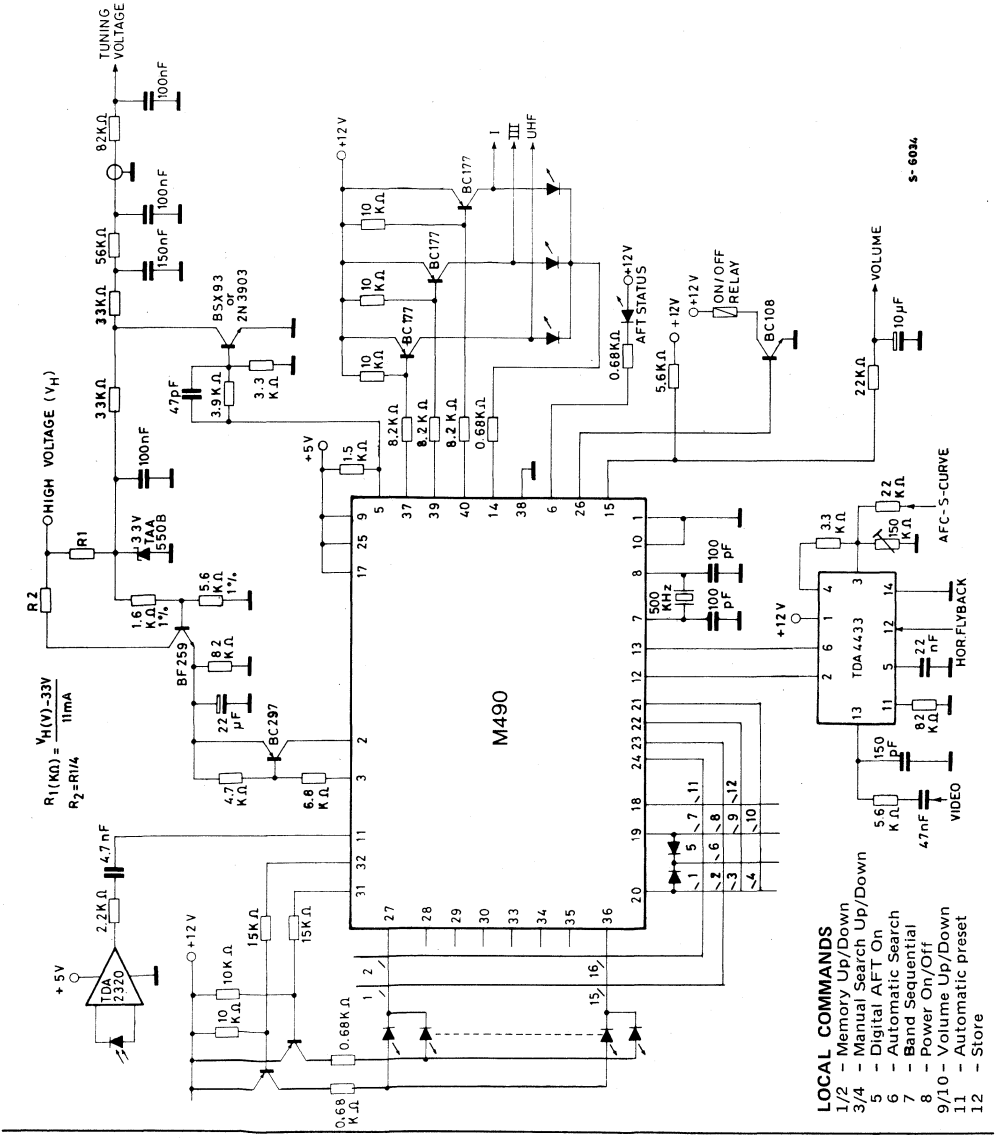
## TYPICAL APPLICATIONS (continued)

Automatic search
Automatic preset
Fine tuning with D/A } Digital AFT



## TYPICAL APPLICATIONS (continued)

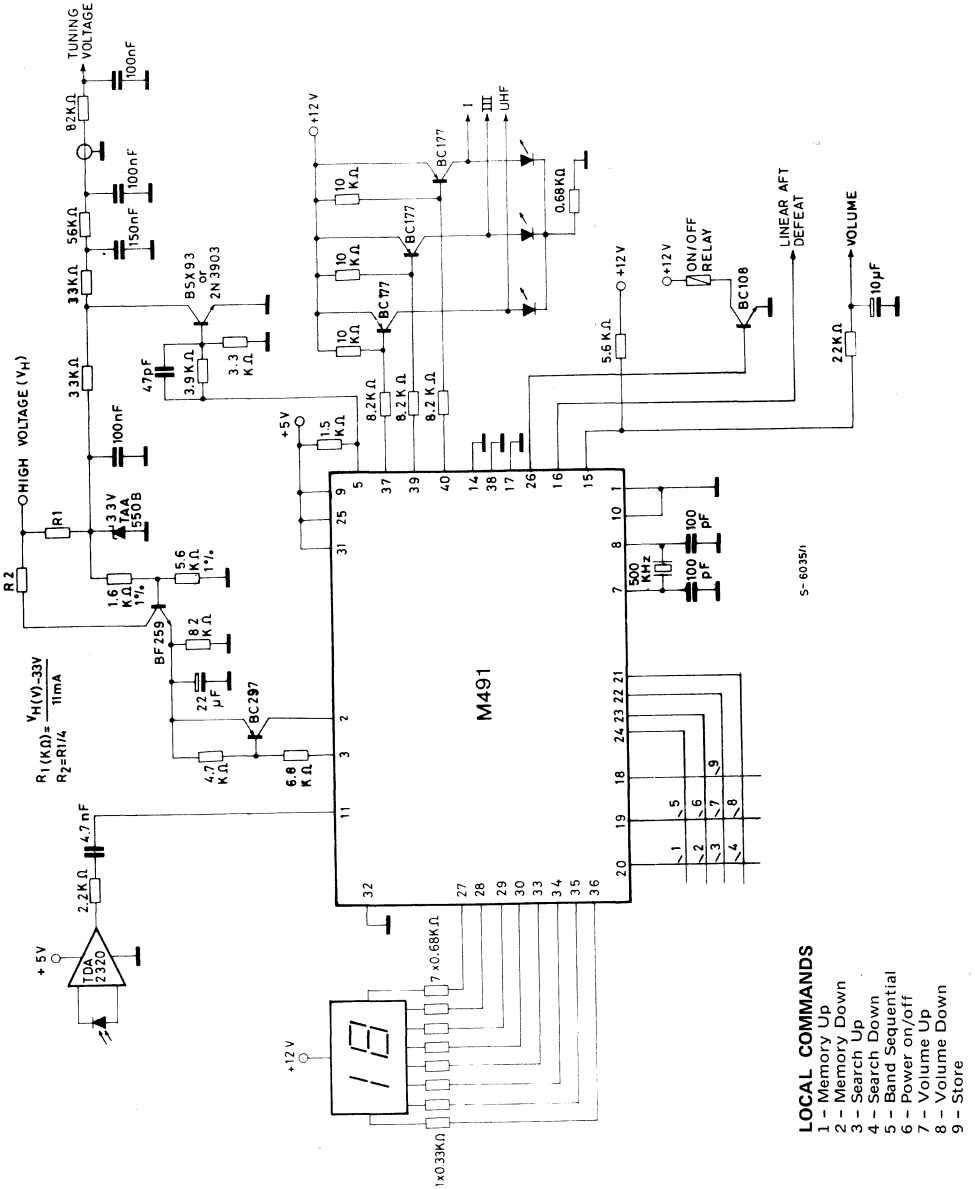
Automatic search
Automatic preset
Manual Up/Down
} Digital AFT




**LOCAL COMMANDS**
1/2 - Memory Up/Down
3/4 - Manual Search Up/Down
5 - Digital AFT On
6 - Automatic Search
7 - Band Sequential
8 - Power On/Off
9/10 - Volume Up/Down
11 - Automatic preset
12 - Store

## TYPICAL APPLICATIONS (continued)

M491 - Manual search with Linear AFT (16 memory Option)



## 15/16 DIVIDER FOR TV PLL FREQUENCY SYNTHESIZER

- HIGH INPUT SENSITIVITY (MIN. 500 $mV_{PP}$)
- LOW POWER DISSIPATION DUE TO CMOS TECHNOLOGY
- TTL COMPATIBLE 15/16 DIVIDER CONTROL INPUT
- TTL OUTPUT LEVEL

The M705 is a 15/16 divider to be used in TV PLL frequency synthesiser systems, in conjunction with a prescaler by 64 and the M206 PLL TV microprocessor interface.
It is produced with a CMOS Silicon Gate technology and is assembled in an 8-pin plastic package.

## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$* | Supply voltage | -0.3 to 7 | V |
| $V_I$ | Input voltage | -0.3 to $V_{DD}$ + 0.3 | V |
| $I_o$ | Output current | 5 | mA |
| $V_{O(off)}$ | Off state output voltage | 6 | V |
| $T_{op}$ | Operating temperature range | 0 to 70 | °C |
| $T_{stg}$ | Storage temperature range | -65 to 150 | °C |

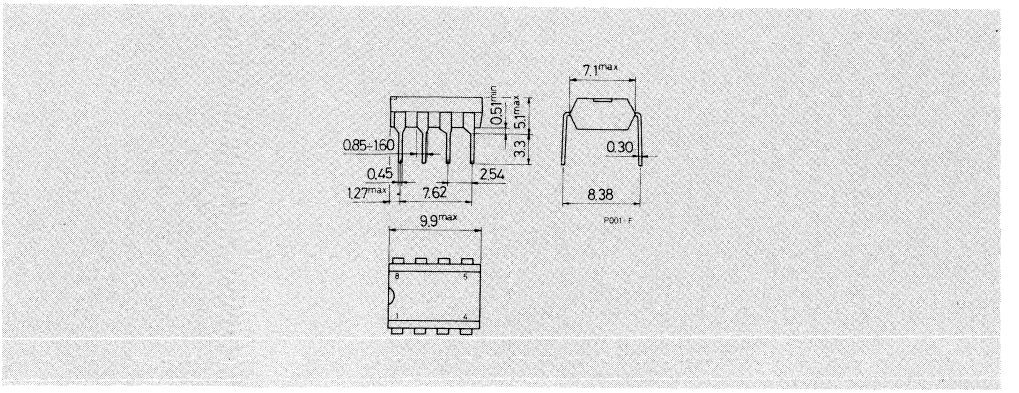
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* All voltages are with respect to $V_{SS}$ (GND).

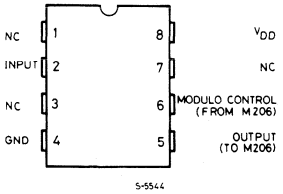
**ORDERING NUMBER:** M705 B1

## MECHANICAL DATA

Dimension in mm



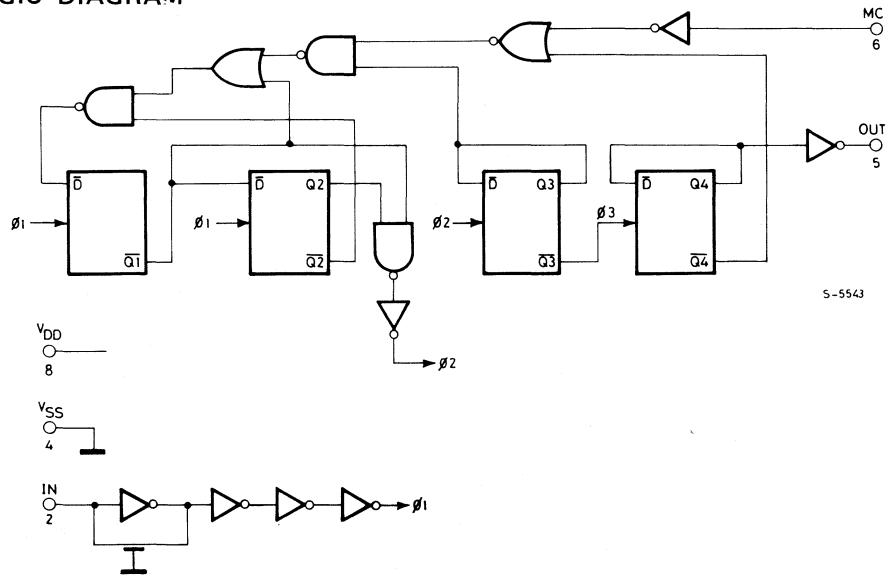
## PIN CONNECTIONS




## TRUTH TABLE

| |
|---|
| MC = 1 → IN : 15 |
| MC = 0 → IN : 16 |

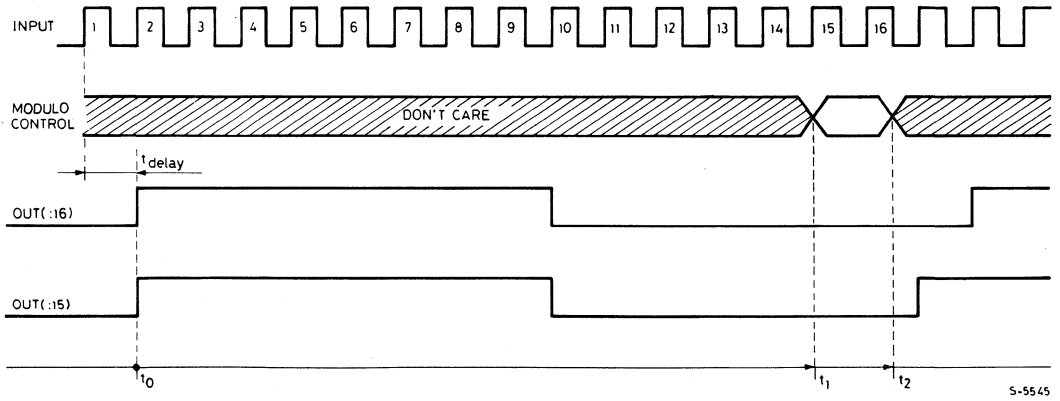
## LOGIC DIAGRAM



## ELECTRICAL CHARACTERISTICS ($T_{amb}$= 0 to 70°C, Typ values are given at $V_{DD}$= 5V)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 4.5 | 5 | 5.5 | V |
| $I_{DD}$ | Supply Current | $V_{DD}$= 5.5V f = 16 MHz | | 1 | 3 | mA |
| $f_i$ | Frequency Range (pin 2) | $C_{out}$= 15 pF | 0.1 | | 16 | MHz |
| $V_i$ | Input Sensitivity (pin 2) | See typical application | 0.5 | | | $V_{PP}$ |
| MC | MC Input Levels $V_{IH}$ | | 2.8 | | | V |
| | $V_{IL}$ | | | | 0.8 | |
| $V_{OL}$ | Low Level Output Voltage | $I_{OL}$= 1.6 mA | | | 0.4 | V |
| $V_{OH}$ | High Level Output Voltage | $I_{OH}$= -1.6 mA | 2.4 | | | V |
| $V_I$ | Input Voltage Range | | 0 | | $V_{DD}$ | V |

## TIMING DIAGRAM




NOTE: The counter is triggered by the positive edge of the input signal.
The Modulo control signal must be stable during the Low level time of the 15th pulse. Including a security reserve time, we can define the maximum set up time $t_1$ with respect to $t_0$ :

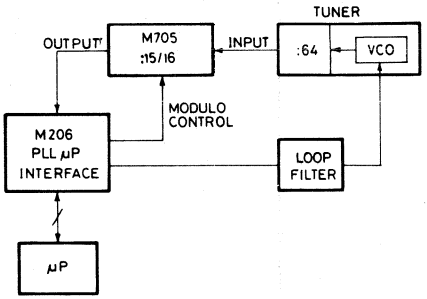
$$t_1 = 15 \cdot \frac{64}{f_{VCO}} - 140 \text{ ns}$$

The 140 ns time includes the propagation delay time of the Modulo control signal and of all the count chain.
At $f_{VCO}$ = 1024 MHz,

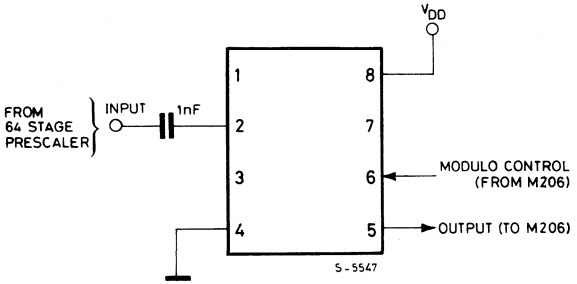
$$t_{1\,max} = 15 \cdot \frac{64}{1024 \cdot 10^6} - 140 \text{ ns} = 800 \text{ ns.}$$

The minimum hold time $t_2$ is $t_1$ plus a security time of 100 ns. Therefore $t_{2\,min}$ = 900 ns.

## SYSTEM CONFIGURATION




## TYPICAL APPLICATION




Note: Pins 1 – 3 must be left open.

# M708
# M708A

**CMOS INTEGRATED CIRCUITS**

**PRELIMINARY DATA**

## PCM REMOTE CONTROL TRANSMITTER

- 30 CHANNELS/4 ADDRESSES
- SELECTABLE FLASH/CARRIER TRANSMISSION MODE
- END OF TRANSMISSION CODE
- VERY LOW POWER DISSIPATION DURING TRANSMISSION: DUTY CYCLE 0.15% (FLASH MODE), 0.7% (CARRIER MODE)
- SINGLE CONTACT MATRIX KEYBOARD
- INTEGRATED ANTIBOUNCE AND INTERLOCK
- WIDE SUPPLY RANGE (M708 4.5 to 10.5V)/(M708A 3 to 10.5V).
- WIDE REFERENCE FREQUENCY RANGE (445 TO 510 kHz CERAMIC RESONATOR)
- 20 PIN PLASTIC PACKAGE
- TO BE USED IN CONJUNCTION WITH M490/M491 SINGLE CHIP STATION MEMORY AND R.C. RECEIVER (FLASH MODE) OR WITH MICROPROCESSOR CONTROLLED SYSTEM (CARRIER MODE)

This IC has been developed for remote control in consumer applications. It uses a highly reliable transmission code which has the capacity of 1024 channels. Each transmitted word is structured into 4 bits which constitute the address and 6 bits which constitute the command. However only 2 addresses and 30 commands are available in this IC. An additional command (000000) is used to transmit the "end of transmission code" when the key is released.

Additional bits are transmitted for synchronization of transmitter and receiver clocks and for security checks. The address organization provides simultaneous applications without interference among each system.

The receiver accepts the decoded command only if the transmitted address matches the address selected at the receiver. Four addresses are available for this purpose. The reference oscillator is controlled by a cheap ceramic resonator.

When the M708 works in conjunction with M490/M491 single chip Station Memory and R.C. receiver the oscillator frequency can be in the range 445 to 510 kHz and no synchronization is required with the receiver clock.

The M708 is produced with CMOS Si-gate technology and is available in a 20 pin dual in-line plastic package.

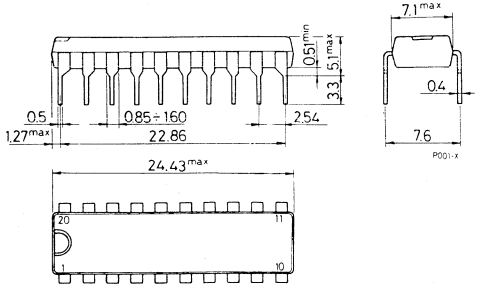
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 12 | V |
| $V_I$ | Input voltage | -0.3 to $V_{DD}$ +0.3 | V |
| $\|I_O\|$ | IR output current ($t < 50\ \mu s$) | 10 | mA |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |
| $P_{tot}$ | Total package power dissipation | 200 | mW |
| $T_{stg}$ | Storage temperature | -55 to 125 | °C |

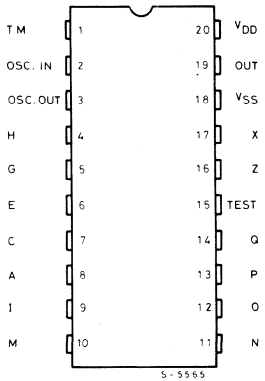
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

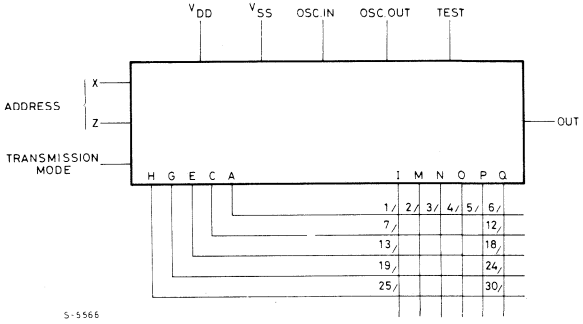
**ORDERING NUMBER:** M708 B1
M708A B1

## MECHANICAL DATA (Dimensions mm.)



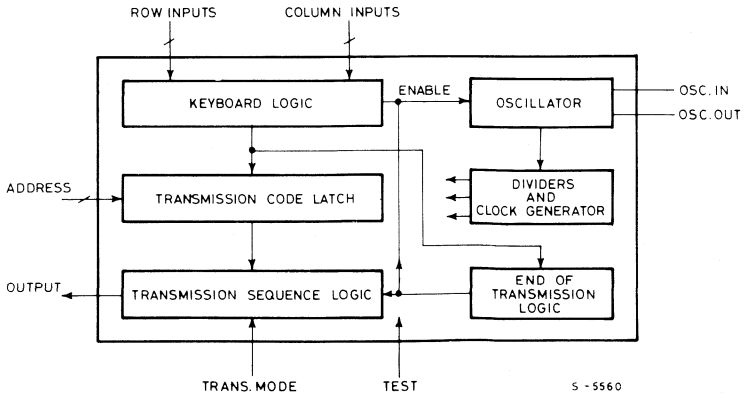

## PIN CONFIGURATION




Note: The test pin must be connected to $V_{SS}$.

## BLOCK DIAGRAM



## RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage: M708 | 4.5 to 10.5 | V |
| | M708A | 3 to 10.5 | V |
| $V_I$ | Input voltage | 0 to $V_{DD}$ | |
| $\|I_O\|$ | IR output current ($t < 50\ \mu s$) | max 2.5 | mA |
| $f_{ref}$ | Reference frequency | 445 to 510 | kHz |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |
| $r_s$ | Serial resistance of a closed key contact | max 2.5 | KΩ |
| $r_p$ | Parallel resistance of open key contact | min. 2.2 | MΩ |
| $R_s$ | Serial resistance of the ceramic resonator | max 20 | Ω |

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at 9V and $T_{amb}$= 25°C

| Parameter | | Pins | Test conditions | | Values Min. | Values Typ. | Values Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply Voltage | | $V_{DD}$= 9V IR output open | Stand-by | | 5 | 15 | μA |
| | | | | Operating (one key closed) | | 4 | 7 | mA |
| $I_{OH}$ | H State IR Output Current | | $V_{DD}$= 9V | $V_{OH}$= 8V | -1.5 | -2.5 | | mA |
| | | | $V_{DD}$= 4.5V | $V_{OH}$= 3.5V | -0.3 | -0.5 | | |
| $I_{OL}$ | L State IR Output Current | | $V_{DD}$= 9V | $V_{OL}$= 1V | 1.5 | -2.5 | | mA |
| | | | $V_{DD}$= 4.5V | $V_{OL}$= 1V | 0.3 | 0.5 | | |
| $V_{TH}$ | Input Threshold High | Selection inputs A to H | $V_{DD}$= 9V | | | | 6 | V |
| | | | $V_{DD}$= 4.5V | | | | 3 | |
| $V_{TL}$ | Input Threshold Low | Selection inputs K to Q | $V_{DD}$= 9V | | 3 | | | V |
| | | | $V_{DD}$= 4.5V | | 1.5 | | | |
| $I_{IL}$ | Input Low Current | Pull-up inputs A to H | $V_{DD}$= 9V $V_{IL}$= 4.5V | | -60 | | -300 | μA |
| $I_{IH}$ | Input High Current | Pull-down inputs K to Q | $V_{DD}$= 9V $V_{IH}$= 4.5V | | 60 | | 300 | μA |
| $I_{IH}$ | Input High Current | Address selection inputs | $V_{DD}$= 9V $V_{IL}$= 8.25V (oscillator running) | | | | 150 | μA |
| $I_L$ | Input Leakage Current | Trans. mode Test pin | $V_{DD}$= 9V $V_{IN}$= 0 to 9V | | | | 1 | μA |
| $I_{OS}$ | Output Current | Osc. out. | $V_{DD}$= 9V Osc. in. = $V_{SS}$ | | -2 | | -8 | μA |

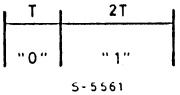
## TRUTH TABLE

| Command No. | Input code | | | | | | | | | | | Command bits | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | C | E | G | H | I | M | N | O | P | Q | C1 | C2 | C3 | C4 | C5 | C6 |
| 0 | END OF TRANSMISSION | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | X | | | | | X | | | | | | 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | X | | | | | | X | | | | | 1 | 1 | 0 | 0 | 0 | 0 |
| 3 | X | | | | | | | X | | | | 0 | 0 | 1 | 0 | 0 | 0 |
| 4 | X | | | | | | | | X | | | 1 | 0 | 1 | 0 | 0 | 0 |
| 5 | X | | | | | | | | | X | | 0 | 1 | 1 | 0 | 0 | 0 |
| 6 | X | | | | | | | | | | X | 1 | 1 | 1 | 0 | 0 | 0 |
| 7 | | X | | | | X | | | | | | 1 | 0 | 0 | 0 | 1 | 0 |
| 8 | | X | | | | | X | | | | | 1 | 1 | 0 | 0 | 1 | 0 |
| 9 | | X | | | | | | X | | | | 0 | 0 | 1 | 0 | 1 | 0 |
| 10 | | X | | | | | | | X | | | 1 | 0 | 1 | 0 | 1 | 0 |
| 11 | | X | | | | | | | | X | | 0 | 1 | 1 | 0 | 1 | 0 |
| 12 | | X | | | | | | | | | X | 1 | 1 | 1 | 0 | 1 | 0 |
| 13 | | | X | | | X | | | | | | 1 | 0 | 0 | 0 | 0 | 1 |
| 14 | | | X | | | | X | | | | | 1 | 1 | 0 | 0 | 0 | 1 |
| 15 | | | X | | | | | X | | | | 0 | 0 | 1 | 0 | 0 | 1 |
| 16 | | | X | | | | | | X | | | 1 | 0 | 1 | 0 | 0 | 1 |
| 17 | | | X | | | | | | | X | | 0 | 1 | 1 | 0 | 0 | 1 |
| 18 | | | X | | | | | | | | X | 1 | 1 | 1 | 0 | 0 | 1 |
| 19 | | | | X | | X | | | | | | 1 | 0 | 0 | 0 | 1 | 1 |
| 20 | | | | X | | | X | | | | | 1 | 1 | 0 | 0 | 1 | 1 |
| 21 | | | | X | | | | X | | | | 0 | 0 | 1 | 0 | 1 | 1 |
| 22 | | | | X | | | | | X | | | 1 | 0 | 1 | 0 | 1 | 1 |
| 23 | | | | X | | | | | | X | | 0 | 1 | 1 | 0 | 1 | 1 |
| 24 | | | | X | | | | | | | X | 1 | 1 | 1 | 0 | 1 | 1 |
| 25 | | | | | X | X | | | | | | 1 | 0 | 0 | 1 | 1 | 1 |
| 26 | | | | | X | | X | | | | | 1 | 1 | 0 | 1 | 1 | 1 |
| 27 | | | | | X | | | X | | | | 0 | 0 | 1 | 1 | 1 | 1 |
| 28 | | | | | X | | | | X | | | 1 | 0 | 1 | 1 | 1 | 1 |
| 29 | | | | | X | | | | | X | | 0 | 1 | 1 | 1 | 1 | 1 |
| 30 | | | | | X | | | | | | X | 1 | 1 | 1 | 1 | 1 | 1 |

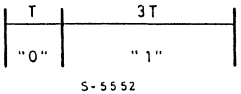
## DESCRIPTION

The signals are transmitted with infrared light using a Pulse Code Modulation. Each word consists of 12 bits. The binary information of a bit is determined by the time interval between two pulses. If "T" is the time base, the bits are coded as follows:

Odd bits (1, 3, etc.)
0 = T
1 = 2T

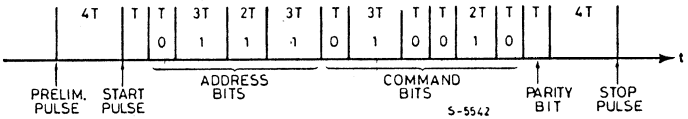



Even bits (2, 4, etc.)
0 = T
1 = 3T




The different code introduced for the even and odd "1s" improves the capability to recognize false codes at the receiver end. For example the double error which can cause the exchange "10" with "01" is easily detected. A Parity bit is also added in order to further increase the reliability of the transmission. This bit is "1" if the number of transmitted "1" is even while it is "0" if the number of transmitted "1" is odd. In addition, every word contains a preliminary pulse, a start pulse and a stop pulse. The spacing between the preliminary and the start pulse is 4T. This is followed after 1T by 11 data pulses (one parity bit), and terminated after a 4T interval by a stop pulse. Consequently, a word in which the binary digit 0 occurs ten times has a total duration of 21T. A word containing ten "1s" has a duration of 36T.

Example:

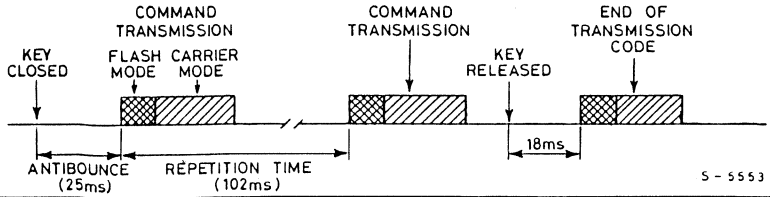



### Synchronization between transmitter and receiver

The transmitter and the receiver can operate with different reference frequencies. Typical values suitable for correct operation of the system should be comprised between 445 and 510 kHz, using a cheap ceramic resonator.
Synchronization between the transmitter and the receiver, necessary to obtain the above described wide range of frequency tolerance is achieved by measuring in the receiver the interval between the start pulse and the first data pulse, storing this value and using it as time base T.

### Keyboard/Code repetition

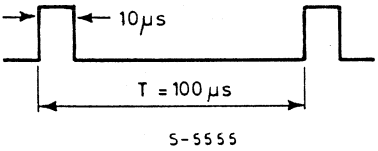
One column input (pins IMNOPQ) has to be connected to one row (pins ACEGH) input to activate the transmitter. The contact must be continuously closed for a minimum of 25 ms.
Double and multiple contact operations are not accepted. The command information is repeatedly transmitted at intervals of 102 ms ($f_{ref}$= 500 kHz) as long as the push button remains operated. When the contact is interrupted the circuit transmits, after a pause of 18 ms, the "end of transmission code" and returns to stand-by mode. If the contact is interrupted while a command is being transmitted the circuit carries on with the transmission to the end. After a pause of about 18 ms it transmits the end of trans mission code.
No command is accepted until the "end of transmission code" is over.



## Transmission mode (pin T)

The M708 can operate in Flash (pin T = $V_{DD}$) or Carrier (pin T = $V_{SS}$) transmission modes. Using a reference frequency of 500 kHz the output signal has these formats respectively:

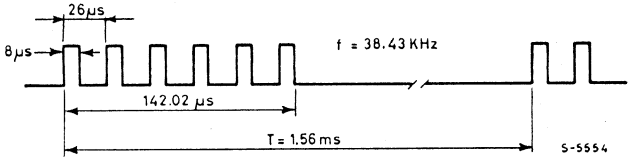
Flash mode




**Transmission time**

min. = 2.1 ms
max. = 3.6 ms
duty cycle = 0.15%

Carrier mode

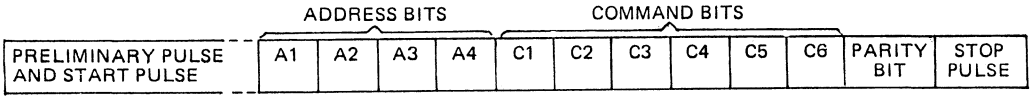


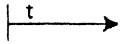

**Transmission time**

min. = 32.76 ms
max. = 56.16 ms
duty cycle = 0.7%

## Address (pins X, Z)

The address information is coded and transmitted as follows:

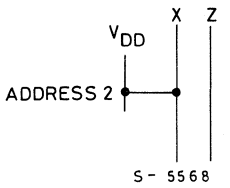


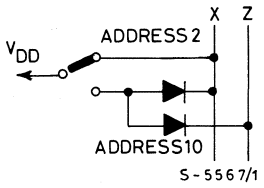

| Address number | Transmitted code A1 | A2 | A3 | A4 | Address Input code X | Z |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | L | L |
| 2 | 1 | 0 | 0 | 0 | H | L |
| 9 | 0 | 0 | 0 | 1 | L | H |
| 10 | 1 | 0 | 0 | 1 | H | H |

The Address inputs have internal pull-downs which are disabled during stand-by.

Single address selection



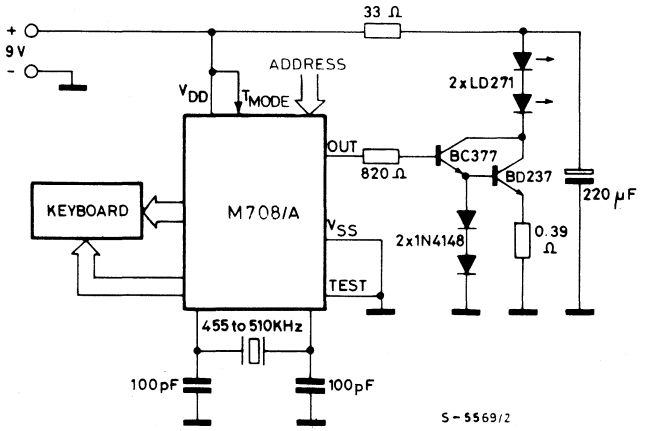

Multiple address selection




Note: Unused inputs can be left open or connected to $V_{SS}$.

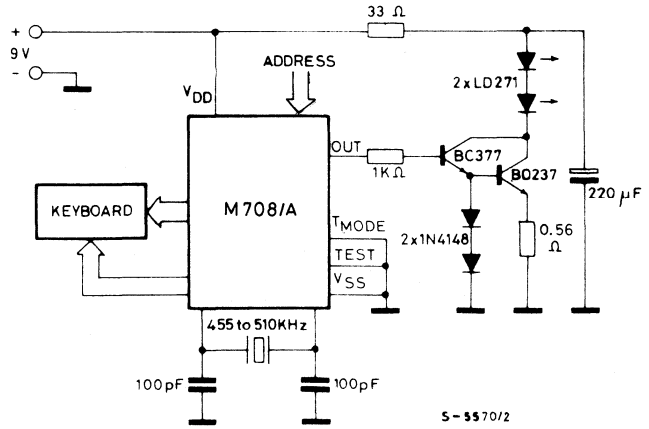
## TYPICAL APPLICATIONS

Flash Mode




INFRARED DIODE PEAK CURRENT = 1.8A
TOTAL AVERAGE CONSUMPTION = 6.5mA

Carrier Mode




INFRARED DIODE PEAK CURRENT = 1.25A
TOTAL AVERAGE CONSUMPTION = 13mA

# CMOS INTEGRATED CIRCUITS

**M709/A**
**M710/A**

**PRELIMINARY DATA**

## PCM REMOTE CONTROL TRANSMITTERS

- M 709 : 40 COMMANDS x 16 ADDRESSES
- M 710 : 64 COMMANDS x 16 ADDRESSES
- ADDRESS ORGANIZATION PROVIDES WIDE RANGE OF SIMULTANEOUS APPLICATIONS WITHOUT INTERFERENCE BETWEEN SYSTEMS
- IMPROVED PCM TRANSMISSION CODE PROVIDES EASY RECOGNITION OF FALSE SIGNALS
- "FLASH" OR "CARRIER" PIN SELECTABLE TRANSMISSION MODES
- END OF TRANSMISSION CODE
- SINGLE CONTACT MATRIX KEYBOARD
- INTEGRATED ANTIBOUNCE AND INTERLOCK
- WIDE SUPPLY RANGE (M709/M710 4.5 to 10.5V)/(M709A/M710A 3 to 10.5V)
- WIDE REFERENCE FREQUENCY RANGE (445 TO 510 kHz CERAMIC RESONATOR)
- VERY LOW POWER CONSUMPTION DURING TRANSMISSION. OUTPUT DUTY CYCLE 0.15% (FLASH MODE), 0.7% (CARRIER MODE)
- TO BE USED IN CONJUCTION WITH M104 OR M105 R.C. RECEIVERS (FLASH MODE). THE CARRIER MODE IS FOR $\mu$P DECODING (e.g. PLL FREQUENCY SYNTHESIZER WITH M3870/M3872 AND M206)

These ICs have been developed for remote control in consumer applications (TV, radio, videorecorders) or in the industrial field and use a highly reliable transmission code which has a capacity of 1024 channels. Each transmitted word is structed into 4 bits which constitute the address and 6 bits which constitute the command (64 commands available). One command (1st = 000000) is used to transmit the "end of transmission code" when the key is released. Additional bits are transmitted for synchronization of transmitter and receiver clocks and for security checks. The address organization provides a wide range of simultaneous applications without interference between systems. The receiver accepts the decoded command only if the transmitted address matches the address selected at the receiver. 16 addresses are available for this purpose.

The reference oscillator is controlled by a cheap ceramic or LC resonator and when the M709/M710 work in conjunction with the M104 or M105 R.C. receives the oscillator frequency can be in the range 445 to 510 kHz and no synchronization is required with the receiver clock. Two types of transmission mode are available: "Flash" or "Carrier" mode.
The M709 is a simplified version of the M710 which can only transmit 40 commands with 16 possible addresses. The M710 on the other hand has the full system capacity: it can transmit 64 commands with 16 addresses.

The M709 and M710 are produced with CMOS Si-gate technology and are available in 24 and 28-pin dual in-line plastic packages respectively.

**ORDERING NUMBERS:** M709 B1
M710 B1
M709A B1
M710A B1

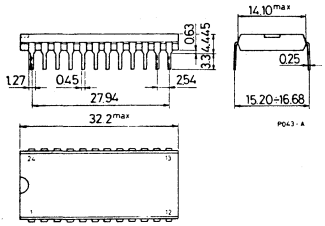
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 12 | V |
| $V_I$ | Input voltage | -0.3 to $V_{DD}$ + 0.3 | V |
| $\|I_O\|$ | IR output current ($t < 50\ \mu s$) | 10 | mA |
| $P_{tot}$ | Total package power dissipation | 200 | mW |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |
| $T_{stg}$ | Storage temperature | -55 to 125 | °C |

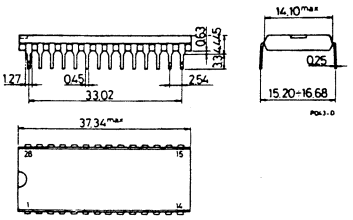
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## MECHANICAL DATA (dimensions in mm)

Dual in-line plastic package (M 709-M 709A)



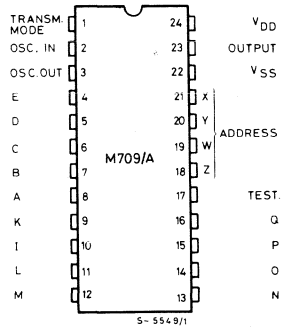

Dual in-line plastic package (M 710-M 710A)

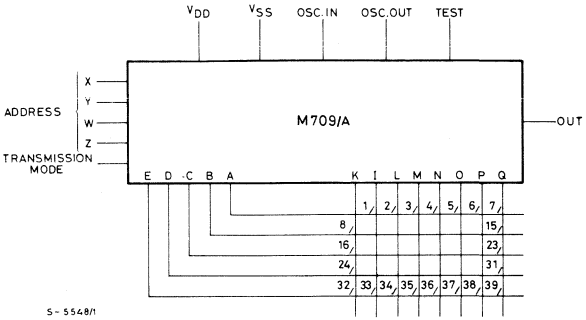


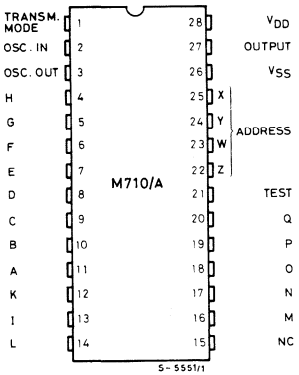

## RECOMMENDED OPERATING CONDITIONS

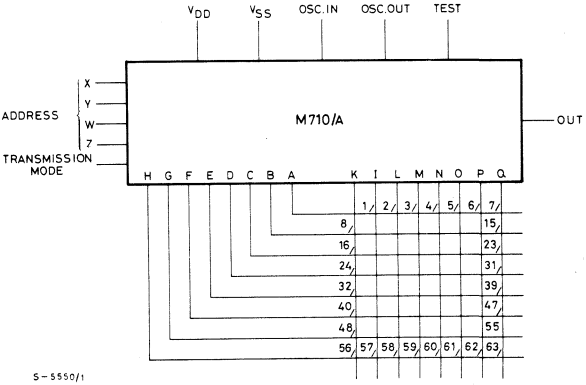
| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage: M709/M710 | 4.5 to 10.5 | V |
| | M709A/M710A | 3. to 10.5 | V |
| $V_I$ | Input voltage | 0 to $V_{DD}$ | |
| $\|I_O\|$ | IR output current ($t < 50\ \mu s$) | max. 2.5 | mA |
| $f_{ref}$ | Reference frequency | 445 to 510 | kHz |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |
| $r_s$ | Serial resistance of a closed key contact | max. 2.5 | KΩ |
| $r_p$ | Parallel resistance of open key contact | min. 2.2 | MΩ |
| $R_s$ | Serial resistance of the ceramic resonator | max. 20 | Ω |

## PIN CONNECTIONS



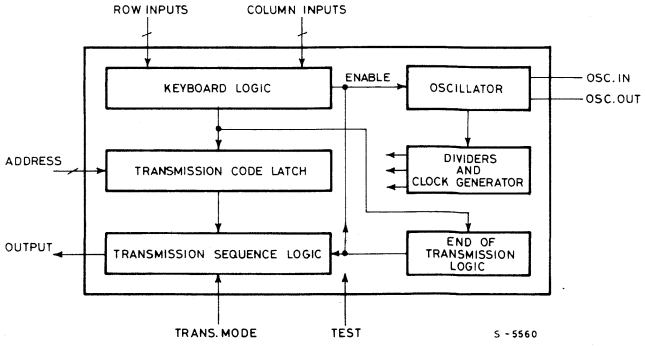




Note: The test pin must be connected to $V_{SS}$

## BLOCK DIAGRAM



## TRUTH TABLE

| Command No. | Input code | | | | | | | | | | | | | | | | Command bits | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | B | C | D | E | F | G | H | K | I | L | M | N | O | P | Q | C1 | C2 | C3 | C4 | C5 | C6 |
| 0 | END OF TRANSMISSION | | | | | | | | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | X | | | | | | | | | X | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 |
| 2 | X | | | | | | | | | | X | | | | | | 0 | 1 | 0 | 0 | 0 | 0 |
| 3 | X | | | | | | | | | | | X | | | | | 1 | 1 | 0 | 0 | 0 | 0 |
| 4 | X | | | | | | | | | | | | X | | | | 0 | 0 | 1 | 0 | 0 | 0 |
| 5 | X | | | | | | | | | | | | | X | | | 1 | 0 | 1 | 0 | 0 | 0 |
| 6 | X | | | | | | | | | | | | | | X | | 0 | 1 | 1 | 0 | 0 | 0 |
| 7 | X | | | | | | | | | | | | | | | X | 1 | 1 | 1 | 0 | 0 | 0 |
| 8 | | X | | | | | | | X | | | | | | | | 0 | 0 | 0 | 1 | 0 | 0 |
| 9 | | X | | | | | | | | X | | | | | | | 1 | 0 | 0 | 1 | 0 | 0 |
| 10 | | X | | | | | | | | | X | | | | | | 0 | 1 | 0 | 1 | 0 | 0 |
| 11 | | X | | | | | | | | | | X | | | | | 1 | 1 | 0 | 1 | 0 | 0 |
| 12 | | X | | | | | | | | | | | X | | | | 0 | 0 | 1 | 1 | 0 | 0 |
| 13 | | X | | | | | | | | | | | | X | | | 1 | 0 | 1 | 1 | 0 | 0 |
| 14 | | X | | | | | | | | | | | | | X | | 0 | 1 | 1 | 1 | 0 | 0 |
| 15 | | X | | | | | | | | | | | | | | X | 1 | 1 | 1 | 1 | 0 | 0 |
| 16 | | | X | | | | | | X | | | | | | | | 0 | 0 | 0 | 0 | 1 | 0 |
| 17 | | | X | | | | | | | X | | | | | | | 1 | 0 | 0 | 0 | 1 | 0 |
| 18 | | | X | | | | | | | | X | | | | | | 0 | 1 | 0 | 0 | 1 | 0 |
| 19 | | | X | | | | | | | | | X | | | | | 1 | 1 | 0 | 0 | 1 | 0 |
| 20 | | | X | | | | | | | | | | X | | | | 0 | 0 | 1 | 0 | 1 | 0 |
| 21 | | | X | | | | | | | | | | | X | | | 1 | 0 | 1 | 0 | 1 | 0 |
| 22 | | | X | | | | | | | | | | | | X | | 0 | 1 | 1 | 0 | 1 | 0 |
| 23 | | | X | | | | | | | | | | | | | X | 1 | 1 | 1 | 0 | 1 | 0 |
| 24 | | | | X | | | | | X | | | | | | | | 0 | 0 | 0 | 1 | 1 | 0 |
| 25 | | | | X | | | | | | X | | | | | | | 1 | 0 | 0 | 1 | 1 | 0 |
| 26 | | | | X | | | | | | | X | | | | | | 0 | 1 | 0 | 1 | 1 | 0 |
| 27 | | | | X | | | | | | | | X | | | | | 1 | 1 | 0 | 1 | 1 | 0 |
| 28 | | | | X | | | | | | | | | X | | | | 0 | 0 | 1 | 1 | 1 | 0 |
| 29 | | | | X | | | | | | | | | | X | | | 1 | 0 | 1 | 1 | 1 | 0 |
| 30 | | | | X | | | | | | | | | | | X | | 0 | 1 | 1 | 1 | 1 | 0 |
| 31 | | | | X | | | | | | | | | | | | X | 1 | 1 | 1 | 1 | 1 | 0 |
| 32 | | | | | X | | | | X | | | | | | | | 0 | 0 | 0 | 0 | 0 | 1 |
| 33 | | | | | X | | | | | X | | | | | | | 1 | 0 | 0 | 0 | 0 | 1 |
| 34 | | | | | X | | | | | | X | | | | | | 0 | 1 | 0 | 0 | 0 | 1 |
| 35 | | | | | X | | | | | | | X | | | | | 1 | 1 | 0 | 0 | 0 | 1 |
| 36 | | | | | X | | | | | | | | X | | | | 0 | 0 | 1 | 0 | 0 | 1 |
| 37 | | | | | X | | | | | | | | | X | | | 1 | 0 | 1 | 0 | 0 | 1 |
| 38 | | | | | X | | | | | | | | | | X | | 0 | 1 | 1 | 0 | 0 | 1 |
| 39 | | | | | X | | | | | | | | | | | X | 1 | 1 | 1 | 0 | 0 | 1 |
| 40 | | | | | | X | | | X | | | | | | | | 0 | 0 | 0 | 1 | 0 | 1 |
| 41 | | | | | | X | | | | X | | | | | | | 1 | 0 | 0 | 1 | 0 | 1 |
| 42 | | | | | | X | | | | | X | | | | | | 0 | 1 | 0 | 1 | 0 | 1 |
| 43 | | | | | | X | | | | | | X | | | | | 1 | 1 | 0 | 1 | 0 | 1 |
| 44 | | | | | | X | | | | | | | X | | | | 0 | 0 | 1 | 1 | 0 | 1 |
| 45 | | | | | | X | | | | | | | | X | | | 1 | 0 | 1 | 1 | 0 | 1 |
| 46 | | | | | | X | | | | | | | | | X | | 0 | 1 | 1 | 1 | 0 | 1 |
| 47 | | | | | | X | | | | | | | | | | X | 1 | 1 | 1 | 1 | 0 | 1 |
| 48 | | | | | | | X | | X | | | | | | | | 0 | 0 | 0 | 0 | 1 | 1 |
| 49 | | | | | | | X | | | X | | | | | | | 1 | 0 | 0 | 0 | 1 | 1 |
| 50 | | | | | | | X | | | | X | | | | | | 0 | 1 | 0 | 0 | 1 | 1 |
| 51 | | | | | | | X | | | | | X | | | | | 1 | 1 | 0 | 0 | 1 | 1 |
| 52 | | | | | | | X | | | | | | X | | | | 0 | 0 | 1 | 0 | 1 | 1 |
| 53 | | | | | | | X | | | | | | | X | | | 1 | 0 | 1 | 0 | 1 | 1 |
| 54 | | | | | | | X | | | | | | | | X | | 0 | 1 | 1 | 0 | 1 | 1 |
| 55 | | | | | | | X | | | | | | | | | X | 1 | 1 | 1 | 0 | 1 | 1 |
| 56 | | | | | | | | X | X | | | | | | | | 0 | 0 | 0 | 1 | 1 | 1 |
| 57 | | | | | | | | X | | X | | | | | | | 1 | 0 | 0 | 1 | 1 | 1 |
| 58 | | | | | | | | X | | | X | | | | | | 0 | 1 | 0 | 1 | 1 | 1 |
| 59 | | | | | | | | X | | | | X | | | | | 1 | 1 | 0 | 1 | 1 | 1 |
| 60 | | | | | | | | X | | | | | X | | | | 0 | 0 | 1 | 1 | 1 | 1 |
| 61 | | | | | | | | X | | | | | | X | | | 1 | 0 | 1 | 1 | 1 | 1 |
| 62 | | | | | | | | X | | | | | | | X | | 0 | 1 | 1 | 1 | 1 | 1 |
| 63 | | | | | | | | X | | | | | | | | X | 1 | 1 | 1 | 1 | 1 | 1 |

Commands not available in the M 709A

## STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at 9V and $T_{amb}$ = 25°C

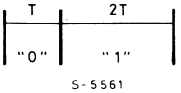
| Parameter | | Pins | Test conditions | | Values | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| $I_{DD}$ | Supply Voltage | M709 pin 24<br>M710 pin 28 | $V_{DD}$= 9V<br>IR output open | Stand-by | | 5 | 15 | µA |
| | | | | Operating (one key closed) | | 4 | 7 | mA |
| $I_{OH}$ | H State<br>IR Output Current | M709 pin 23<br>M710 pin 27 | $V_{DD}$= 9V | $V_{OH}$= 8V | -1.5 | -2.5 | | mA |
| | | | $V_{DD}$= 4.5V | $V_{OH}$= 3.5V | -0.3 | -0.5 | | |
| $I_{OL}$ | L State<br>IR Output Current | M709 pin 23<br>M710 pin 27 | $V_{DD}$= 9V | $V_{OL}$= 1V | 1.5 | -2.5 | | mA |
| | | | $V_{DD}$= 4.5V | $V_{OL}$= 1V | 0.3 | 0.5 | | |
| $V_{TH}$ | Input Threshold High | Selection inputs A to H | $V_{DD}$= 9V | | | | 6 | V |
| | | | $V_{DD}$= 4.5V | | | | 3 | |
| $V_{TL}$ | Input Threshold Low | Selection inputs K to Q | $V_{DD}$= 9V | | 3 | | | V |
| | | | $V_{DD}$= 4.5V | | 1.5 | | | |
| $I_{IL}$ | Input Low Current | Pull-up inputs A to H | $V_{DD}$= 9V<br>$V_{IL}$= 4.5V | | -60 | | -300 | µA |
| $I_{IH}$ | Input High Current | Pull-down inputs K to Q | $V_{DD}$= 9V<br>$V_{IH}$= 4.5V | | 60 | | 300 | µA |
| $I_{IH}$ | Input High Current | Address selection inputs | $V_{DD}$= 9V<br>$V_{IL}$= 8.25V<br>(oscillator running) | | | | 150 | µA |
| $I_L$ | Input Leakage Current | Trans. mode Test pin | $V_{DD}$= 9V<br>$V_{IN}$= 0 to 9V | | | | 1 | µA |
| $I_{OS}$ | Output Current | Osc. out. | $V_{DD}$= 9V<br>Osc. in. = $V_{SS}$ | | -2 | | -8 | µA |

## DESCRIPTION

The signals are transmitted with infrared light using pulse code modulation. Each word consists of 12 bits. The binary information of a bit is determined by the time interval between two pulses.
If "T" is the time base, the bits are coded as follows:

Odd bits (1, 3, etc)

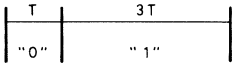
0 = T
1 = 2T



S-5561

Even bits (2, 4, etc)

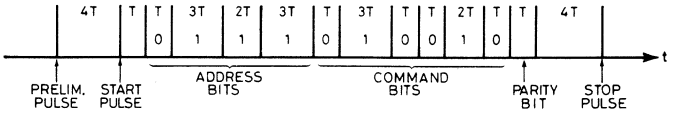
0 = T
1 = 3T



S-5552

The different code introduced for the even and odd "1s" improves the capability to recognize false codes at the receiver end. For example the double error which can cause the exchange "10" with "01" is easily detected.
A parity bit is also added in order to further increase the reliability of the transmission. This bits is "1" if the number of transmitted "1s" is even while it is "0" if the number of transmitted "1s" is odd.
In addition, every word contains a preliminary pulse, a start pulse and a stop pulse. The spacing between the preliminary and the start pulse is 4T. This is followed after 1T by 11 data pulses (one parity bit), and terminated after 4T interval by a stop pulse.
Consequently, a word in which the binary digit 0 occurs ten times has a total duration of 21T.
A word containing ten "1s" has a duration of 36T.

Example:



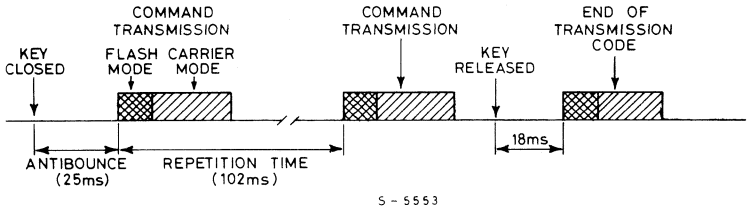
S-5542

### Synchronization between transmitter and receiver

The transmitter and the receiver can operate with different reference frequencies.
Typical values suitable for correct operation of the system should be between 445 and 510 kHz, using a cheap ceramic resonator.
Synchronization between the transmitter and the receiver, necessary to obtain the wide range of frequency tolerance described above is achieved by measuring in the receiver the interval between the start pulse and the first data pulse, storing this value and using it as time base T.

## Keyboard (pins A to Q) / Code repetition

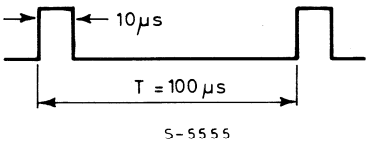
One column input (K to Q) has to be connected to one row (A to H) input to activate the transmitter. The contact must be continuously closed for a minimum of 25 ms.
Double and multiple contact operations are not accepted.
The command information is repeatedly transmitted at intervals of 102 ms ($f_{ref}$ = 500 kHz) as long as the push button remains operated.
When the contact is interrupted the circuit transmits, after a pause of about 18 ms, the "end of transmission code" and returns to stand-by mode.
If the contact is interrupted while a command is being transmitted the circuit carries on with the transmission to the end. After a pause of about 18 ms it transmits the end of transmission code.
No command is accepted until the "end of transmission code" is over.




## Transmission mode (pin 7)

The M 709/M 710 can operate in Flash (pin T = $V_{DD}$) or Carrier (pin T = $V_{SS}$) transmission modes.
Using a reference frequency of 500 kHz the output signal has these formats:

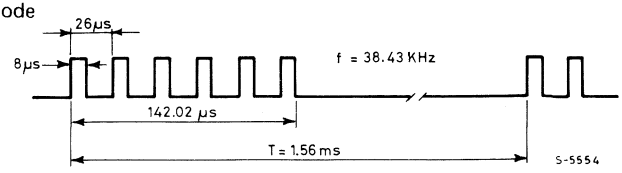
Flash mode




**Transmission time**

min. = 2.1 ms
max. = 3.6 ms
duty cycle = 0.15%

Carrier mode

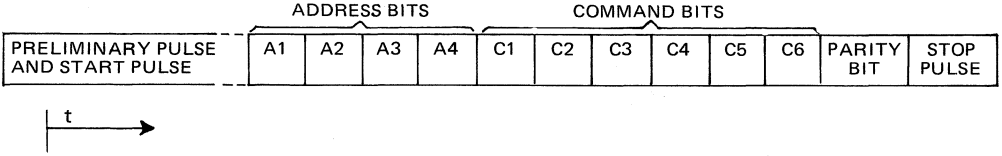



**Transmission time**

min. = 32.76 ms
max. = 56.16 ms
duty cycle = 0.7%

## Address (pins X, Y, W, Z)

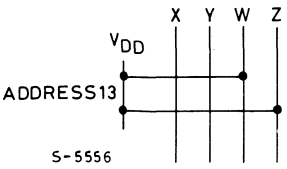
The Address information is coded and transmitted as follows:



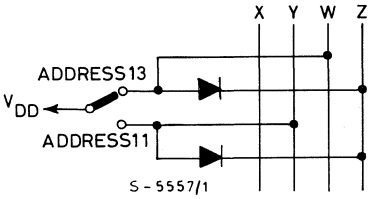

| Address number | Transmitted code | | | | Address Input code | | | |
|---|---|---|---|---|---|---|---|---|
| | A1 | A2 | A3 | A4 | X | Y | W | Z |
| 1 | 0 | 0 | 0 | 0 | L | L | L | L |
| 2 | 1 | 0 | 0 | 0 | H | L | L | L |
| 3 | 0 | 1 | 0 | 0 | L | H | L | L |
| 4 | 1 | 1 | 0 | 0 | H | H | L | L |
| 5 | 0 | 0 | 1 | 0 | L | L | H | L |
| 6 | 1 | 0 | 1 | 0 | H | L | H | L |
| 7 | 0 | 1 | 1 | 0 | L | H | H | L |
| 8 | 1 | 1 | 1 | 0 | H | H | H | L |
| 9 | 0 | 0 | 0 | 1 | L | L | L | H |
| 10 | 1 | 0 | 0 | 1 | H | L | L | H |
| 11 | 0 | 1 | 0 | 1 | L | H | L | H |
| 12 | 1 | 1 | 0 | 1 | H | H | L | H |
| 13 | 0 | 0 | 1 | 1 | L | L | H | H |
| 14 | 1 | 0 | 1 | 1 | H | L | H | H |
| 15 | 0 | 1 | 1 | 1 | L | H | H | H |
| 16 | 1 | 1 | 1 | 1 | H | H | H | H |

The address inputs have internal pull-downs which are disabled during stand-by

Single address selection



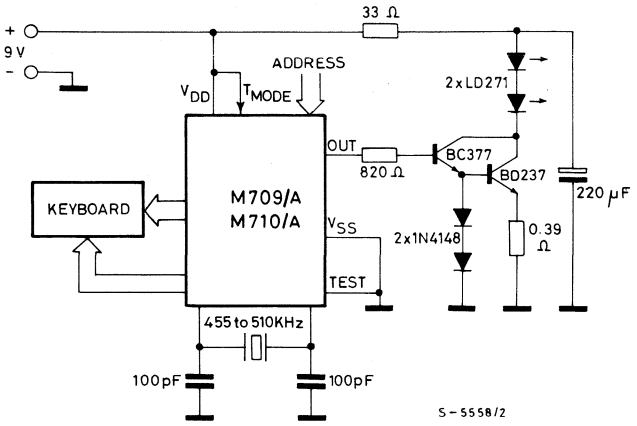

Multiple address selection




Note: unused inputs can be left open or connected to $V_{SS}$

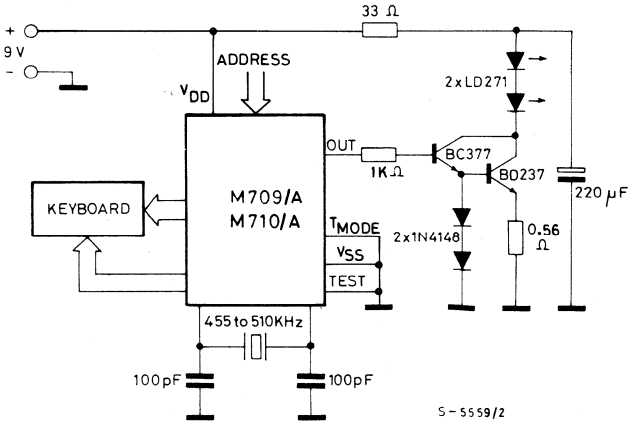
## TYPICAL APPLICATIONS

Flash mode




INFRARED DIODE PEAK CURRENT = 1.8A
TOTAL AVERAGE CONSUMPTION = 6,5 mA

Carrier mode




INFRARED DIODE PEAK CURRENT = **1.25A**
TOTAL AVERAGE CONSUMPTION = **13mA**

SGS M5450 M5451

# MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

## LED DISPLAY DRIVERS

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.
A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to $V_{DD}$ or to a separate supply of 13.2V maximum.
The M5450 and M5451 are improved pin-to-pin replacements of the NS MM 5450 and MM 5451.

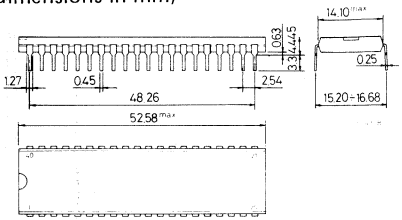
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 15 | V |
| $V_I$ | Input voltage | -0.3 to 15 | V |
| $V_{O(off)}$ | Off state output voltage | 15 | V |
| $I_O$ | Output sink current | 40 | mA |
| $P_{tot}$ | Total package power dissipation | at 25°C | 1W |
| | | at 85°C | 560 mW |
| $T_j$ | Junction temperature | 150 | °C |
| $T_{op}$ | Operating temperature range | -25 to 85 | °C |
| $T_{stg}$ | Storage temperature range | -65 to 150 | °C |

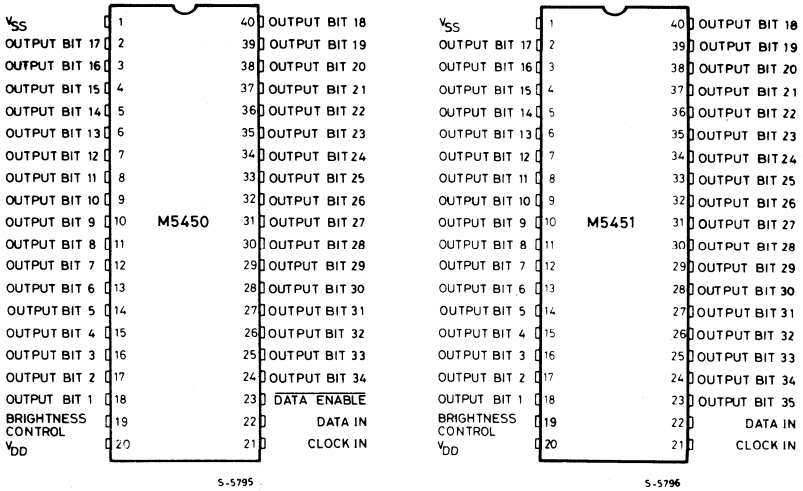
Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ORDERING NUMBERS:** M5450 B7
M5451 B7

## MECHANICAL DATA (dimensions in mm)

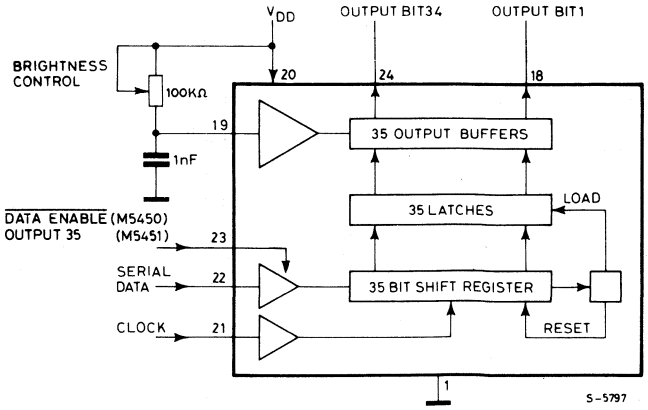



## PIN CONNECTIONS




## BLOCK DIAGRAM

Fig. 1



## STATIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ within operating range, $V_{DD}$= 4.75V to 13.2V, $V_{SS}$= 0V, unless otherwise specified)

| | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 4.75 | | 13.2 | V |
| $I_{DD}$ | Supply Current | $V_{DD}$= 13.2V | | | 7 | mA |
| VI | Input Voltage<br>Logical "0" Level<br>Logical "1" Level | ± 10 μA input bias<br>4.75 ⩽ $V_{DD}$ ⩽ 5.25<br>$V_{DD}$ > 5.25 | <br>-0.3<br>2.2<br>$V_{DD}$-2 | | <br>0.8<br>$V_{DD}$<br>$V_{DD}$ | <br>V<br>V<br>V |
| $I_B$ | Brightness Input Current (note 2) | | 0 | | 0.75 | mA |
| $V_B$ | Brightness Input Voltage (pin 19) | Input current = 750 μA | 3 | | 4.3 | V |
| $V_{O(off)}$ | Off State Out. Voltage | | | | 13.2 | V |
| $I_O$ | Out. Sink Current (note 3)<br>Segment OFF<br>Segment ON | <br>$V_O$ = 3V<br>$V_O$ = 1V (note 4)<br>Brightness In. = 0 μA<br>Brightness In. = 100 μA<br>Brightness In. = 750 μA | <br><br><br>0<br>2<br>12 | <br><br><br><br>2.7<br>15 | <br>10<br><br>10<br>4<br>25 | <br>μA<br><br>μA<br>mA<br>mA |
| $f_{clock}$ | Input Clock Frequency | | 0 | | 0.5 | MHz |
| $I_O$ | Output Matching (note 1) | | | | ± 20 | % |

**Notes :** 1. Output matching is calculated as the percent variation from $I_{MAX}$ + $I_{MIN}$/2.

2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.

3. Absolute maximum for each output should be limited to 40 mA.

4. The $V_O$ voltage should be regulated by the user. See figures 5 and 6 for allowable $V_O$ versus $I_O$ operation.

## FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current LED displays.
A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.
A block diagram is shown in figure 1. For the M5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the M5450.

## FUNCTIONAL DESCRIPTION (continued)

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.
Figure 3 shows the timing relationship between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V $V_{OUT}$.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + (V_{DD} \cdot 7\ \text{mA})\ ]\ (124\ °C/W) + T_{amb}$$

where:

$T_j$ = junction temperature (150°C max)
$V_{OUT}$ = the voltage at the LED driver outputs
$I_{LED}$ = the LED current
124°C/W = thermal coefficient of the package
$T_{amb}$ = ambient temperature

The above equation was used to plot figure 4, 5 and 6.

Fig. 2 - Input Data Format

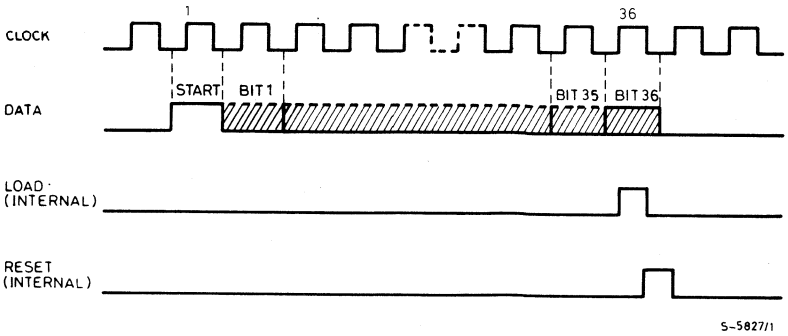


Fig. 3

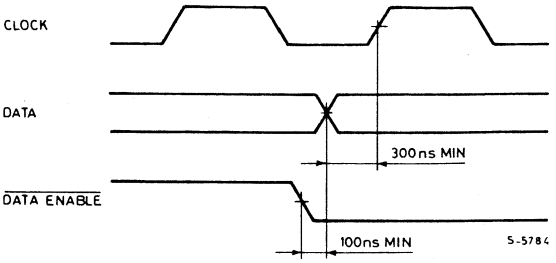



Fig. 4

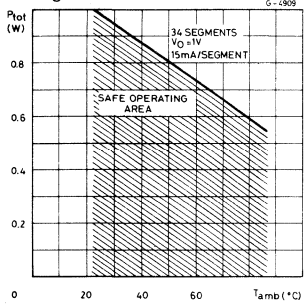



Fig. 5

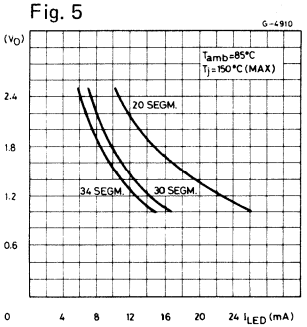
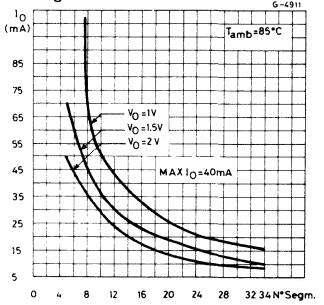
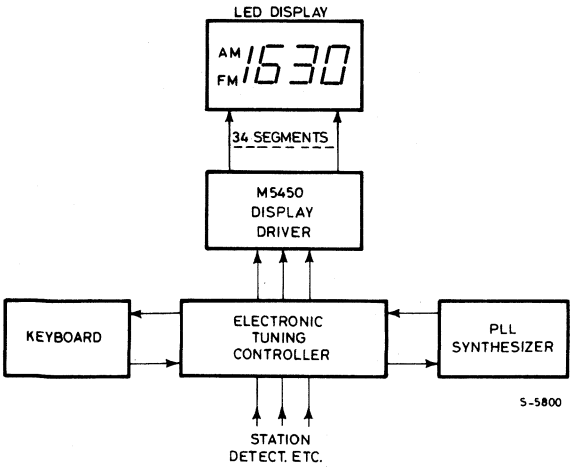



Fig. 6



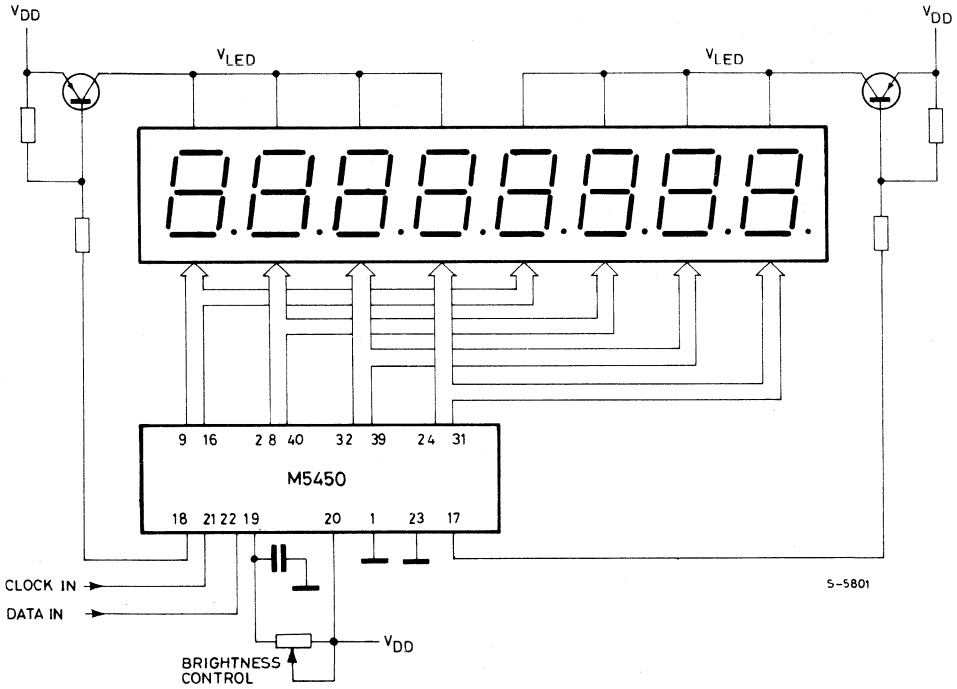

## TYPICAL APPLICATIONS

Basic electronically tuned Radio or TV system



## TYPICAL APPLICATIONS (continued)

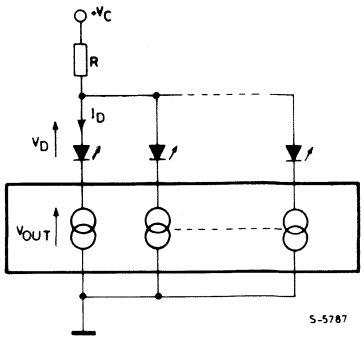
Duplexing 8 Digits with One M5450




## POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

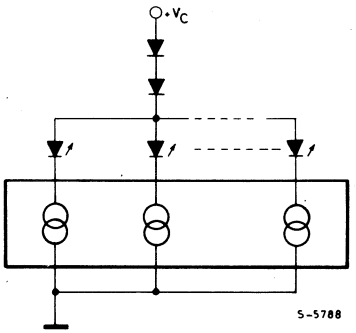


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

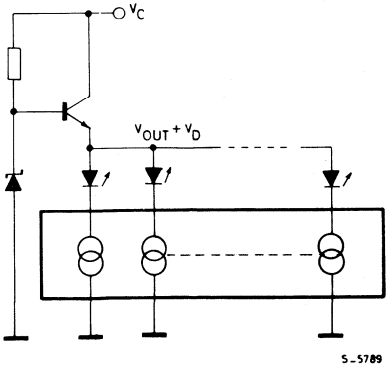
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and $P_{tot}$ limited.

b)




In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)




In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

# MOS INTEGRATED CIRCUITS

**M5480**

PRELIMINARY DATA

## LED DISPLAY DRIVER

- $3\frac{1}{2}$ DIGIT LED DRIVER (23 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- NO LOAD SIGNAL REQUIRED
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Applications Examples

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATION
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5480 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5451 die packaged in a 28-pin plastic package making it ideal for a 3½ digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to $V_{DD}$ or to a separate supply of 13.2V maximum.
The M5480 is an improved pin-to-pin replacement of the NS MM 5480.

## ABSOLUTE MAXIMUM RATINGS

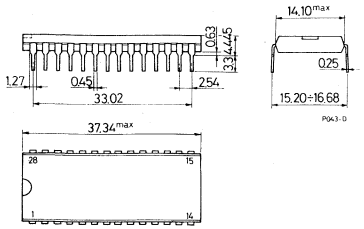
| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 15 | V |
| $V_I$ | Input voltage | -0.3 to 15 | V |
| $V_{O(off)}$ | Off state output voltage | 15 | V |
| $I_O$ | Output sink current | 40 | mA |
| $P_{tot}$ | Total package power dissipation | at 25°C | 940 mW |
| | | at 85°C | 490 mW |
| $T_j$ | Junction temperature | 150 | °C |
| $T_{op}$ | Operating temperature range | -25 to 85 | °C |
| $T_{stg}$ | Storage temperature range | -65 to 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

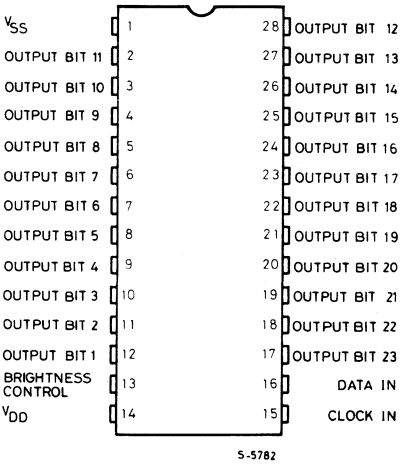
**ORDERING NUMBER:** M5480 B7

# M5480

## MECHANICAL DATA (dimension in mm)

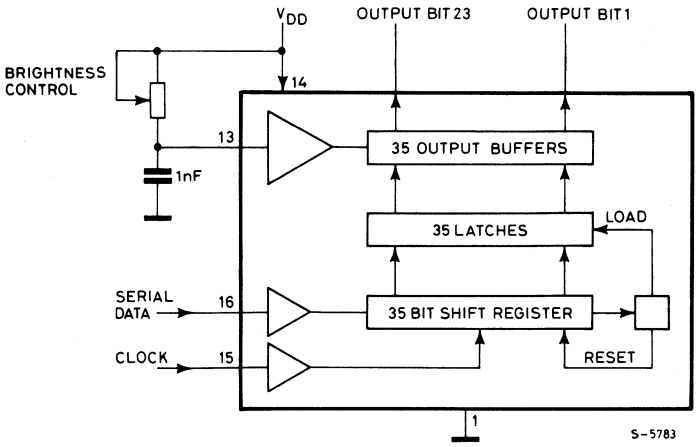



## PIN CONNECTIONS




## BLOCK DIAGRAM

Fig. 1



## STATIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ within operating range, $V_{DD}$= 4.75V to 13.2V, $V_{SS}$= 0V, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 4.75 | | 13.2 | V |
| $I_{DD}$ | Supply Current | $V_{DD}$= 13.2V | | | 7 | mA |
| $V_I$ | Input Voltages<br>Logical "0" Level<br>Logical "1" Level | ± 10 μA Input Bias<br>4.75 ⩽ $V_{DD}$ ⩽ 5.25<br>$V_{DD}$ > 5.25 | <br>-0.3<br>2.2<br>$V_{DD}$-2 | | <br>0.8<br>$V_{DD}$<br>$V_{DD}$ | <br>V<br>V<br>V |
| $I_B$ | Brightness Input Current (note 2) | | 0 | | 0.75 | mA |
| $V_B$ | Brightness Input Voltage (pin 13) | Input Current = 750 μA | 3 | | 4.3 | V |
| $V_{O(off)}$ | Off State Output Voltage | | | | 13.2 | V |
| $I_O$ | Output Sink Current (note 3)<br>Segment OFF<br>Segment ON | <br>$V_O$ = 3V<br>$V_O$ = 1V (note 4)<br>Brightness In. = 0 μA<br>Brightness In. = 100 μA<br>Brightness In. = 750 μA | <br><br><br>0<br>2<br>12 | <br><br><br><br>2.7<br>15 | <br>10<br><br>10<br>4<br>25 | <br>μA<br><br>μA<br>mA<br>mA |
| $f_{clock}$ | Input Clock Frequency | | 0 | | 0.5 | MHz |
| $I_O$ | Output Matching (note 1) | | | | ± 20 | % |

**Notes:** 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The $V_O$ voltage should be regulated by the user.

## FUNCTIONAL DESCRIPTION

The M5480 is specifically designed to operate $3^1/_2$ digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.
Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

## FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, and Clock. A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are "Don't Care".

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V $V_{OUT}$.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (132\ °C/W) + T_{amb}$$

where:

$T_j$ = junction temperature (150°C max)
$V_{OUT}$ = the voltage at the LED driver outputs
$I_{LED}$ = the LED current
132°C/W = thermal coefficient of the package
$T_{amb}$ = ambient temperature

Fig. 2 - Input Data Format

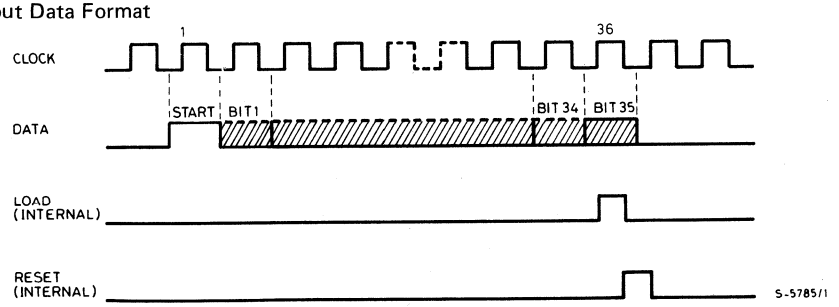



Fig. 3

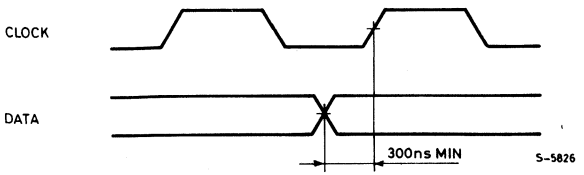
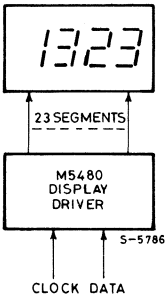


Fig. 4 - Serial Data Bus/Outputs Correspondence

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5451 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | START |
| 5480 | X | 23 | 22 | 21 | 20 | 19 | X | X | 18 | X | 17 | 16 | 15 | 14 | 13 | 12 | X | X | X | X | 11 | 10 | 9 | 8 | X | X | X | 7 | 6 | 5 | 4 | 3 | 2 | 1 | X | START |

## TYPICAL APPLICATION

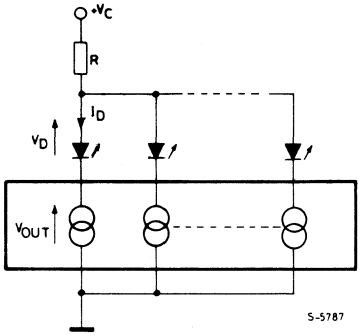
BASIC $3^1/_2$ Digit interface.




## POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

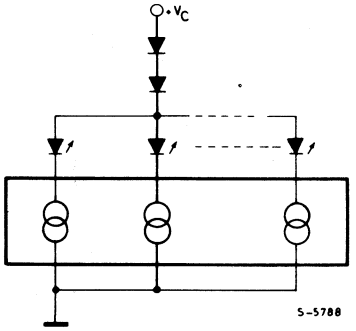



In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\ MAX} - V_{OUT\ MIN}}{N_{MAX} \cdot I_D}$$

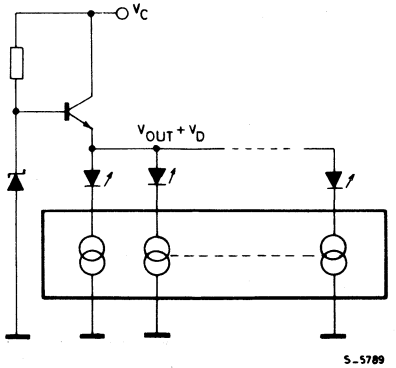
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and $P_{tot}$ limited.

b)




In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

c)




In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

# MOS INTEGRATED CIRCUITS

**M5481**

**PRELIMINARY DATA**

## LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (14 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5481 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to $V_{DD}$ or to a separate supply of 13.2V maximum.
The M5481 is an improved pin-to-pin replacement of the NS MM 5481.

## ABSOLUTE MAXIMUM RATINGS

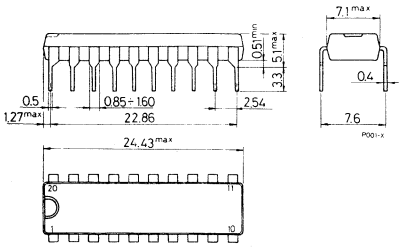
| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 15 | V |
| $V_I$ | Input voltage | -0.3 to 15 | V |
| $V_{O(off)}$ | Off state output voltage | 15 | V |
| $I_O$ | Output sink current | 40 | mA |
| $P_{tot}$ | Total package power dissipation | at 25°C | 1.5W |
| | | at 85°C | 800 mW |
| $T_j$ | Junction temperature | 150 | °C |
| $T_{op}$ | Operating temperature range | -25 to 85 | °C |
| $T_{stg}$ | Storage temperature range | -65 to 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

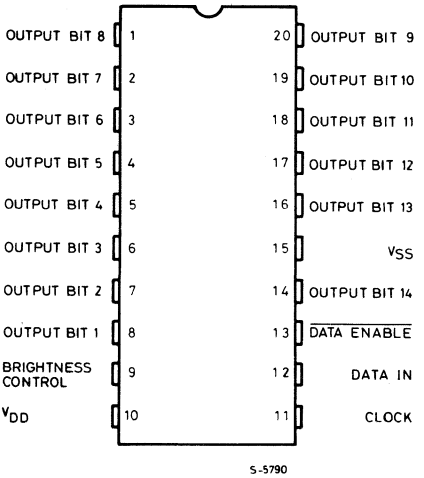
**ORDERING NUMBER:** M5481 B7

# M5481

## MECHANICAL DATA (dimensions in mm)

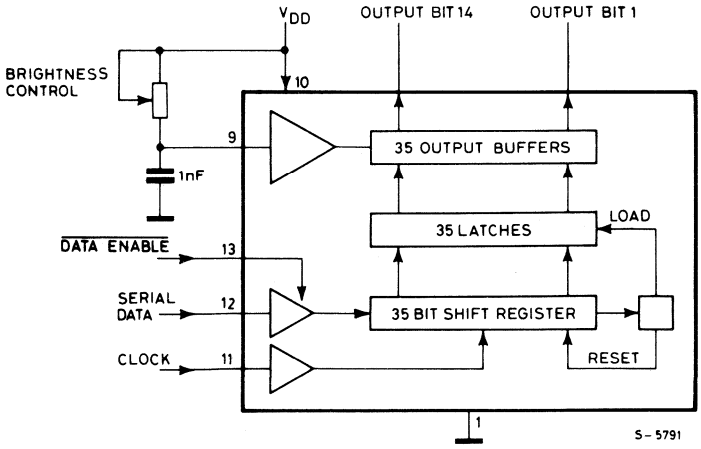



## PIN CONNECTIONS




## BLOCK DIAGRAM

Fig. 1



## STATIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ within operating range, $V_{DD}$= 4.75V to 13.2V, $V_{SS}$= 0V, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 4.75 | | 13.2 | V |
| $I_{DD}$ | Supply Current | $V_{DD}$= 13.2V | | | 7 | mA |
| $V_I$ | Input Voltages<br>Logical "0" Level<br>Logical "1" Level | <br>± 10 μA Input Bias<br>4.75 ⩽ $V_{DD}$ ⩽ 5.25<br>$V_{DD}$ > 5.25 | <br>-0.3<br>2.2<br>$V_{DD}$-2 | | <br>0.8<br>$V_{DD}$<br>$V_{DD}$ | <br>V<br>V<br>V |
| $I_B$ | Brightness Input Current (note 2) | | 0 | | 0.75 | mA |
| $V_B$ | Brightness Input Voltage (pin 9) | Input Current = 750 μA | 3 | | 4.3 | V |
| $V_{O(off)}$ | Off State Output Voltage | | | | 13.2 | V |
| $I_O$ | Output Sink Current (note 3)<br>Segment OFF<br>Segment ON | <br>$V_O$ = 3V<br>$V_O$ = 1V (note 4)<br>Brightness In. = 0 μA<br>Brightness In. = 100 μA<br>Brightness In. = 750 μA | <br><br><br>0<br>2<br>12 | <br><br><br><br>2.7<br>15 | <br>10<br><br>10<br>4<br>25 | <br>μA<br><br>μA<br>mA<br>mA |
| $f_{clock}$ | Input Clock Frequency | | 0 | | 0.5 | MHz |
| $I_O$ | Output Matching (note 1) | | | | ± 20 | % |

**Notes:** 1. Output matching is calculates as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The $V_O$ voltage should be regulated by the user.

## FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
These is an internal limiting resistor of 400Ω nominal value.

## FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data, Clock and $\overline{\text{DATA ENABLE}}$.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5481. Because it uses only 14 of the possible 35 outputs, 21 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V $V_{OUT}$.
The following equation can be used for calculations.

$$T_j \equiv [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (80\ °C/W) + T_{amb}$$

where:
$T_j$ = junction temperature (150°C max)
$V_{OUT}$ = the voltage at the LED driver outputs
$I_{LED}$ = the LED current
80°C/W = thermal coefficient of the package
$T_{amb}$ = ambient temperature

Fig. 2 - Input Data Format

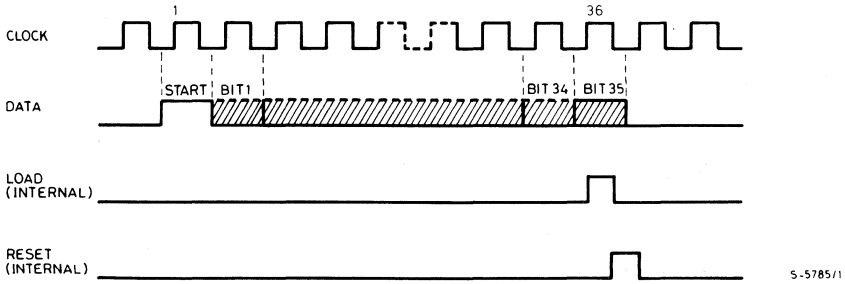



Fig. 3

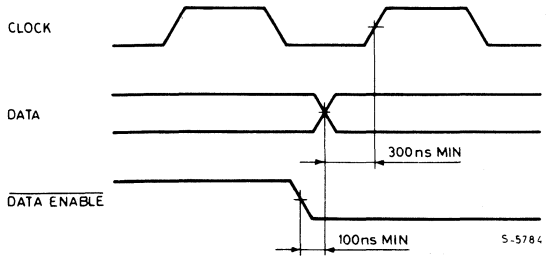
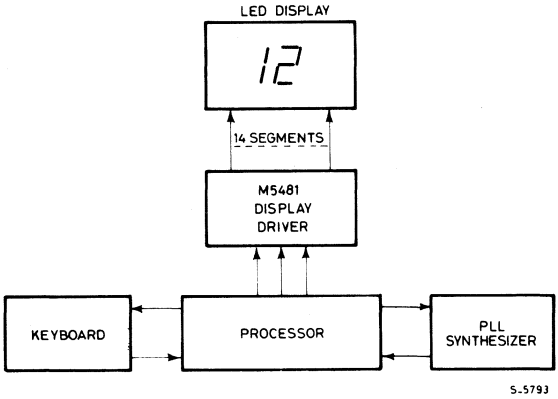


Fig. 4 - Serial Data Bus/Outputs Correspondence

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5450 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | START |
| 5481 | X | X | X | X | 14 | 13 | X | X | X | X | 12 | 11 | 10 | 9 | X | X | X | X | 8 | 7 | 6 | 5 | X | X | X | X | 4 | 3 | 2 | 1 | X | X | X | X | START |

## TYPICAL APPLICATION

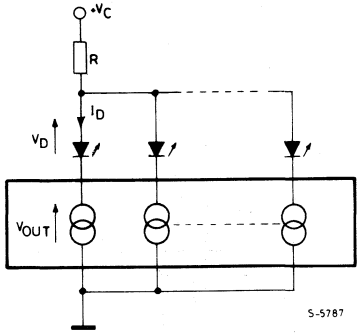
BASIC electronically tuned TV system




## POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

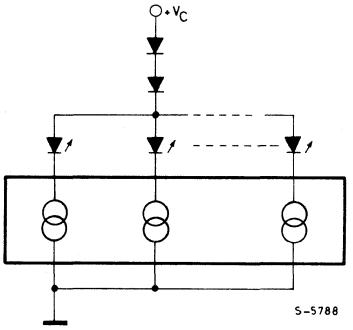



In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

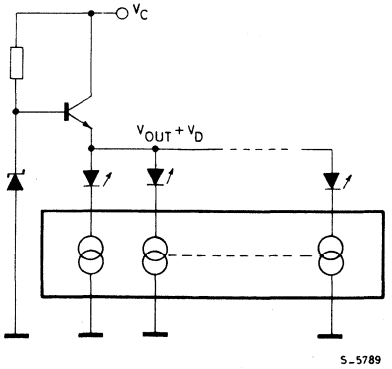
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and $P_{tot}$ limited.

b)




In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)




In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

# MOS INTEGRATED CIRCUITS

**M5482**

**PRELIMINARY DATA**

## LED DISPLAY DRIVER

- 2 DIGIT LED DRIVER (15 SEGMENTS)
- CURRENT GENERATOR OUTPUTS (NO RESISTOR REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5482 is a monolithic MOS integrated circuit produced with an N-channel silicon gate technology. It utilizes the M5451 die packaged in a 20-pin plastic package copper frame, making it ideal for a 2-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to $V_{DD}$ or to a separate supply of 13.2V maximum.

## ABSOLUTE MAXIMUM RATINGS

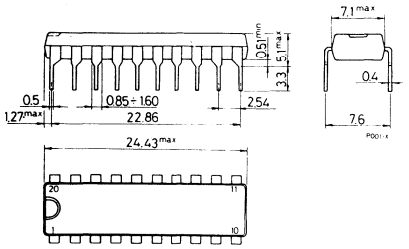
| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 15 | V |
| $V_I$ | Input voltage | -0.3 to 15 | V |
| $V_{O(off)}$ | Off state output voltage | 15 | V |
| $I_O$ | Output sink current | 40 | mA |
| $P_{tot}$ | Total package power dissipation | at 25°C | 1.5W |
| | | at 85°C | 800 mW |
| $T_j$ | Junction temperature | 150 | °C |
| $T_{op}$ | Operating temperature range | -25 to 85 | °C |
| $T_{stg}$ | Storage temperature range | -65 to 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

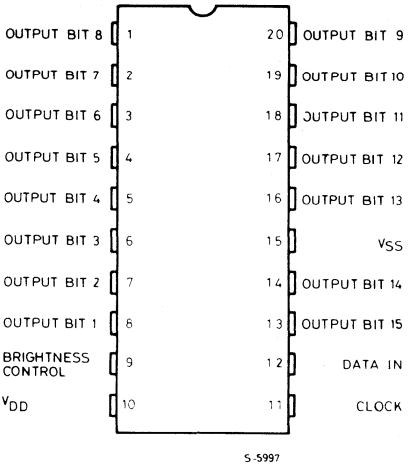
**ORDERING NUMBER:** M5482 B7

# M5482

## MECHANICAL DATA (dimensions in mm)

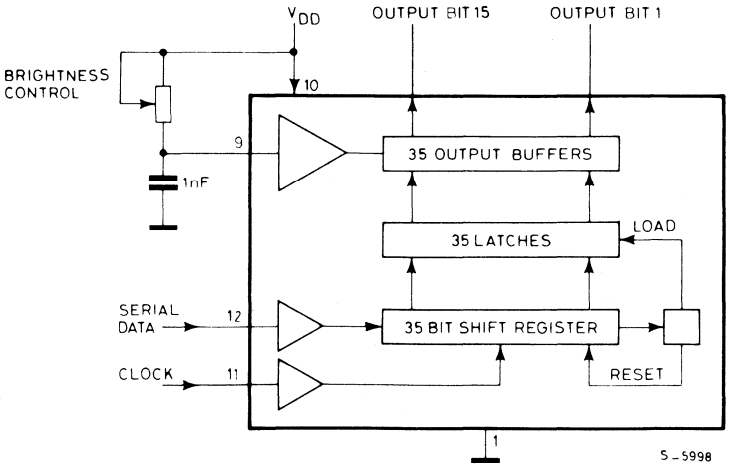



## PIN CONNECTIONS




## BLOCK DIAGRAM

Fig. 1



## STATIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ within operating range, $V_{DD}$= 4.75V to 13.2V, $V_{SS}$= 0V, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 4.75 | | 13.2 | V |
| $I_{DD}$ | Supply Current | $V_{DD}$= 13.2V | | | 7 | mA |
| $V_I$ | Input Voltages<br>Logical "0" Level<br>Logical "1" Level | ± 10 μA Input Bias<br>4.75 ⩽ $V_{DD}$ ⩽ 5.25<br>$V_{DD}$ > 5.25 | <br>-0.3<br>2.2<br>$V_{DD}$-2 | | <br>0.8<br>$V_{DD}$<br>$V_{DD}$ | <br>V<br>V<br>V |
| $I_B$ | Brightness Input Current (note 2) | | 0 | | 0.75 | mA |
| $V_B$ | Brightness Input Voltage (pin 9) | Input Current = 750 μA | 3 | | 4.3 | V |
| $V_{O(off)}$ | Off State Output Voltage | | | | 13.2 | V |
| $I_O$ | Output Sink Current (note 3)<br>Segment OFF<br>Segment ON | <br>$V_O$ = 3V<br>$V_O$ = 1V (note 4)<br>Brightness In. = 0 μA<br>Brightness In. = 100 μA<br>Brightness In. = 750 μA | <br><br><br>0<br>2<br>12 | <br><br><br><br>2.7<br>15 | <br><br>10<br><br>10<br>4<br>25 | <br><br>μA<br><br>μA<br>mA<br>mA |
| $f_{clock}$ | Input Clock Frequency | | 0 | | 0.5 | MHz |
| $I_O$ | Output Matching (note 1) | | | | ± 20 | % |

**Notes:** 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40 mA.
4. The $V_O$ voltage should be regulated by the user.

## FUNCTIONAL DESCRIPTION

The M5482 uses the M5451 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal.
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in figure 1. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.
There is an internal limiting resistor of 400Ω nominal value.

## FUNCTIONAL DESCRIPTION (continued)

Figure 2 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.
At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 3 shows the timing relationships between Data and Clock.
A maximum clock frequency of 0.5 MHz is assumed.

Figure 4 shows the Output Data Format for the M5482. Because it uses only 15 of the possible 35 outputs, 20 of the bits are "Don't Cares".

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V $V_{OUT}$.
The following equation can be used for calculations.

$$T_j \equiv [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + V_{DD} \cdot 7\ \text{mA}\ ]\ (80\ ^\circ\text{C/W}) + T_{amb}$$

where:
$T_j$ = junction temperature (150°C max)
$V_{OUT}$ = the voltage at the LED driver outputs
$I_{LED}$ = the LED current
80°C/W = thermal coefficient of the package
$T_{amb}$ = ambient temperature

Fig. 2 - Input Data Format

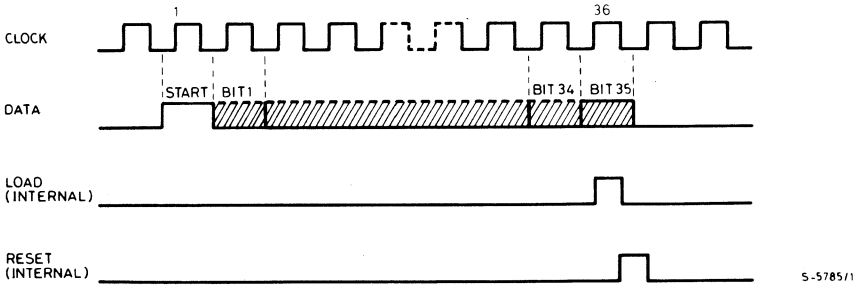



Fig. 3

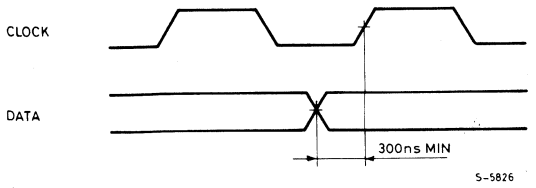
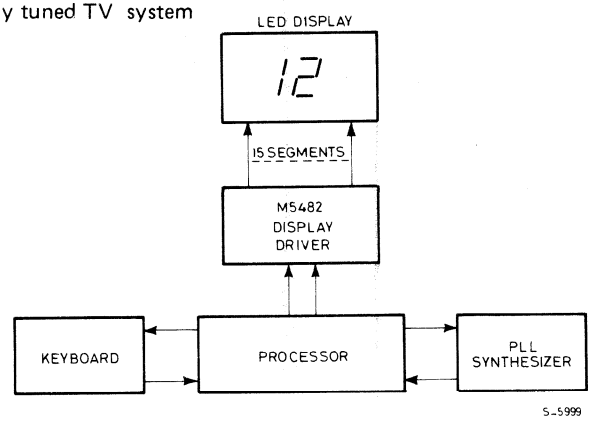


Fig. 4 - Serial Data Bus/Outputs Correspondence

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5451 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | START |
| 5482 | 15 | X | X | X | X | 14 | 13 | X | X | X | X | 12 | 11 | 10 | 9 | X | X | X | X | 8 | 7 | 6 | 5 | X | X | X | X | 4 | 3 | 2 | 1 | X | X | X | X | START |

## TYPICAL APPLICATION

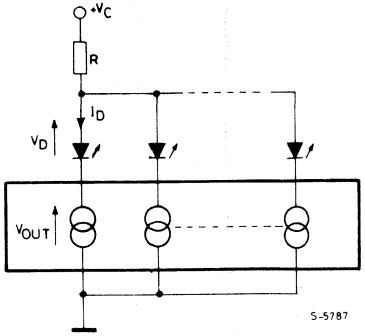
BASIC electronically tuned TV system




## POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

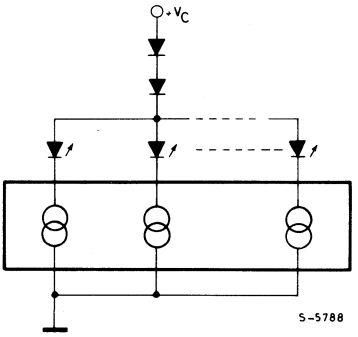



In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

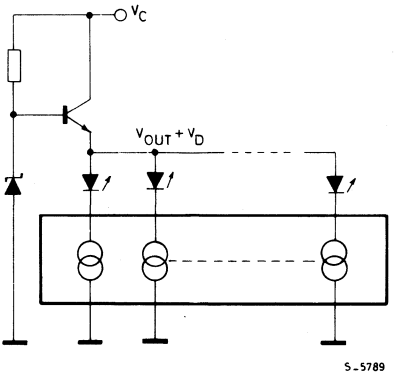
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments. In this case the current variation in the single resistor is reduced and $P_{tot}$ limited.

b)




In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)




In this configuration $V_{OUT}+V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

# MOS INTEGRATED CIRCUITS

**M5486**

PRELIMINARY DATA

## LED DISPLAY DRIVER

- 33 OUTPUTS, 15 mA SINK CAPABILITY
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT-OUTPUT
- ENABLE INPUT
- CASCADE OPERATION CAPABILITY
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

The M5486 is a monolithic MOS integrated circuits produced with an N-channel silicon gate technology. It is available in a 40-pin dual in-line plastic package.
A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to $V_{DD}$ or to a separate supply of 13.2V maximum.
The M5486 is an improved pin-to-pin replacement of the NS MM 5486.

## ABSOLUTE MAXIMUM RATINGS

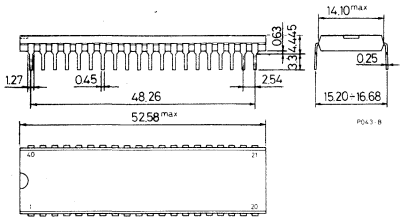
| | | | |
|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.3 to 15 | V |
| $V_I$ | Input voltage | -0.3 to 15 | V |
| $V_{O(off)}$ | Off state output voltage | 15 | V |
| $I_O$ | Output sink current | 40 | mA |
| $P_{tot}$ | Total package power dissipation | at 25°C | 1W |
| | | at 85°C | 560 mW |
| $T_j$ | Junction temperature | 150 | °C |
| $T_{op}$ | Operating temperature range | -25 to 85 | °C |
| $T_{stg}$ | Storage temperature range | -65 to 150 | °C |

Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

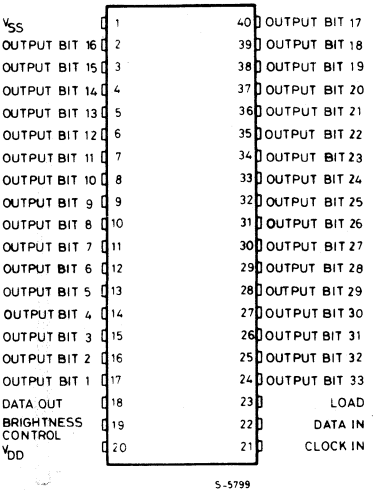
**ORDERING NUMBERS:** M5486 B7

# M5486

## MECHANICAL DATA (dimensions in mm.)

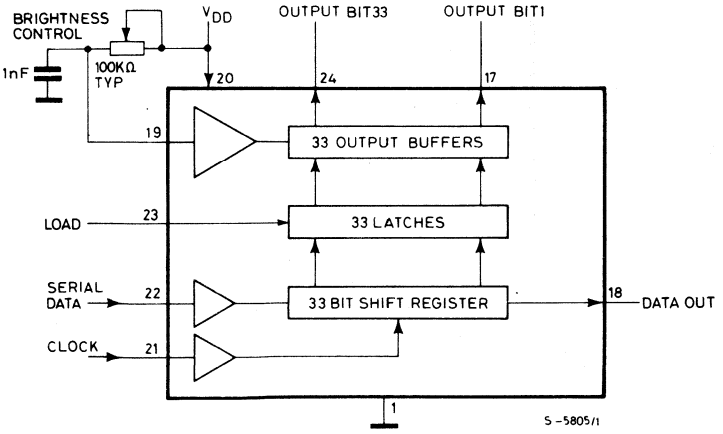



## PIN CONNECTIONS




## BLOCK DIAGRAM

Fig. 1



## STATIC ELECTRICAL CHARACTERISTICS ($T_{amb}$ within operating range, $V_{DD}$= 4.75V to 13.2V, $V_{SS}$= 0V, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 4.75 | | 13.2 | V |
| $I_{DD}$ | Supply Current | $V_{DD}$= 13.2V | | | 7 | mA |
| $V_I$ | Input Voltages<br>Logical "0" Level<br>Logical "1" Level | ± 10 μA input bias<br>4.75 ⩽ $V_{DD}$ ⩽ 5.25<br>$V_{DD}$ > 5.25 | <br>-0.3<br>2.2<br>$V_{DD}$-2 | | <br>0.8<br>$V_{DD}$<br>$V_{DD}$ | <br>V<br>V<br>V |
| $I_B$ | Brightness Input Current (note 2) | | 0 | | 0.75 | mA |
| $V_B$ | Brightness Input Voltage (pin 19) | Input current = 750 μA | 3 | | 4.3 | V |
| $V_{O(off)}$ | Off State Out. Voltage | | | | 13.2 | V |
| $I_O$ | Out Sink Current (note 3)<br>Segment OFF<br>Segment ON | <br>$V_O$ = 3V<br>$V_O$ = 1V (note 4)<br>Brightness In. = 0 μA<br>Brightness In. = 100 μA<br>Brightness In. = 750 μA | <br><br><br>0<br>2<br>12 | <br><br><br><br>2.7<br>15 | <br>10<br><br>10<br>4<br>25 | <br>μA<br><br>μA<br>mA<br>mA |
| $f_{clock}$ | Input Clock Frequency | | 0 | | 0.5 | MHz |
| $I_O$ | Output Matching (note 1) | | | | ± 20 | % |

**Notes :** 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.

2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.

3. Absolute maximum for each output should be limited to 40 mA.

4. The $V_O$ voltage should be regulated by the user. See figures 6 and 7 for allowable $V_O$ versus $I_O$ operation.

## FUNCTIONAL DESCRIPTION

The M5486 is specifically designed to operate 4 digit displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 3 signals, serial data, clock and load.
The 33 data bits are latched by a positive pulse, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.
Display brightness is determined by control of the output current LED displays.
A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in figure 1.
The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400 Ω nominal value.

## FUNCTIONAL DESCRIPTION (continued)

Figures 2 and 3 show the input data format. Bit "1" is the first bit into the data input pin and it will appear on pin 17. A logical "1" at the input will turn on the appropriate LED.
The Load signal latches the 33 bits of the shift registers into the latches. The data out pin allows for cascading the shift registers for more than 33 output drivers.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The first clock returns the chip to its normal operation.

Figure 4 shows the timing relationship between data, clock an load. A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V $V_{OUT}$.
The following equation can be used for calculations.

$$T_j = [\ (V_{OUT})\ (I_{LED})\ (\text{No. of segments}) + (V_{DD} \cdot 7\ \text{mA})\ ]\ (124\ °C/W) + T_{amb}$$

where:

$T_j$ = junction temperature (+150°C max)
$V_{OUT}$ = the voltage at the LED driver outputs
$I_{LED}$ = the LED current
124°C/W = thermal coefficient of the package
$T_{amb}$ = ambient temperature

The above equation was used to plot figures 5, 6 and 7.

Fig. 2 - Input Data Format

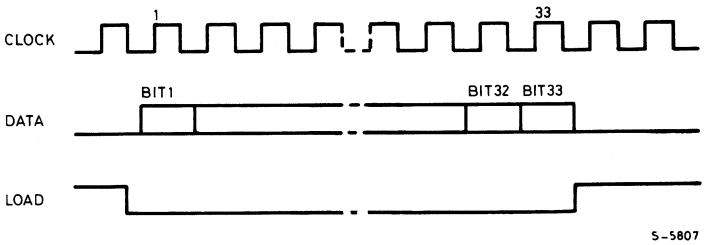



Fig. 3

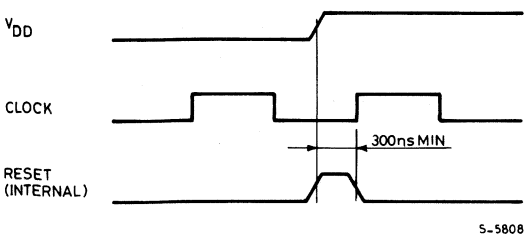


Fig. 4

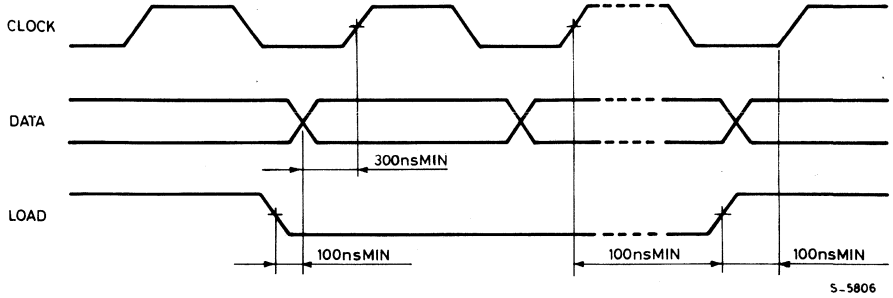



Fig. 5

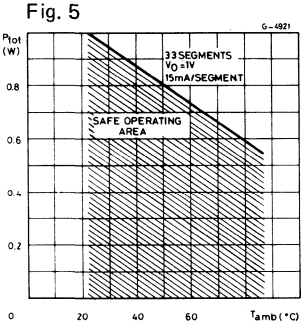



Fig. 6

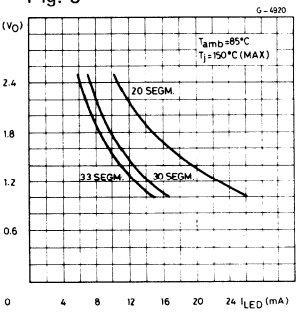
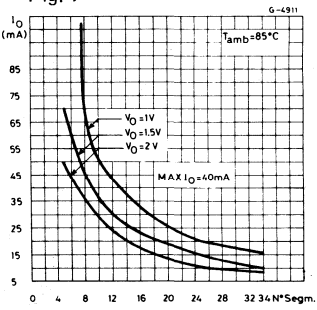
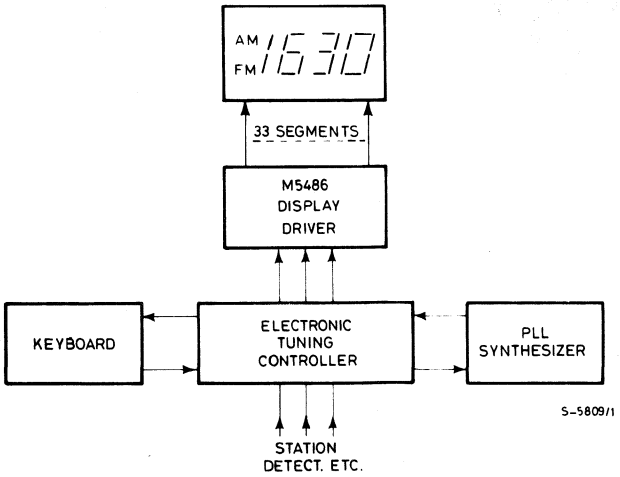



Fig. 7



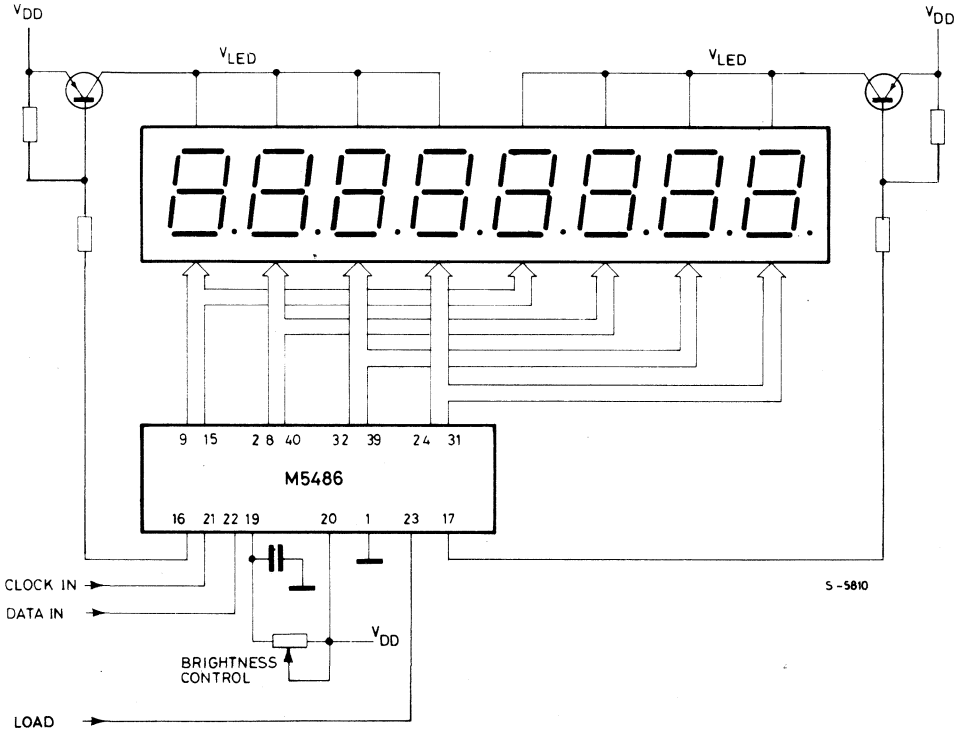

## TYPICAL APPLICATIONS

Basic electronically tuned Radio or TV system



## TYPICAL APPLICATIONS (continued)

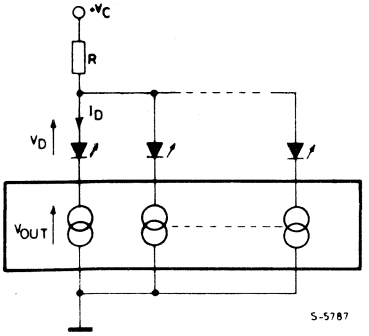
Duplexing 8 Digits with One M5486




## POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

a)

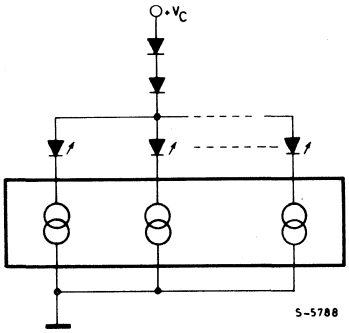


In this application R must be chosen taking into account the worst operating conditions.
R is determined by the maximum number of segments activated.

$$R = \frac{V_C - V_{D\,MAX} - V_{O\,MIN}}{N_{MAX} \cdot I_D}$$

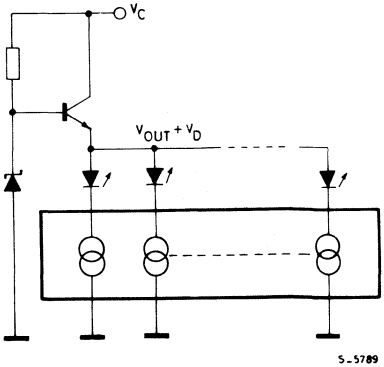
The worst case condition for the device is when roughly half of the maximum number of segments are activated.
It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.
In critical cases more resistors can be used in conjunction with groups of segments.
In this case the current variation in the single resistor is reduced and $P_{tot}$ limited.

b)




In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the IC is, in first approximation, depending only on the number of segments activated.

c)




In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

# MJE13004
# MJE13005

# MULTIEPITAXIAL MESA NPN

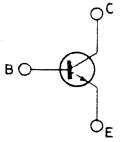
## HIGH VOLTAGE POWER SWITCH

The MJE13004/13005 are silicon multiepitaxial mesa NPN transistors in Jedec TO-220 plastic package particularly intended for switch-mode applications.

## ABSOLUTE MAXIMUM RATINGS

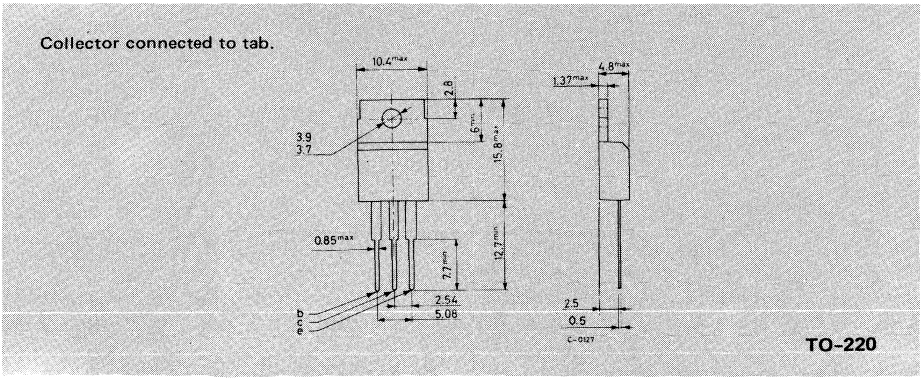
| | | MJE13004 | MJE13005 |
|---|---|---|---|
| $V_{CEV}$ | Collector-emitter voltage | 600V | 700V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B = 0$) | 300V | 400V |
| $V_{EBO}$ | Emitter-base ($I_C = 0$) | 9V | |
| $I_C$ | Collector current | 4A | |
| $I_{CM}$ | Collector peak current | 8A | |
| $I_B$ | Base current | 2A | |
| $I_{BM}$ | Base peak current | 4A | |
| $P_{tot}$ | Total power dissipation at $T_{case} \leqslant 25°C$ | 75W | |
| $T_{stg}$ | Storage temperature | -65 to 150°C | |
| $T_j$ | Junction temperature | 150°C | |

## INTERNAL SCHEMATIC DIAGRAM




## MECHANICAL DATA

Dimensions in mm



## THERMAL DATA

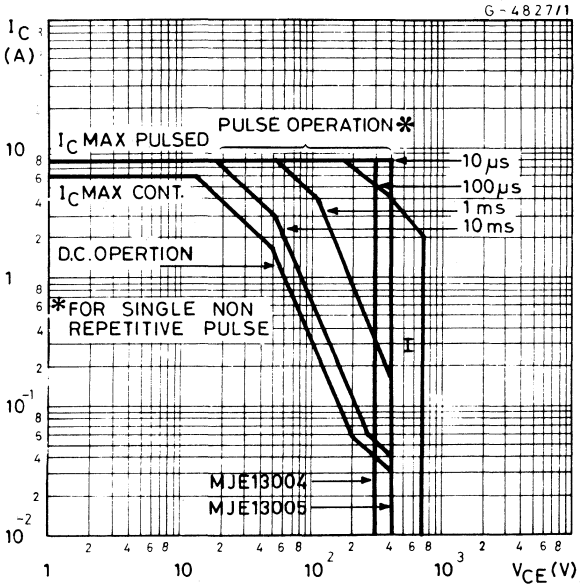
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max. | 1.67 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{case}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CEV}$ | Collector cutoff current ($V_{BE}$ = -1.5V) | for **MJE13004**<br>$V_{CE}$ = 600V<br>$V_{CE}$ = 600V $T_{case}$ = 100°C<br>for **MJE13005**<br>$V_{CE}$ = 700V<br>$V_{CE}$ = 700V $T_{case}$ = 100°C | | | 1<br>5<br><br>1<br>5 | mA<br>mA<br><br>mA<br>mA |
| $I_{EBO}$ | Emitter cutoff current ($I_C$ = 0) | $V_{EB}$ = 9V | | | 1 | mA |
| $V_{CEO(sus)}$* | Collector-emitter sustaining voltage ($I_B$ = 0) | $I_C$ = 10mA for **MJE13004**<br>for **MJE13005** | 300<br>400 | | | V<br>V |
| $V_{CE(sat)}$* | Collector-emitter saturation voltage | $I_C$ = 1A $I_B$ = 0.2A<br>$I_C$ = 2A $I_B$ = 0.5A<br>$I_C$ = 4A $I_B$ = 1A | | | 0.5<br>0.6<br>1 | V<br>V<br>V |
| $V_{BE(sat)}$* | Base-emitter saturation voltage | $I_C$ = 1A $I_B$ = 0.2A<br>$I_C$ = 2A $I_B$ = 0.5A | | | 1.2<br>1.6 | V<br>V |
| $h_{FE}$ | DC current gain | $I_C$ = 1A $V_{CE}$ = 5V<br>$I_C$ = 2A $V_{CE}$ = 5V | 10<br>8 | 30 | 60<br>40 | –<br>– |
| $t_{on}$ | Turn-on time | $I_C$ = 2A<br>$I_{B1}$ = -$I_{B2}$ = 0.4A<br>$V_{CC}$ = 250V | | | 0.8 | μs |
| $t_s$ | Storage time | | | | 4 | μs |
| $t_f$ | Fall time | | | | 0.9 | μs |

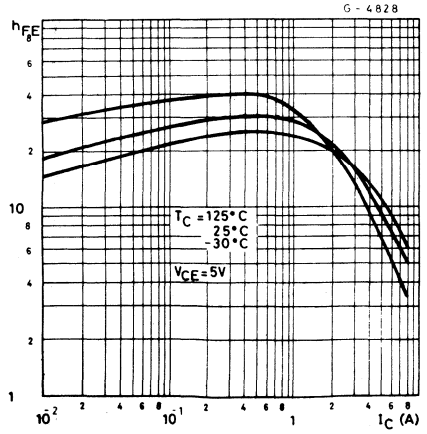
* Pulsed: pulse duration = 300 μs, duty cycle = 1.5%.

Safe operating areas

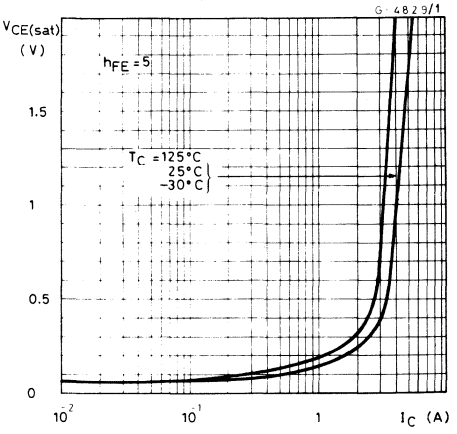



I — Area of permissible operation during turn-on provided $R_{BE} \leqslant 100\Omega$ and $t_p \leqslant 0.25\ \mu s$.

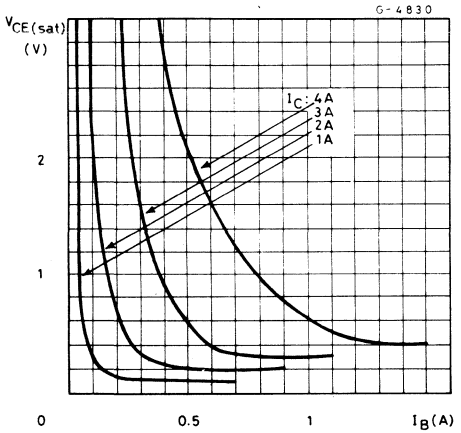
DC current gain



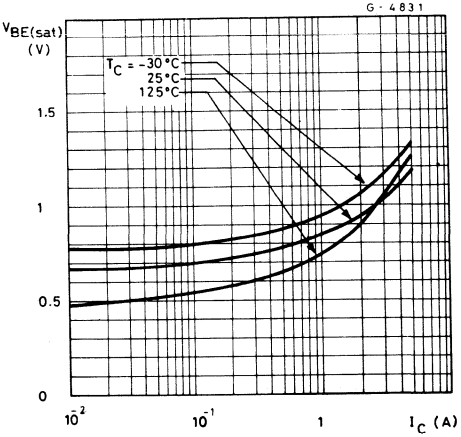

Collector-emitter saturation voltage



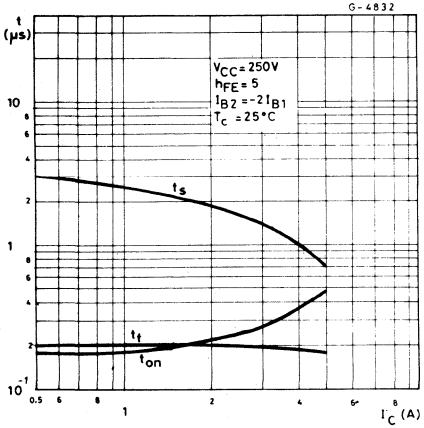
Collector-emitter saturation voltage



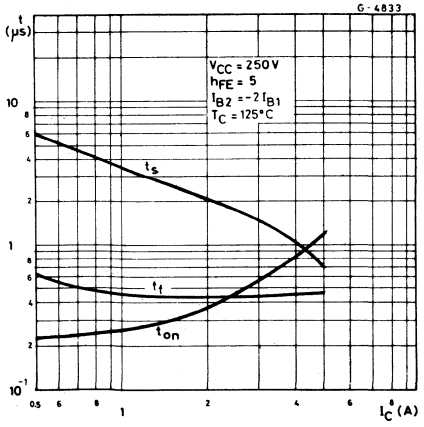

Base-emitter saturation voltage



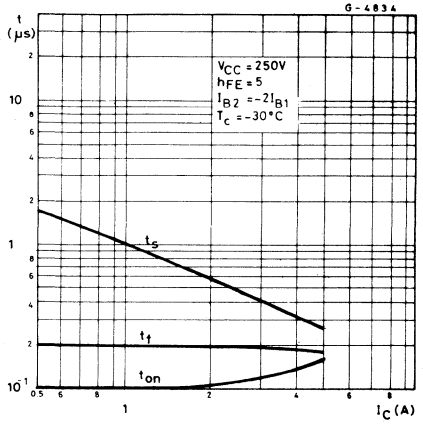

Saturated switching characteristics



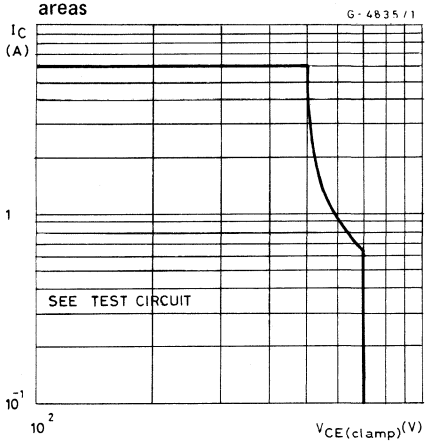

Saturated switching characteristics



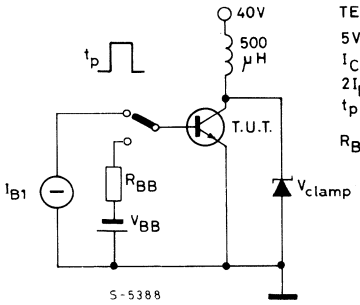
## Saturated switching characteristics




## Clamped reverse bias safe operating areas




## Clamped $E_{s/b}$ test circuit




TEST CONDITIONS ;
$5V \geq |-V_{BB}| \geq 2V$
$I_C / I_B \geq 4$
$2I_{B1} \geq |-I_{B2}| \geq I_{B1}$
$t_p$ = adjusted for nominal $I_C$
$R_{BB}$ = adjusted for $I_{B2}$

# TBA331

## GENERAL PURPOSE TRANSISTOR ARRAY

The TBA 331 is an array of 5 monolithic NPN transistors in a 14-lead dual in-line plastic package. Two transistors are internally connected to form a differential amplifier.
The transistors of the TBA 331 are well suited to low noise general purpose and to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete components in conventional circuits; in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

## ABSOLUTE MAXIMUM RATINGS

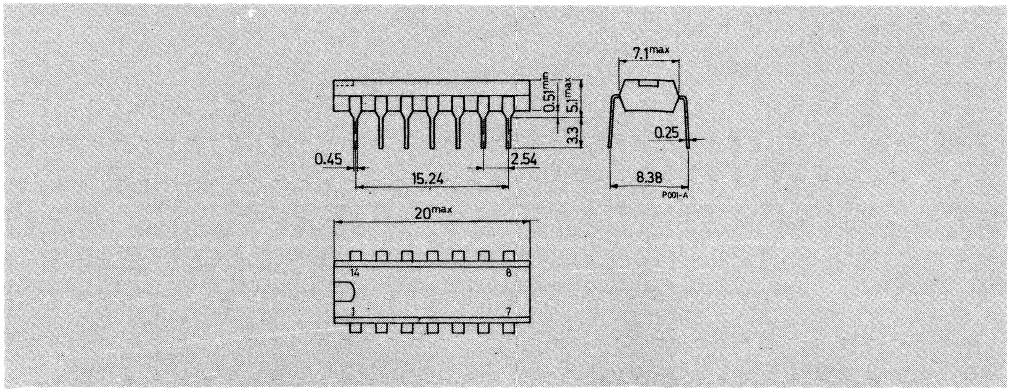
| | | Each transistor | Total package | |
|---|---|---|---|---|
| $V_{CBO}$ | Collector-base voltage ($I_E = 0$) | 20 | – | V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B = 0$) | 15 | – | V |
| $V_{CSS}$* | Collector-substrate voltage | 20 | – | V |
| $V_{EBO}$ | Emitter-base voltage ($I_C = 0$) | 5 | – | V |
| $I_C$ | Collector current | 50 | – | mA |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 55°C$ | 300 | 750 | mW |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | | °C |
| $T_{op}$ | Operating temperature | 0 to 85 | | °C |

* The collector of each transistor of the TBA 331 is isolated from the substrate by an integrated diode. The substrate (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

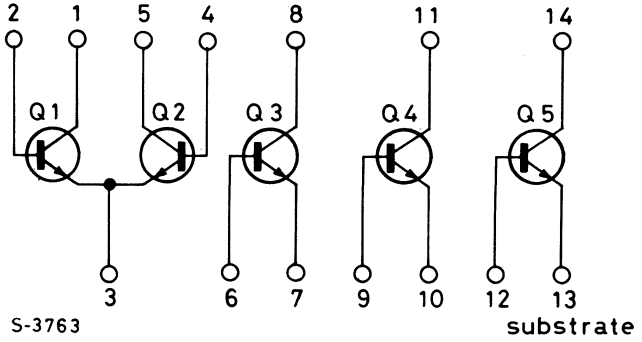
**ORDERING NUMBER:** TBA 331

## MECHANICAL DATA

Dimensions in mm



## SCHEMATIC DIAGRAM




## THERMAL DATA

| | | | each | Total |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 315° C/W | 126° C/W |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{CBO}$ | Collector cutoff current ($I_E$ = 0) | $V_{CB}$ = 10 V | | 0.002 | 40 | nA |
| $I_{CEO}$ | Collector cutoff current ($I_B$ = 0) | $V_{CE}$ = 10 V | | see curve | 0.5 | μA |
| $\lvert I_{B1}-I_{B2}\rvert$ | Input offset current | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V | | 0.3 | 2 | μA |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CBO}$ | Collector-base voltage ($I_E$ = 0) | $I_C$ = 10 μA | 20 | 60 | | V |
| $V_{CEO}$ | Collector-emitter voltage ($I_B$ = 0) | $I_C$ = 1 mA | 15 | 24 | | V |
| $V_{CSS}$ | collector-substrate voltage ($I_{CSS}$ = 0) | $I_C$ = 10 μA | 20 | 60 | | V |
| $V_{CE\ (sat)}$ | Collector-emitter saturation voltage | $I_B$ = 1 mA<br>$I_C$ = 10 mA | | 0.23 | | V |
| $V_{EBO}$ | Emitter-base voltage ($I_C$ = 0) | $I_E$ = 10 μA | 5 | 7 | | V |
| $V_{BE}$ | Base-emitter voltage | $I_E$ = 1 mA<br>$V_{CE}$ = 3 V<br>$I_E$ = 10 mA<br>$V_{CE}$ = 3 V | | 0.715<br>0.8 | | V<br>V |
| $\lvert V_{BE1}-V_{BE2}\rvert$ | Input offset voltage | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V | | 0.45 | 5 | mV |
| $\lvert V_{BE3}-V_{BE4}\rvert$ | Input offset voltage | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V | | 0.45 | 5 | mV |
| $\lvert V_{BE4}-V_{BE5}\rvert$ | Input offset voltage | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V | | 0.45 | 5 | mV |
| $\lvert V_{BE5}-V_{BE4}\rvert$ | Input offset voltage | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V | | 0.45 | 5 | mV |
| $\frac{\Delta V_{BE}}{\Delta T}$ | Base-emitter voltage temperature coefficient | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V | | -1.9 | | mV/°C |
| $\frac{\lvert V_{BE1}-V_{BE2}\rvert}{\Delta T}$ | Input offset voltage temperature coefficient | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V | | 1.1 | | μV/°C |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|---|
| $h_{FE}$ | DC current gain | $I_C$ = 10 mA<br>$V_{CE}$ = 3 V | | 100 | | – |
| | | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V | 40 | 100 | | – |
| | | $I_C$ = 10 μA<br>$V_{CE}$ = 3 V | | 54 | | – |
| $f_T$ | Transition frequency | $I_C$ = 3 mA<br>$V_{CE}$ = 3 V | 300 | 550 | | MHz |
| NF | Noise figure | $I_C$ = 100 μA<br>$V_{CE}$ = 3 V<br>f = 1 KHz<br>$R_g$ = 1 kΩ | | 3.25 | | dB |
| $H_{ie}$ | Input impedance | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V<br>f = 1 kHz | | 3.5 | | kΩ |
| $h_{fe}$ | Forward current transfer ratio | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V<br>f = 1 kHz | | 110 | | – |
| $h_{re}$ | Reverse voltage transfer ratio | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V<br>f = 1 kHz | | $1.8 \times 10^{-4}$ | | – |
| $h_{oe}$ | Output admittance | $I_C$ = 1 mA<br>$V_{CE}$ = 3V<br>f = 1 kHz | | 15.6 | | μS |
| $y_{ie}$ | Input admittance | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V<br>f = 1 MHz | | 0.3+j0.04 | | mS |
| $y_{fe}$ | Forward transadmittance | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V<br>f = 1 MHz | | 31–j1.5 | | mS |
| $y_{re}$ | Reverse transadmittance | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V<br>f = 1 MHz | | see curve | | mS |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit. |
|---|---|---|---|---|---|---|
| $Y_{oe}$ | Output admittance | $I_C$ = 1 mA<br>$V_{CE}$ = 3 V<br>f = 1 MHz | | 0.001+j0.03 | | mS |
| $C_{EBO}$ | Emitter-base capacitance | $I_C$ = 0<br>$V_{EB}$ = 3 V | | 0.6 | | pF |
| $C_{CBo}$ | Collector-base capacitance | $I_E$ = 0<br>$V_{CB}$ = 3 V | | 0.58 | | pF |
| $C_{CSS}$ | Collector-sustrate capacitance | $I_C$ = 0<br>$V_{CSS}$ = 3 V | | 2.8 | | pF |

Fig. 1 - Collector cutoff current vs ambient temperature

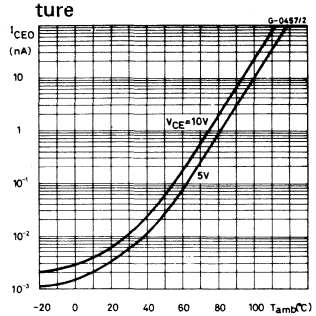



Fig. 2 - DC current gain vs. emitter current.

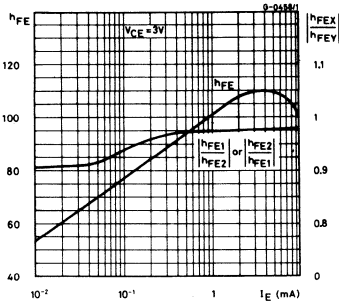



Fig. 3 - Input voltage and input offset voltage vs. emitter current

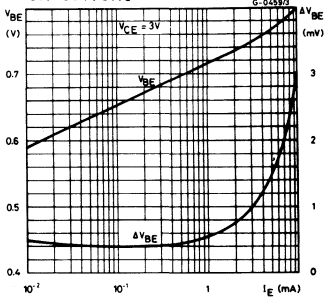



Fig. 4 - Input characteristic for each transistor

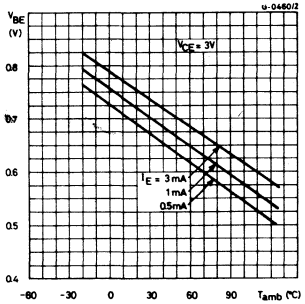



Fig. 5 - Input offset voltage vs. ambient temperature

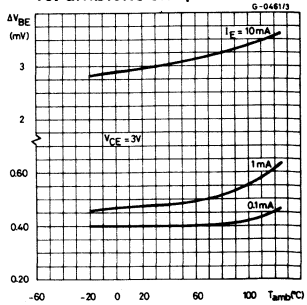



Fig. 6 - Input offset current for matched transistor pair

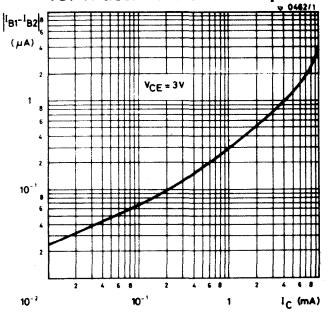


Fig. 7 - Noise figure vs collector current

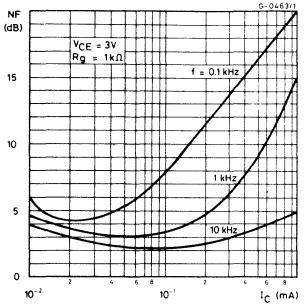



Fig. 8 - Forward admittance

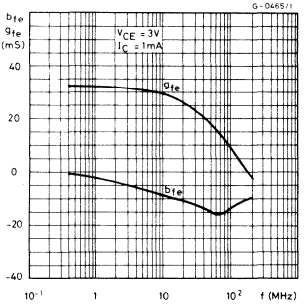



Fig. 9 - Input admittance

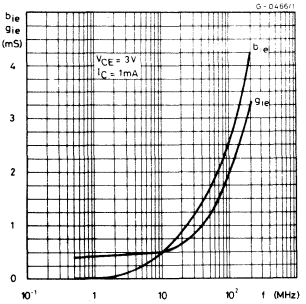



Fig. 10 - Output admittance

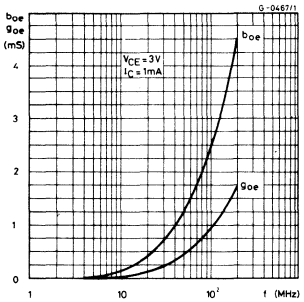



Fig. 11 - Reverse admittance

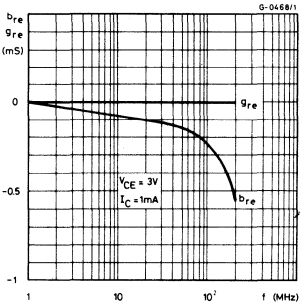
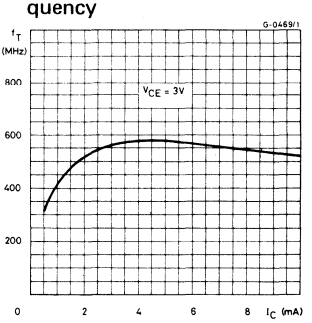



Fig. 12 - Transition frequency



# LINEAR INTEGRATED CIRCUITS

## FULLY-PROTECTED 7W AUDIO AMPLIFIER FOR CB RADIO

- HIGH OUTPUT POWER (7W AT 16V/4Ω; 14.4V/2Ω)
- HIGH OUTPUT CURRENT (3A REPETITIVE)
- LOAD DUMP PROTECTION UP TO 40V
- LOAD SHORT CIRCUIT PROTECTION UP TO $V_s$ = 15V
- POLARITY INVERSION PROTECTION
- THERMAL PROTECTION

The TBA 810CB is a monolithic integrated circuit in a 12-lead quad in-line plastic package, expressly designed for use as a power audio amplifier in CB radios.
The TBA 810 ACB has the same electrical characteristics as the TBA 810CB but its cooling tabs are flat and pierced so that an external heatsink can be easily attached.

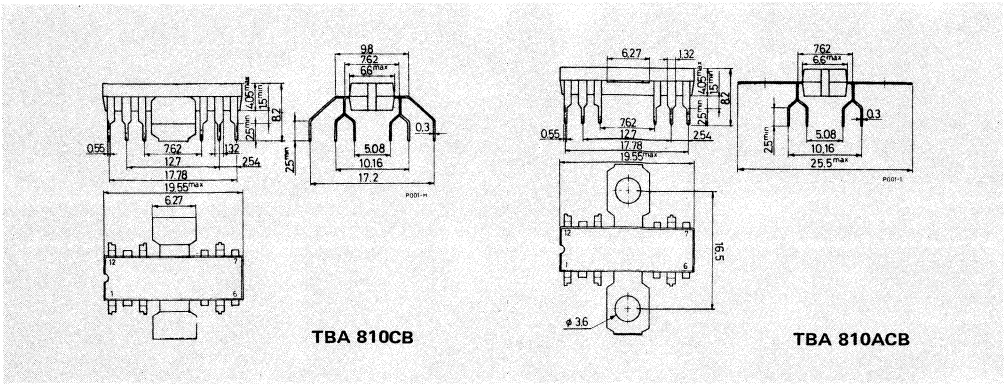
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{s(peak)}$ | Peak supply voltage (50 ms) | 40 | V |
| $V_s$ | DC supply voltage | 28 | V |
| $V_s$ | Operating supply voltage | 20 | V |
| $I_o$ | Output peak current (non repetitive) | 4 | A |
| $I_o$ | Output peak current (repetitive) | 3 | A |
| $P_{tot}$ | Power dissipation at $T_{amb} \leqslant 80°C$ (for **TBA 810CB**) | 1 | W |
| | $T_{tab} \leqslant 100°C$ (for **TBA 810ACB**) | 5 | W |
| $T_{stg}, T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TBA 810CB
TBA 810ACB

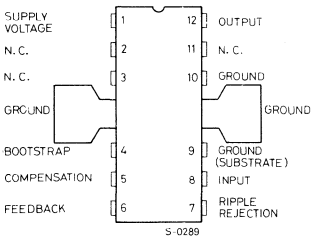
## MECHANICAL DATA

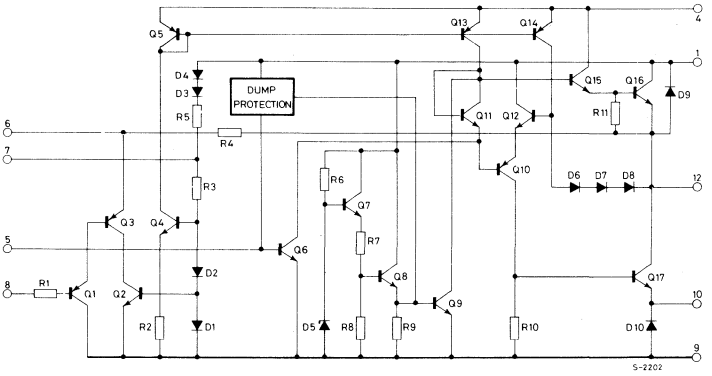
Dimensions in mm



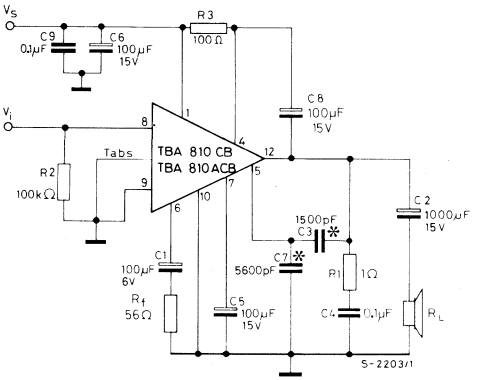
# TBA810CB

## CONNECTION AND SCHEMATIC DIAGRAMS
(top view)




## TEST AND APPLICATION CIRCUIT




*C3, C7 SEE FIG.6

## THERMAL DATA

| | | | TBA 810CB | TBA 810ACB |
|---|---|---|---|---|
| $R_{th\ j\text{-}tab}$ | Thermal resistance junction-tab | max | 12 °C/W | 10 °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70* °C/W | 80 °C/W |

* Obtained with tabs soldered to printed circuit with minimized copper area.

**ELECTRICAL CHARACTERISTICS** (Refer to the test circuit; $V_s$ = 14.4V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage (pin 1) | | 4 | | 20 | V |
| $V_o$ | Quiescent output voltage (pin 12) | | 6.4 | 7.2 | 8 | V |
| $I_d$ | Quiescent drain current | | | 12 | 20 | mA |
| $I_b$ | Input bias current (pin 8) | | | 0.4 | | μA |
| $P_o$ | Output power | d = 10% f = 1 kHz<br>$R_L$ = 4Ω<br>$R_L$ = 2Ω | <br>5.5<br>5.5 | <br>6<br>7 | | <br>W<br>W |
| $V_{i(rms)}$ | Input saturation voltage | | 220 | | | mV |
| $V_i$ | Input sensitivity | f = 1 kHz<br>$P_o$ = 6W $R_L$ = 4Ω<br>$R_f$ = 56Ω<br>$R_f$ = 22Ω<br>$P_o$ = 7W $R_L$ = 2Ω<br>$R_f$ = 56Ω<br>$R_f$ = 22Ω | | <br><br>75<br>30<br><br>55<br>20 | | <br><br>mV<br>mV<br><br>mV<br>mV |
| $R_i$ | Input resistance (pin 8) | | | 5 | | MΩ |
| B | Frequency response (-3 dB) | $R_L$ = 4Ω/2Ω<br>$C_3$ = 820 pF<br>$C_3$ = 1500 pF | | 40 to 20 000<br>40 to 10 000 | | Hz<br>Hz |
| d | Distortion | $P_o$ = 50 mW to 2.5W<br>$R_L$ = 4Ω/2Ω<br>f = 1 kHz | | 0.3 | | % |
| $G_v$ | Voltage gain (open loop) | $R_L$ = 4Ω f = 1 kHz | | 80 | | dB |
| $G_v$ | Voltage gain (closed loop) | $R_L$ = 4Ω/2Ω f = 1 kHz | 34 | 37 | 40 | dB |
| $e_N$ | Input noise voltage | $V_s$ = 16V<br>B (-3 dB) = 40 to 15 000 Hz | | 2 | | μV |
| $i_N$ | Input noise current | | | 80 | | pA |
| η | Efficiency | $P_o$ = 6W $R_L$ = 4Ω<br>f = 1 kHz | | 75 | | % |
| SVR | Supply voltage rejection | $R_L$ = 4Ω $V_{ripple}$ = 1 $V_{rms}$<br>$f_{ripple}$ = 100 Hz | 40 | 48 | | dB |

## BUILT-IN PROTECTION SYSTEMS

### Load dump protection

The load dump case occurs in a car when the engine is running and the battery is disconnected: voltage spikes on the power line are supplied by the alternator since there is no clamping effect due to battery capacitance.
The TBA 810CB was designed to withstand a pulse train on pin 1, of the type shown in Fig. 1. Providing an LC filter is included, as shown in Fig. 2, a much higher pulse train amplitude (up to 100 $V_{peak}$) is allowed on the supply line with no damage to the device.

Fig. 1

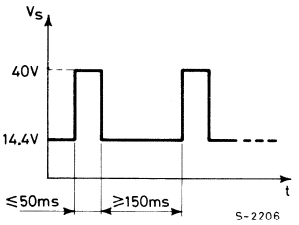
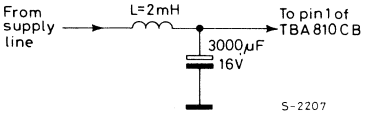



Fig. 2




### Short-circuit protection

The TBA 810CB can withstand a permanent short circuit across the load for a supply voltage up to 15V.

### Polarity inversion protection

High current (up to 5A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1A fuse (normally connected in series with the supply).
This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

### Open ground protection

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TBA 810CB, protection diodes are included to avoid any damage.

### Inductive load protection

A protection diode is provided between pin 12 and pin 1 (see the internal schematic diagram) to allow use of the TBA 810CB with inductive loads.
In particular, the TBA 810CB can drive the coupling transformer for audio modulation in CB transmitters.

### DC voltage protection

The maximum operating DC voltage on the TBA 810CB is 20V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries were series connected to crank the engine.

## BUILT-IN PROTECTION SYSTEMS (continued)

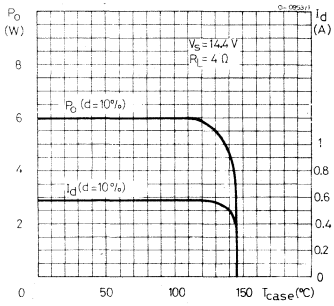
### Thermal protection

A thermal limiting circuit is internally provided on TBA 810CB to prevent chip temperature exceeding 150°C. This protection offers the following advantages:

1. An overload on the output (even if permanent), or an above-limit ambient temperature can be withstood.
2. The heatsink can be designed with smaller safety margins compared with that of a conventional power audio amplifier.

The TBA 810CB will remain undamaged in the event of excessive junction temperature: all that happens is that $P_o$ (and therefore $P_{tot}$) are reduced (Fig. 3).

Fig. 3 - Output power and drain current vs. package temperature



## 7W AUDIO AMPLIFIER

**The TBA 810P is an improvement of TBA 810S.**

It offers:
- Higher output power ($R_L = 4\Omega$ and $2\Omega$)
- Lower noise
- Polarity inversion protection
- Fortuitous open ground protection
- Higher supply voltage rejection (40 dB min.)

The TBA 810P is a monolithic integrated circuit in a 12-lead quad in-line plastic package, intended for use as a low frequency class B amplifier.
The TBA 810 P provides 7-W output power at 16V/4Ω ; 7-W at 14.4V/2Ω.
It gives high output current (up to 3A), high efficiency (75% at 6W output), very low harmonic and crossover distortion. The circuit is provided with a thermal limiting circuit and can withstand a short-circuit on the load for supply voltages up to 15V.
The TBA 810AP has the same electrical characteristics as the TBA 810P, but its cooling tabs are flat and pierced so that an external heatsink can easily be attached.

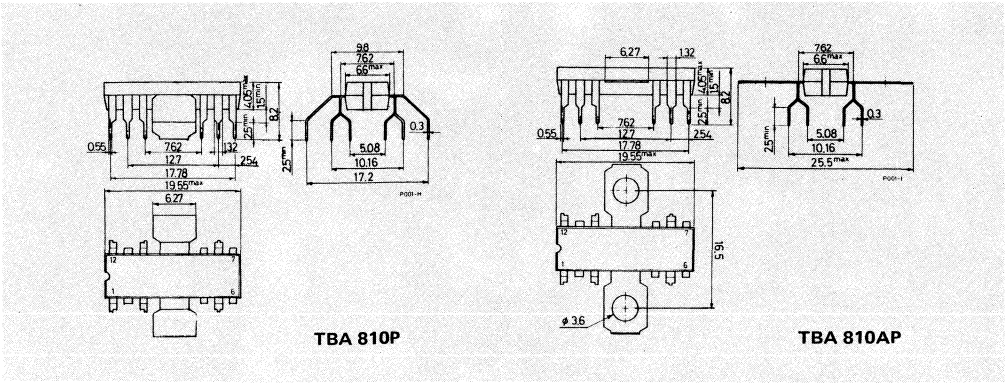
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 20 | V |
| $I_o$ | Output peak current (non repetitive) | 4 | A |
| $I_o$ | Output peak current (repetitive) | 3 | A |
| $P_{tot}$ | Power dissipation at $T_{amb} \leqslant$ 80°C (for **TBA 810P**) | 1 | W |
| | $T_{tab} \leqslant$ 100°C (for **TBA 810AP**) | 5 | W |
| $T_{stg}, T_j$ | Storage and junction temperature | -40 to 150 | °C |

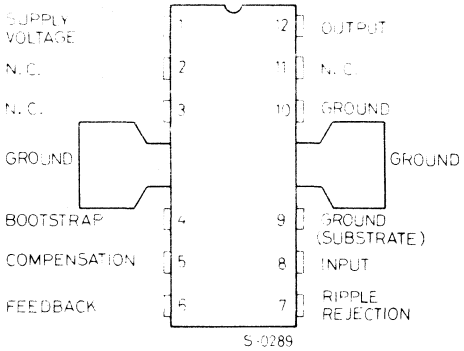
**ORDERING NUMBERS:** TBA 810P
TBA 810AP

## MECHANICAL DATA

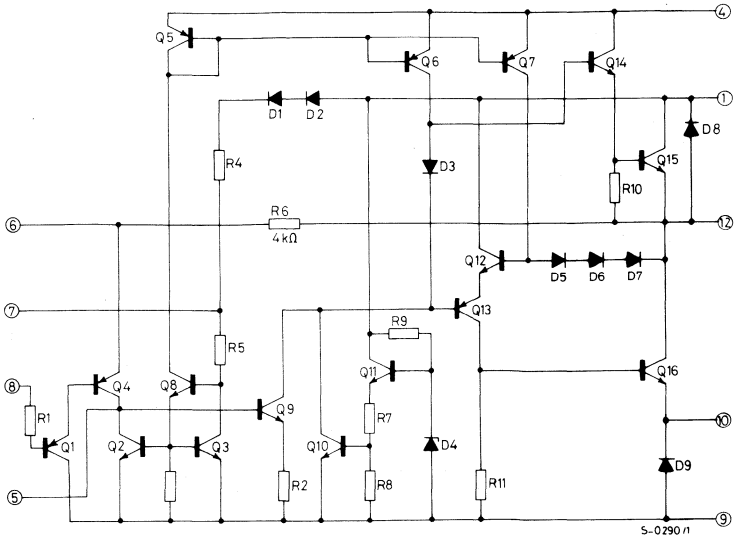
Dimensions in mm



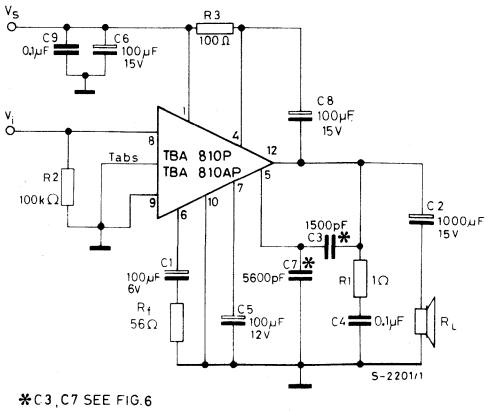
## CONNECTION DIAGRAM (top view)




## SCHEMATIC DIAGRAM



## TEST AND APPLICATION CIRCUIT




*C3, C7 SEE FIG.6

## THERMAL DATA

| | | | TBA 810P | TBA 810AP |
|---|---|---|---|---|
| $R_{th\ j\text{-}tab}$ | Thermal resistance junction-tab | max | 12°C/W | 10°C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70*°C/W | 80°C/W |

* Obtained with tabs soldered to printed circuit with minimized copper area

## ELECTRICAL CHARACTERISTICS

(Refer to the test circuit; $V_s$ = 14.4V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage (pin 1) | | 4 | | 20 | V |
| $V_o$ | Quiescent output voltage (pin 12) | | 6.4 | 7.2 | 8 | V |
| $I_d$ | Quiescent drain current | | | 12 | 20 | mA |
| $I_b$ | Input bias current | | | 0.4 | | µA |
| $P_o$ | Output power | d = 10% f = 1 kHz<br>$R_L$ = 4Ω<br>$R_L$ = 2Ω | <br>5.5<br>5.5 | <br>6<br>7 | | <br>W<br>W |
| $V_{i(rms)}$ | Input saturation voltage | | 220 | | | mV |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_i$ | Input sensitivity | f = 1 kHz<br>$P_o$ = 6W $R_L$ = 4Ω<br>$R_f$ = 56Ω<br>$R_f$ = 22Ω<br>$P_o$ = 7W $R_L$ = 2Ω<br>$R_f$ = 56Ω<br>$R_f$ = 22Ω | | <br><br>75<br>30<br><br>55<br>20 | | <br><br>mV<br>mV<br><br>mV<br>mV |
| $R_i$ | Input resistance (pin 8) | | | 5 | | MΩ |
| B | Frequency response (- 3 dB) | $R_L$ = 4Ω/2Ω<br>$C_3$ = 820 pF<br>$C_3$ = 1500 pF | | 40 to 20 000<br>40 to 10 000 | | Hz<br>Hz |
| d | Distortion | $P_o$ = 50 mW to 2.5W<br>$R_L$ = 4Ω/2Ω f = 1 kHz | | 0.3 | | % |
| $G_v$ | Voltage gain (open loop) | $R_L$ = 4Ω f = 1 kHz | | 80 | | dB |
| $G_v$ | Voltage gain (closed loop) | $R_L$ = 4Ω/2Ω f = 1 kHz | 34 | 37 | 40 | dB |
| $e_N$ | Input noise voltage | $V_s$ = 16V<br>B (-3 dB) = 40 to 15 000 Hz | | 2 | | μV |
| $i_N$ | Input noise current | | | 80 | | pA |
| η | Efficiency | $P_o$ = 6W $R_L$ = 4Ω<br>f = 1 kHz | | 75 | | % |
| SVR | Supply voltage rejection | $R_L$ = 4Ω $V_{ripple}$ = 1$V_{rms}$<br>$f_{ripple}$ = 100 Hz | 40 | 48 | | dB |
| $I_d$ | Drain current | $P_o$ = 6W $R_L$ = 4Ω | | 600 | | mA |

Fig. 1 - Output power vs. supply voltage

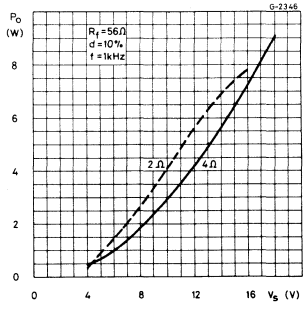



Fig. 2 - Maximum power dissipation vs. supply voltage (sine wave operation)

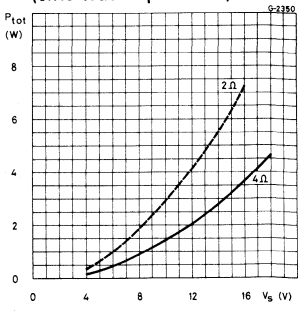
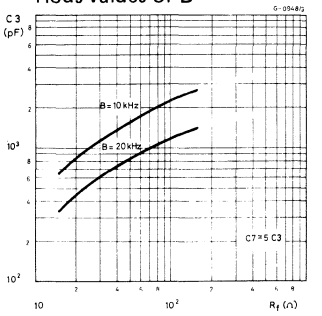



Fig. 3 - Value of C3 vs. feedback resistance for various values of B



## 7 W AUDIO AMPLIFIER

The TBA 810 S is a monolithic integrated circuit in a 12 lead quad in-line plastic package, intended for use as a low frequency class B amplifier.
The TBA 810 S provides 7 W power output at 16 V/4 Ω, 6 W at 14.4 V/4 Ω, 2.5 W at 9 V/4 Ω, 1 W at 6 V/4 Ω and works with a wide range of supply voltages (4 to 20 V); it gives high output current (up to 2.5 A), high efficiency (75% at 6 W output), very low harmonic and cross-over distortion. In addition, the circuit is provided with a thermal protection circuit.
The TBA 810 AS has the same electrical characteristics as the TBA 810S, but its cooling tabs are flat and pierced so that an external heatsink can easily be attached.

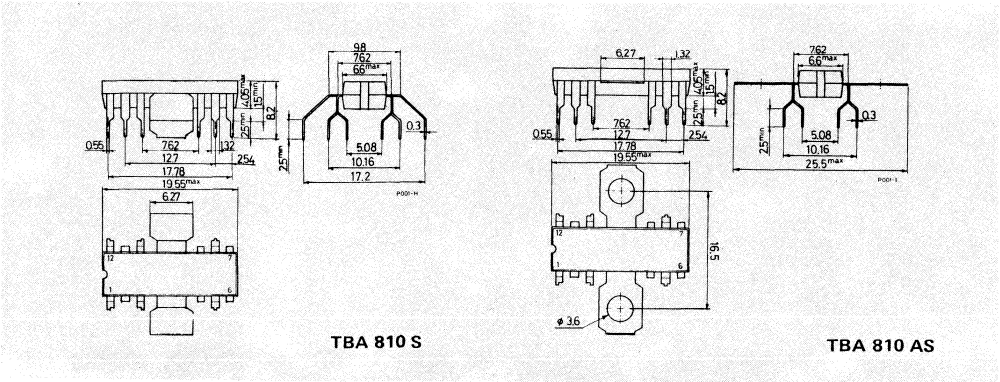
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 20 | V |
| $I_o$ | Output peak current (non-repetitive) | 3.5 | A |
| $I_o$ | Output current (repetitive) | 2.5 | A |
| $P_{tot}$ | Power dissipation: at $T_{amb}$ = 70°C | 1 | W |
| | at $T_{tab}$ = 100°C | 5 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

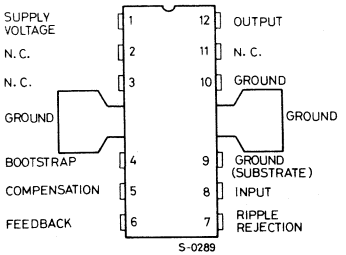
**ORDERING NUMBERS:** TBA 810 S
TBA 810 AS

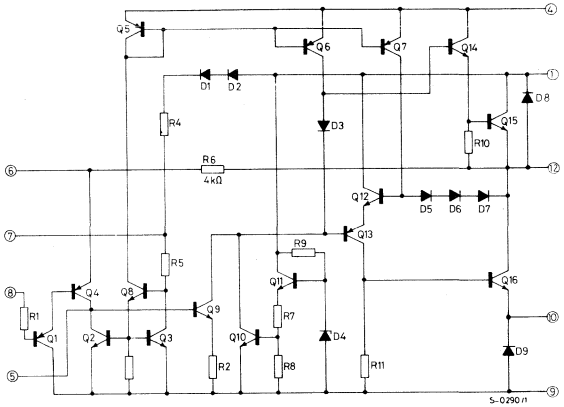
## MECHANICAL DATA

Dimensions in mm

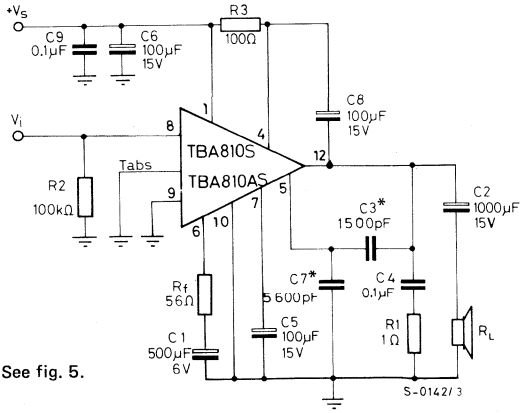


## CONNECTION AND SCHEMATIC DIAGRAM
(top view)




## TEST AND APPLICATION CIRCUIT




* See fig. 5.

## THERMAL DATA

| | | | TBA810S | TBA810AS |
|---|---|---|---|---|
| $R_{th\ j\text{-}tab}$ | Thermal resistance junction-tab | max | 12 °C/W | 10 °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70*° C/W | 80 ° C/W |

* Obtained with tabs soldered to printed circuit with minimized copper area.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit; $T_{amb}$ = 25 °C)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage (pin 1) | | 4 | | 20 | V |
| $V_o$ | Quiescent output voltage (pin 12) | | 6.4 | 7.2 | 8 | V |
| $I_d$ | Quiescent drain current | $V_s$ = 14.4V | | 12 | 20 | mA |
| $I_b$ | Bias current (pin 8) | | | 0.4 | | μA |
| $P_o$ | Power output | d = 10%<br>$R_L$ = 4Ω<br>f = 1 kHz<br>$V_s$ = 16V<br>$V_s$ = 14.4V<br>$V_s$ = 9V<br>$V_s$ = 6V | 5.5 | 7<br>6<br>2.5<br>1 | | W<br>W<br>W<br>W |
| $V_{i(rms)}$ | Input voltage | | | | 220 | mV |
| $V_i$ | Input sensitivity | $P_o$ = 6W<br>$V_s$ = 14.4V<br>$R_L$ = 4Ω<br>f = 1kHz<br>$R_f$ = 56Ω<br>$R_f$ = 22Ω | | 80<br>35 | | mV<br>mV |
| $R_i$ | Input resistance (pin 8) | | | 5 | | MΩ |
| B | Frequency response (-3 dB) | $V_s$ = 14.4V<br>$R_L$ = 4Ω<br>C3 = 820 pF<br>C3 = 1500 pF | | 40 to 20,000<br>40 to 10,000 | | Hz<br>Hz |
| d | Distorsion | $P_o$ = 50mW to 3W<br>$V_s$ = 14.4V<br>$R_L$ = 4Ω<br>f = 1kHz | | 0.3 | | % |
| $G_v$ | Voltage gain (open loop) | $V_s$ = 14.4V<br>$R_L$ = 4Ω<br>f = 1kHz | | 80 | | dB |
| $G_v$ | Voltage gain (closed loop) | $V_s$ = 14.4V<br>$R_L$ = 4Ω<br>f = 1kHz | 34 | 37 | 40 | dB |
| $e_N$ | Input noise voltage | $V_s$ = 14.4V<br>$R_g$ = 0<br>B (-3 dB) = 20Hz to 20,000 Hz | | 2 | | μV |
| $i_N$ | Input noise current | $V_s$ = 14.4V<br>B (-3 dB) = 20 Hz to 20,000 Hz | | 0.1 | | nA |
| η | Efficiency | $P_o$ = 5W<br>$V_s$ = 14.4V<br>$R_L$ = 4Ω<br>f = 1kHz | | 70 | | % |
| SVR | Supply voltage rejection | $V_s$ = 14.4V<br>$R_L$ = 4Ω<br>$f_{ripple}$ = 100 Hz | | 38 | | dB |

# TBA820M

## MINIDIP 1.2W AUDIO AMPLIFIER

The TBA 820M is a monolithic integrated audio amplifier in a 8 lead dual in-line plastic package. It is intended for use as low frequency class B power amplifier with wide range of supply voltage: 3 to 16V, in portable radios, cassette recorders and players etc. Main features are: minimum working supply voltage of 3V, low quiescent current, low number of external components, good ripple rejection, no crossover distortion, low power dissipation.
Output power: $P_o$= 2W at 12V/8Ω, 1.6W at 9V/4Ω and 1.2W at 9V/8Ω.

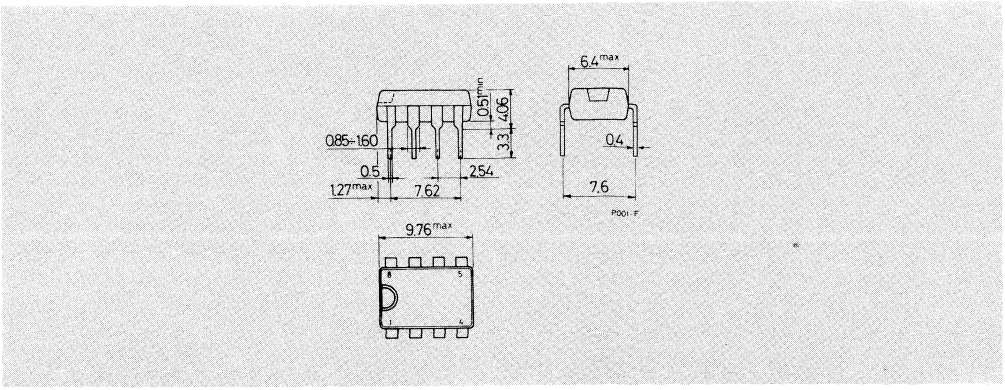
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 16 | V |
| $I_o$ | Output peak current | 1.5 | A |
| $P_{tot}$ | Power dissipation at $T_{amb}$= 50°C | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TBA 820M

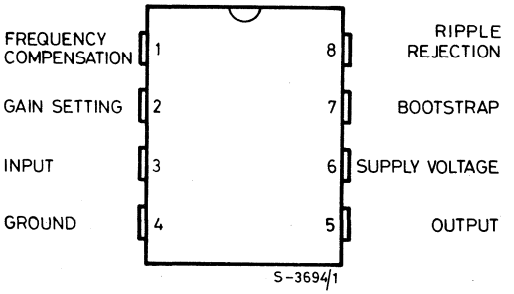
## MECHANICAL DATA

Dimensions in mm

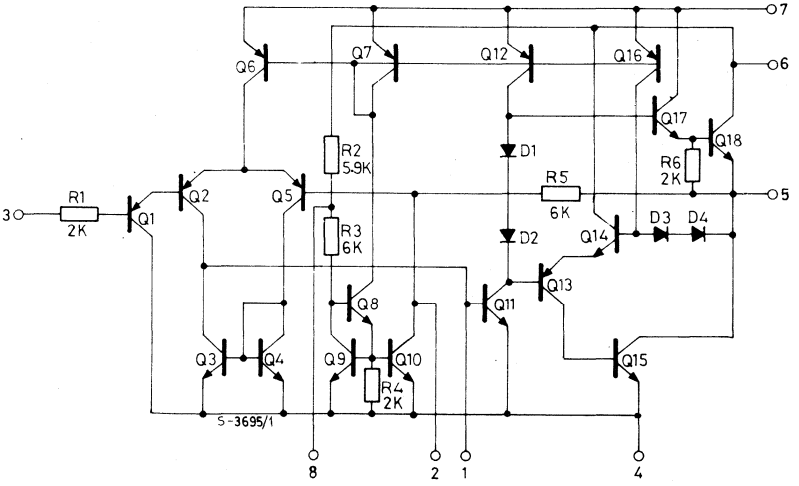


## CONNECTION DIAGRAM

(top view)




## SCHEMATIC DIAGRAM



## TEST AND APPLICATION CIRCUITS

Fig. 1 - Circuit diagram with load connected to the supply voltage.

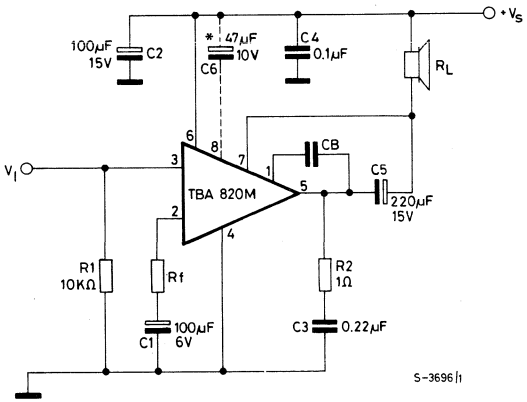
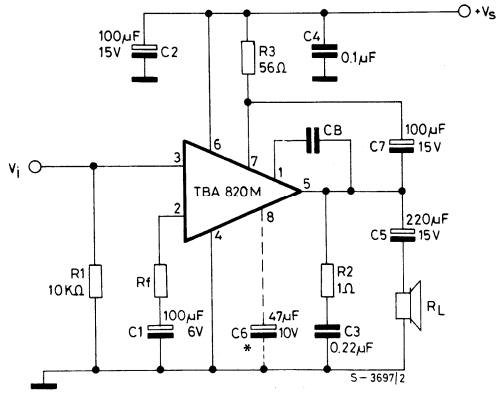



Fig. 2 - Circuit diagram with load connected to ground.




* Capacitor C6 must be used when high ripple rejection is requested.

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuits $V_s$= 9V, $T_{amb}$= 25°C unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | 3 | | 16 | V |
| $V_o$ | Quiescent output voltage (pin 5) | | | 4 | 4.5 | 5 | V |
| $I_d$ | Quiescent drain current | | | | 4 | 12 | mA |
| $I_b$ | Bias current (pin 3) | | | | 0.1 | | μA |
| $P_o$ | Output power | d = 10%<br>$R_f$= 120Ω<br>$V_s$= 12V<br>$V_s$= 9V<br>$V_s$= 9V<br>$V_s$= 6V<br>$V_s$= 3.5V<br>$V_s$= 3V | f = 1 kHz<br><br>$R_L$= 8Ω<br>$R_L$= 4Ω<br>$R_L$= 8Ω<br>$R_L$= 4Ω<br>$R_L$= 4Ω<br>$R_L$= 4Ω | 0.9 | <br><br>2<br>1.6<br>1.2<br>0.75<br>0.25<br>0.20 | | <br><br>W<br>W<br>W<br>W<br>W<br>W |
| $V_{i\ (rms)}$ | Input sensitivity | $P_o$= 1.2W<br>$R_L$= 8Ω<br>f = 1 kHz | $R_f$= 33Ω | | 16 | | mV |
| | | | $R_f$= 120Ω | | 60 | | |
| | | $P_o$= 50 mW<br>$R_L$= 8Ω<br>f = 1 kHz | $R_f$= 33Ω | | 3.5 | | mV |
| | | | $R_f$= 120Ω | | 12 | | |
| $R_i$ | Input resistance (pin 3) | f = 1 kHz | | | 5 | | MΩ |
| B | Frequency response (-3 dB) | $R_L$= 8Ω<br>$C_5$ = 1000 μF<br>$R_f$= 120Ω | $C_B$= 680 pF | 25 to 7,000 | | | Hz |
| | | | $C_B$= 220 pF | 25 to 20,000 | | | |
| d | Distortion | $P_o$= 500 mW<br>$R_L$= 8Ω<br>f = 1 kHz | $R_f$= 33Ω | | 0.8 | | % |
| | | | $R_f$= 120Ω | | 0.4 | | |
| $G_v$ | Voltage gain (open loop) | f = 1 kHz | $R_L$= 8Ω | | 75 | | dB |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $G_v$ | Voltage gain (closed loop) | $R_L$= 8Ω | $R_f$= 33Ω | | 45 | | dB |
| | | f = 1 kHz | $R_f$= 120Ω | | 34 | | |
| $e_N$ | Input noise voltage (*) | | | | 3 | | μV |
| $i_N$ | Input noise current (*) | | | | 0.4 | | nA |
| $\frac{S+N}{N}$ | Signal to noise ratio (*) | $P_o$= 1.2W<br>$R_L$= 8Ω<br>$G_v$= 34 dB | R1= 10KΩ | | 80 | | dB |
| | | | R1= 50 kΩ | | 70 | | |
| SVR | Supply voltage rejection (test circuit of fig. 2) | $R_L$= 8Ω<br>f (ripple) = 100 Hz<br>C6= 47 μF<br>$R_f$= 120Ω | | | 42 | | dB |

(*) B = 22 Hz to 22 KHz

Fig. 3 - Output power vs. supply voltage

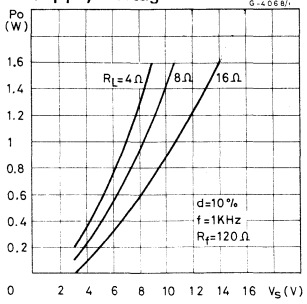



Fig. 4 - Harmonic distortion vs. output power

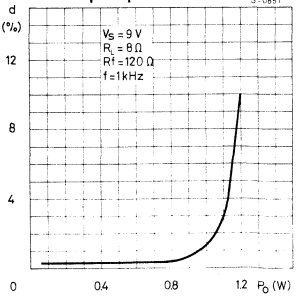



Fig.5 - Power dissipation and efficiency vs. output power

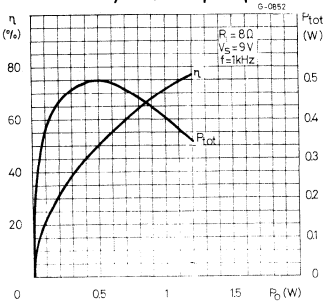


Fig. 6 - Maximum power dissipation (sine wave operation)

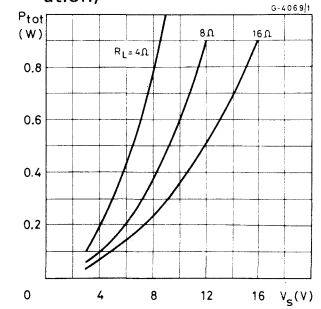



Fig. 7 - Suggested value of $C_B$ vs. $R_f$

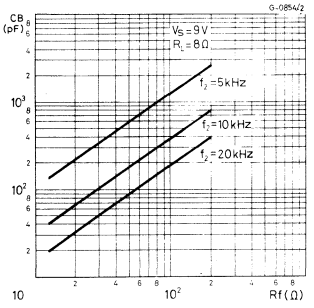



Fig. 8 - Frequency response

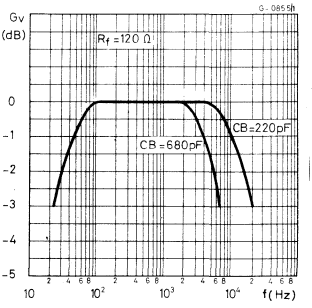



Fig. 9 - input sensitivity vs. $R_f$

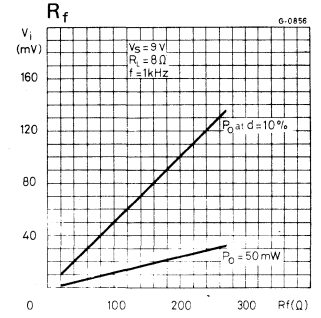



Fig. 10 - Voltage gain (closed loop) vs. $R_f$

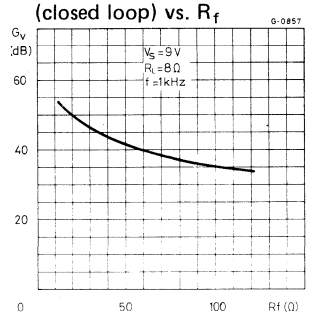



Fig. 11 - Harmonic distortion vs. frequency

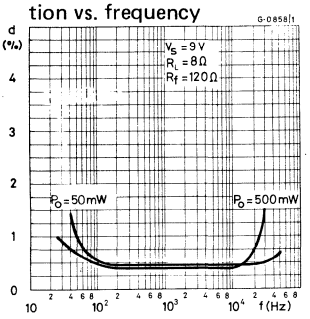



Fig. 12 - Supply voltage rejection (fig. 2 circuit)

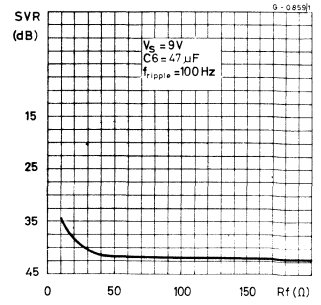



Fig. 13 - Quiescent output voltage at pin 5 vs. supply voltage

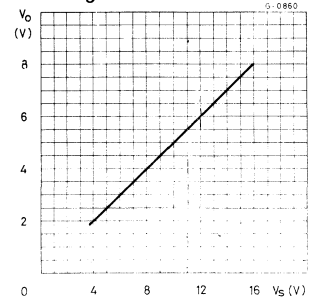
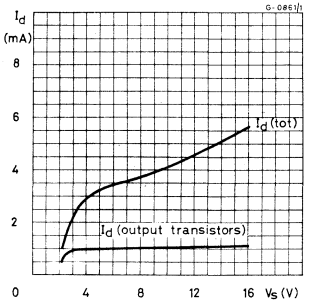



Fig. 14 - Quiescent current vs. supply voltage



## APPLICATION INFORMATION

Fig. 15 - Low cost toy AM radio (0,5 to 1,5 MHz)

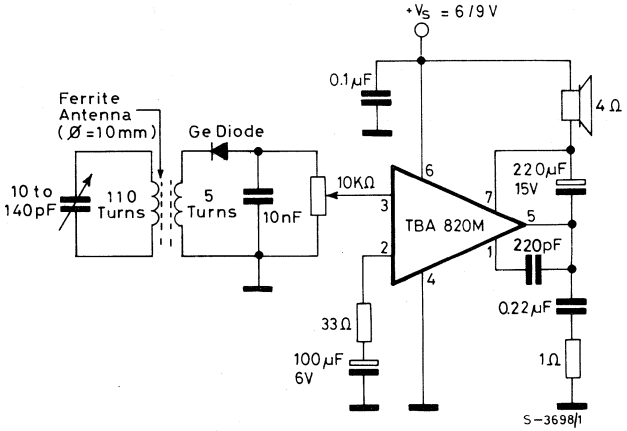
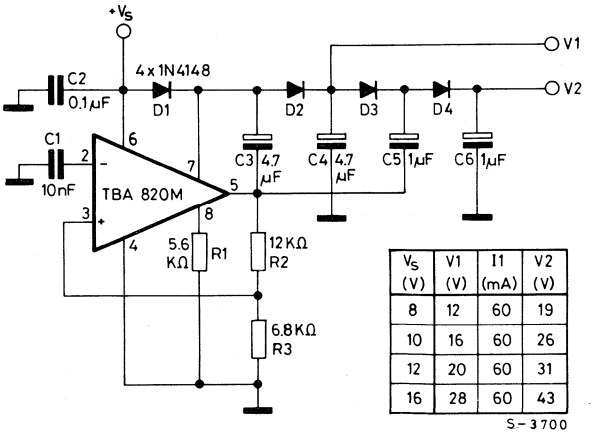



Fig. 16 - 1.5W DC/DC converter (f = 40 KHz)




| $V_S$ (V) | V1 (V) | I1 (mA) | V2 (V) |
|---|---|---|---|
| 8 | 12 | 60 | 19 |
| 10 | 16 | 60 | 26 |
| 12 | 20 | 60 | 31 |
| 16 | 28 | 60 | 43 |

## FM-IF RADIO SYSTEM

- HIGH LIMITING SENSITIVITY
- HIGH AMR
- HIGH RECOVERED AUDIO
- GOOD CAPTURE RATIO
- LOW DISTORTION
- MUTING CAPABILITY

The TCA 3089 is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It provides a complete subsystem for amplification of FM signals.
The functions incorporated are:
– FM amplification and detection
– Interchannel controlled muting
– AFC and delayed AGC for FM tuner
– Switching of stereo decoder
– Driver of a field strength meter
The TCA 3089 can be used for FM-IF amplifier application in Hi-Fi, car-radios and communication receivers.

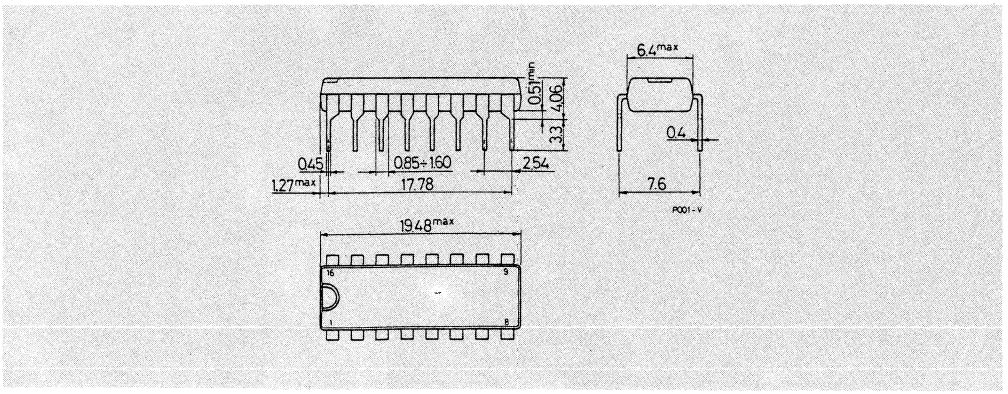
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 16 | V |
| $I_o$ | Output current (from pin 15) | 2 | mA |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 70°C$ | 800 | mW |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |
| $T_{op}$ | Operating temperature | -25 to 70 | °C |

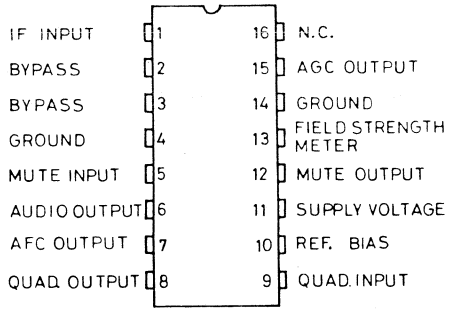
**ORDERING NUMBER:** TCA 3089

## MECHANICAL DATA

Dimensions in mm

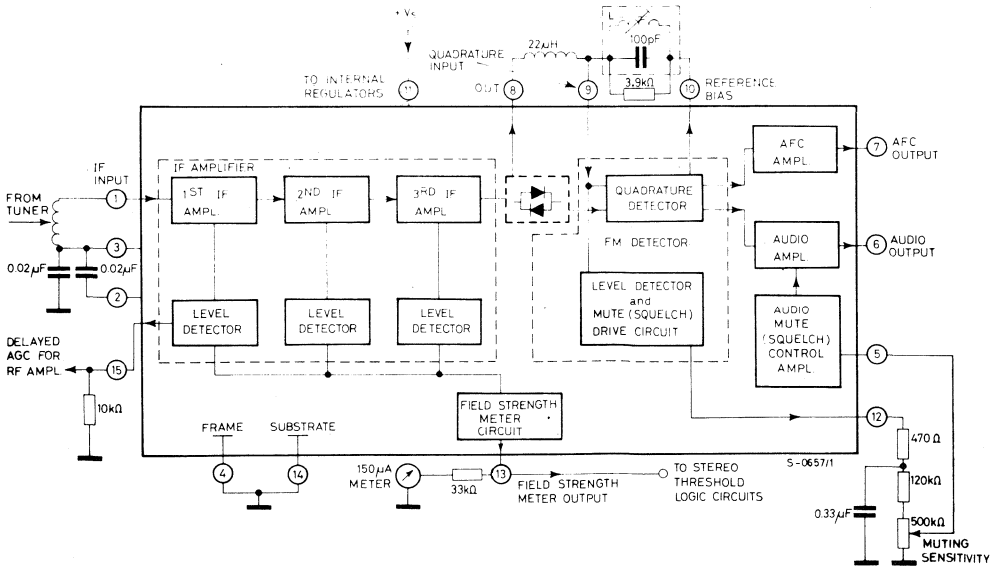


## CONNECTION DIAGRAM
(top view)

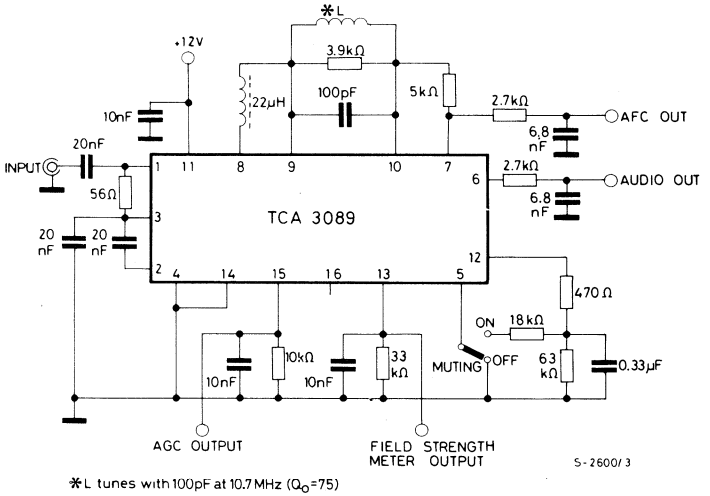



S-0398/1

## BLOCK DIAGRAM



## TEST CIRCUIT




*L tunes with 100pF at 10.7 MHz ($Q_o$=75)

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS

(Refer to the test circuit; $V_s$= 12V, $f_o$ = 10.7 MHz, $V_5$= 0V, $T_{amb}$= 25°C)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $I_s$ | Supply current | | 16 | 23 | 30 | mA |
| $V_i$ | Voltage at the IF amplifier input | | 1.2 | 1.9 | 2.4 | V |
| $V_2, V_3$ | Voltage at the input bypassing | | 1.2 | 1.9 | 2.4 | V |
| $V_6$ | Voltage at the audio output | | 5 | 5.6 | 6 | V |
| $V_{10}$ | Reference bias voltage | | 5 | 5.6 | 6 | V |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | | |
| $V_{i(threshold)}$ | Input limiting voltage (-3 dB) at pin 1 | $f_m$ = 1 kHz<br>$\Delta f$ = ± 75 kHz | | 12 | 25 | μV |
| $V_o$ | Recovered audio voltage (pin 6) | $V_i \geq 100\ \mu V$<br>$f_m$ = 1 kHz<br>$\Delta f$ = ± 75 kHz | 300 | 400 | 500 | mV |
| $V_7$ | Recovered audio voltage (pin 7) | | 200 | 350 | 500 | mV |
| d | Distortion | $V_i \geq 1$ mV<br>$f_m$ = 1 kHz<br>$\Delta f$ = ± 75 kHz | | 0.5 | 1 | % |
| $\frac{S+N}{N}$ | Signal to noise ratio | | 60 | 67 | | dB |
| AMR | Amplitude modulation rejection | $V_i$ = 100 mV<br>$f_m$ = 1 kHz<br>$\Delta f$ = ± 75 kHz<br>m = 0.3 | 45 | 55 | | dB |
| $V_i$ | Input voltage for delayed AGC action (pin 1) | | | 10 | | mV |
| $V_{15}$ | AGC output | $V_i$ = 100 mV | | | 0.5 | V |
| $\frac{\Delta I_7}{\delta f}$ | AFC control slope (note 1) | $V_i$ = 10 mV | | 1.2 | | $\frac{\mu A}{kHz}$ |
| $V_{13}$ | Field strength meter output sensitivity | $V_i$ = 0.5 mV | | 1.5 | | V |
| | No signal mute (note 2) | muting: ON | 55 | | | dB |

**Note:** 1) $\Delta I_7 = \frac{\Delta V_{7,10}}{R_{7,10}}$

2) No signal mute = $20 \log \frac{V_o @ V_i \geq 100\ \mu V}{V_o @ V_i = 0}$

Fig. 1 - Relative recovered audio and noise output vs. input voltage

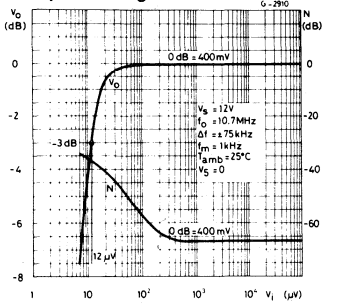



Fig. 2 - Capture ratio vs. input voltage

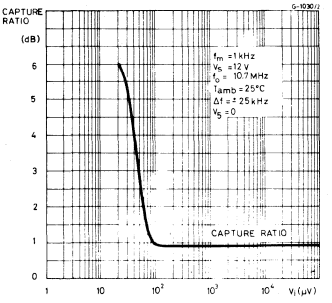



Fig. 3 - AGC ($V_{15}$) and field strength meter output ($V_{13}$) vs. input voltage

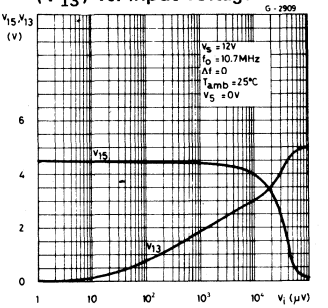



Fig. 4 - AFC output current vs. change in tuning frequency

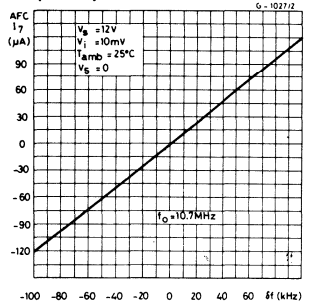



Fig. 5 - Amplitude modulation rejection vs. input voltage

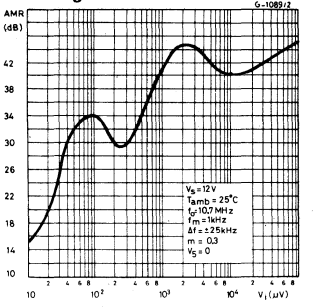
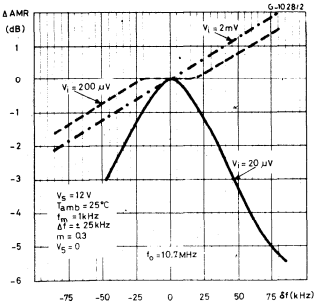



Fig. 6 - AMR vs. change in tuning frequency




## APPLICATION INFORMATION

Fig. 7 - P.C. board and component layout of the circuit of fig. 8 (1:1 scale)

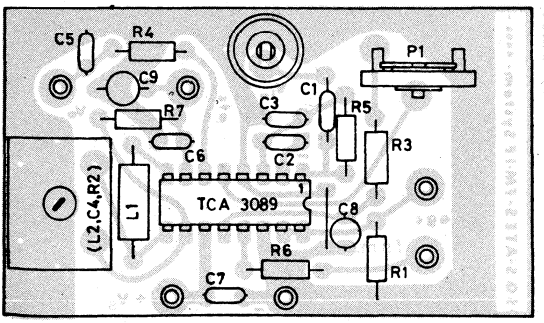
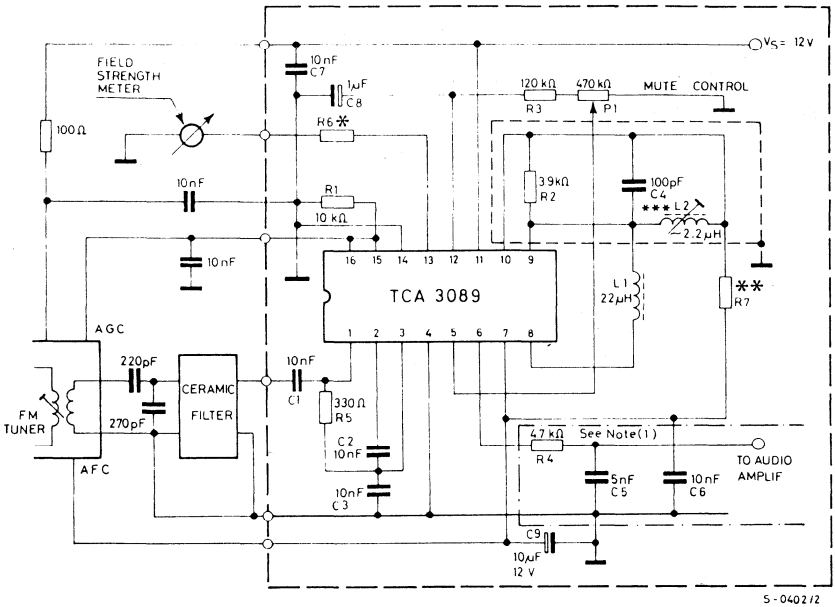
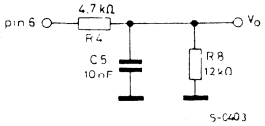


Fig. 8 - Typical application circuit




Notes (1): When $V_S$ is less than 12V, a resistor R8= 12 kΩ must be connected between audio output and ground, and the integrator capacitor C5 must be changed to 10 nF, as follows:




* Dependent on field strength meter sensitivity.
** Dependent on the tuner's AFC circuit.
*** L2 tunes with 100 pF at 10.7 MHz ($Q_o$ = 75)

# TCA3189

# LINEAR INTEGRATED CIRCUITS

## FM-IF HIGH QUALITY RADIO SYSTEM

- EXCEPTIONAL LIMITING SENSITIVITY
- VERY LOW DISTORTION (0.1% - DOUBLE TUNED DETECTOR COIL)
- IMPROVED S/N RATIO
- EXTERNALLY PROGRAMMABLE AUDIO LEVEL
- ON CHANNEL STEP FOR SEARCH CONTROL
- PROGRAMMABLE AGC VOLTAGE AND AFC FOR TUNER
- INTERCHANNEL MUTING (SQUELCH)
- DEVIATION MUTING
- DIRECT DRIVE OF TUNING METER
- DIRECT DRIVE OF FIELD STRENGTH METER

The TCA 3189 is a monolithic integrated circuit in a 16-lead dual in-line plastic package, which provides a **complete subsystem** for amplification of 10.7 MHz FM signal in Hi-Fi, car-radios and communications receivers.

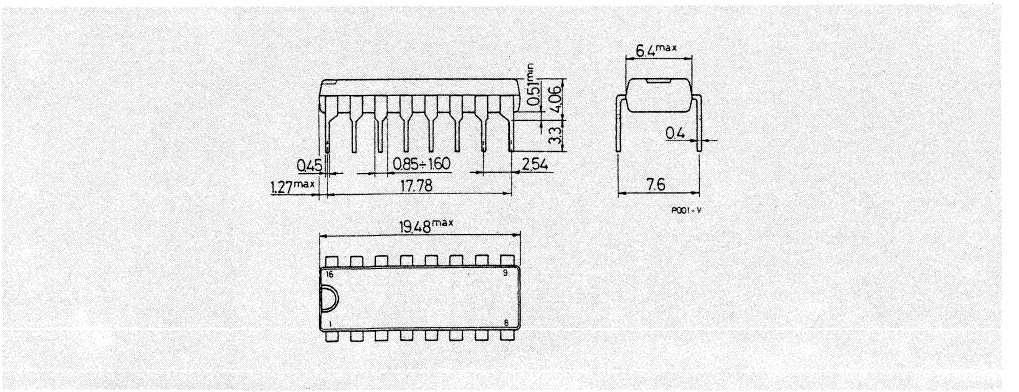
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 16 | V |
| $I_o$ | Output current (from pin 15) | 2 | mA |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 70°C$ | 800 | mW |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |
| $T_{op}$ | Operating temperature | -25 to 85 | °C |

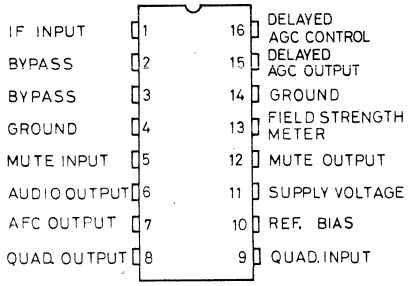
**ORDERING NUMBER:** TCA 3189

## MECHANICAL DATA

Dimensions in mm

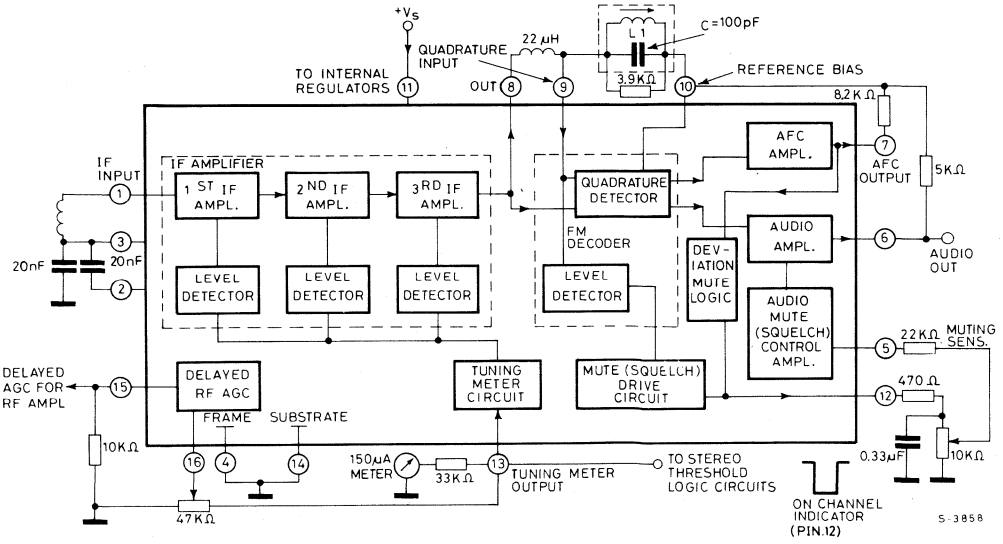


## CONNECTION DIAGRAM
(top view)




S-3286

## BLOCK DIAGRAM



## THERMAL DATA

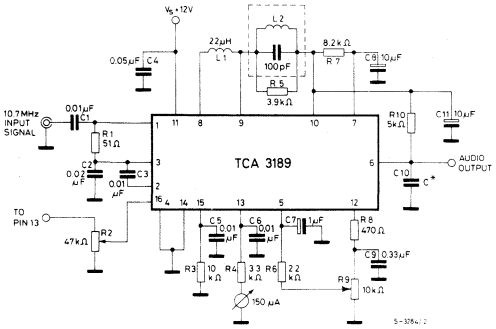
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max. | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s$ = 12V, $T_{amb}$ = 25°C)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage range | No signal input, non muted | | 9 | | 16 | V |
| $I_s$ | Supply current | | | 20 | 31 | 44 | mA |
| $V_1$ | Voltage at the IF amplifier input | | | 1.2 | 1.9 | 2.4 | V |
| $V_2$, $V_3$ | Voltage at the input bypass | | | 1.2. | 1.9 | 2.4 | V |
| $V_{15}$ | Voltage at the pin 15 (RF AGC) | | | 7.5 | 9.5 | 11 | V |
| $V_{10}$ | Reference bias voltage | | | 5 | 5.6 | 6 | V |
| $V_i$ | Input limiting voltage (-3 dB) at pin 1 | $f_o$ = 10.7 MHz<br>$f_m$= 1 KHz<br>$\Delta f$= ± 75 KHz | | | 12 | 25 | μV |
| $V_o$ | Recovered audio voltage (pin 6) | $V_i \geqslant$ 50 μV<br>$f_o$ = 10.7 MHz<br>$f_m$= 1 KHz<br>$\Delta f$= ± 75 KHz | | 325 | 500 | 650 | mV |
| d | Distortion (single tuned) | $V_i \geqslant$ 1 mV<br>$f_o$ = 10.7 MHz<br>$f_m$= 1 KHz<br>$\Delta f$ = ± 75 KHz | | | 0.5 | 1 | % |
| d | Distortion (double tuned) | | | | 0.1 | | % |
| $\frac{S+N}{N}$ | Signal to noise ratio | | | 65 | 72 | | dB |
| AMR | Amplitude modulation rejection | $V_i$ = 100 mV<br>$f_o$ = 10.7 MHz<br>$f_m$ = 1 KHz<br>$\Delta f$ = ± 75 KHz<br>AM mod. 30% | | 45 | 55 | | dB |
| $V_{16}$ | RF AGC threshold | | | | 1.25 | | V |
| $\frac{\Delta I_7}{\Delta f}$ | AFC control slope | | | | 1.9 | | $\frac{\mu A}{KHz}$ |
| $V_{12}$ | On channel step (deviation mute) | $V_i$ = 100 mV | $f_{DEV.} <$ ± 40 KHz | | 0 | | V |
| | | $f_o$ = 10.7 MHz | $f_{DEV.} >$ ± 40 KHz | | 5.6 | | V |

## TEST CIRCUITS

Single tuned detector coil




Double tuned detector coil

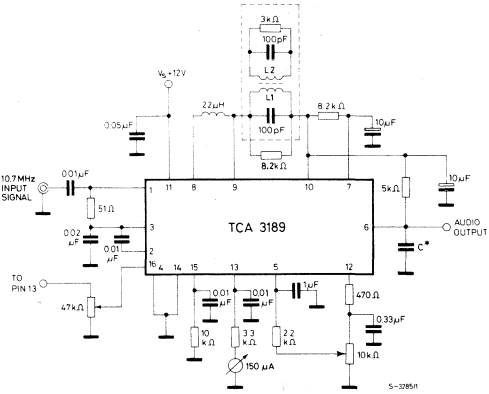



Fig. 1 - P.C. board and component layout of the single tuned circuit (1:1 scale)

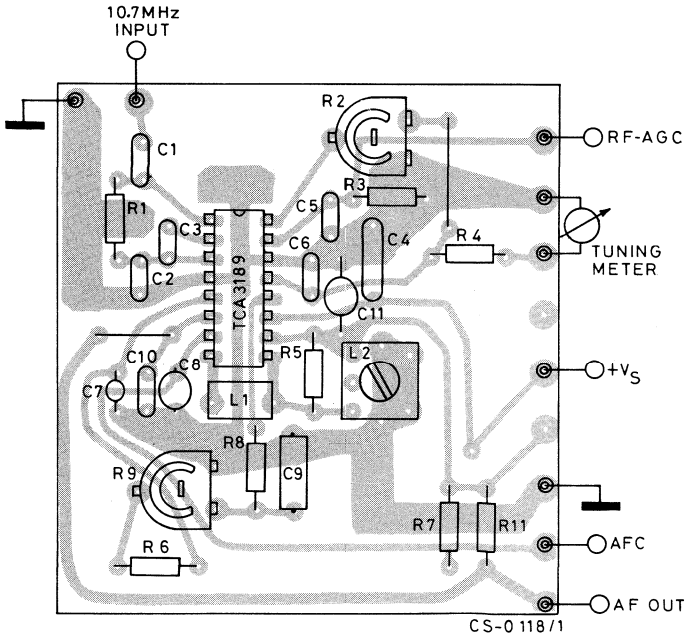


Fig. 2 - Limiting and noise characteristics

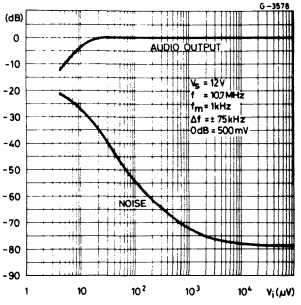



Fig. 3 - Deviation mute threshold vs. $R_{7-10}$

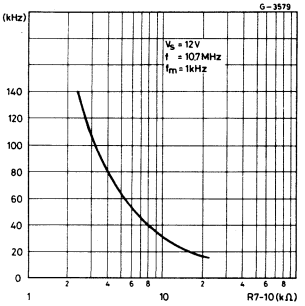



Fig. 4 - Recovered audio and muting action vs. input level

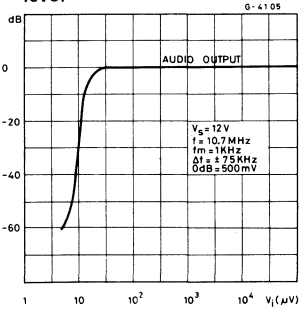



Fig. 5 - AFC characteristics

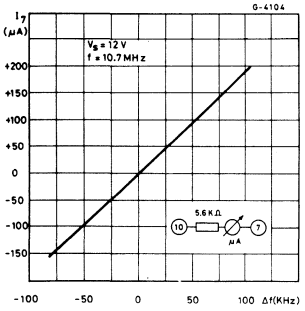



Fig. 6 - AGC voltage for FM tuner vs. input level

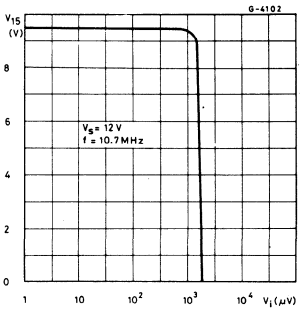
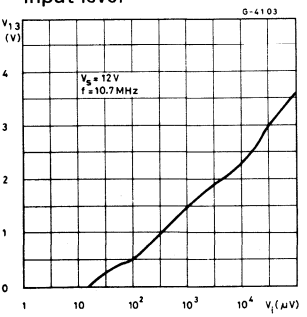



Fig. 7 - Field strength and tuning meter output vs. input level




| FEATURES | TCA 3189 | TCA 3089 |
|---|---|---|
| Low Limiting Sensitivity (25 μV max.) | Yes | Yes |
| Low Distortion (< 1%) | Yes | Yes |
| Single-coil Tuning Capability | Yes | Yes |
| Programmable Audio Level | Yes | No |
| S/N Mute | Yes | Yes |
| Deviation Mute | Yes | No |
| AFC and delayed AGC | Yes | Yes |
| Programmable AGC Threshold and Voltage | Yes | No |
| Typical S + N/N > 70 dB | Yes | No |
| Typical S + N/N > 60 dB | Yes | Yes |
| Meter Drive Voltage Depressed at Very-Low Signal Levels | Yes | No |
| On-Channel Step Control Voltage | Yes | No |

# TDA440S

## TV VISION IF SYSTEM

The TDA 440S is a monolithic integrated circuit in a 16-lead dual in-line plastic package. The functions incorporated are:

- Gain controlled vision IF amplifier
- Synchronous detector
- AGC detector with gating facility
- AGC amplifier for PNP tuner drive with variable delay
- Video preamplifier with positive and negative outputs.

It is intended for use in black and white and colour TV receivers.

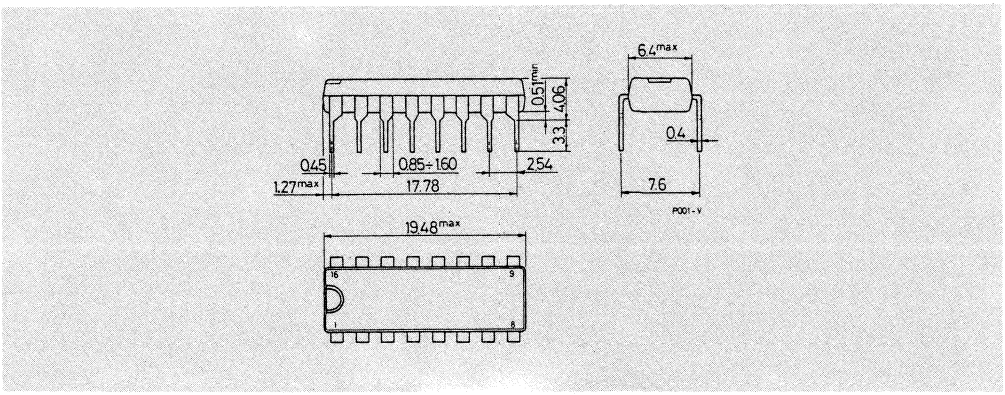
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 13) | 15 | V |
| $V_5$ | Voltage at pin 5 | 15 | V |
| $V_{10}$ | Voltage at pin 10 | -1 to 3 | V |
| $V_{11}$ | Voltage at pin 11 (with load connected to $V_s$) | 8 | V |
| $I_{11}$, $I_{12}$ | Output current | 5 | mA |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 70°C$ | 800 | mW |
| $T_{stg}$ | Storage temperature | -55 to 150 | °C |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

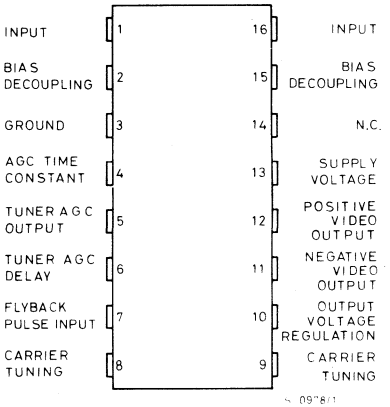
**ORDERING NUMBER:** TDA 440S

## MECHANICAL DATA

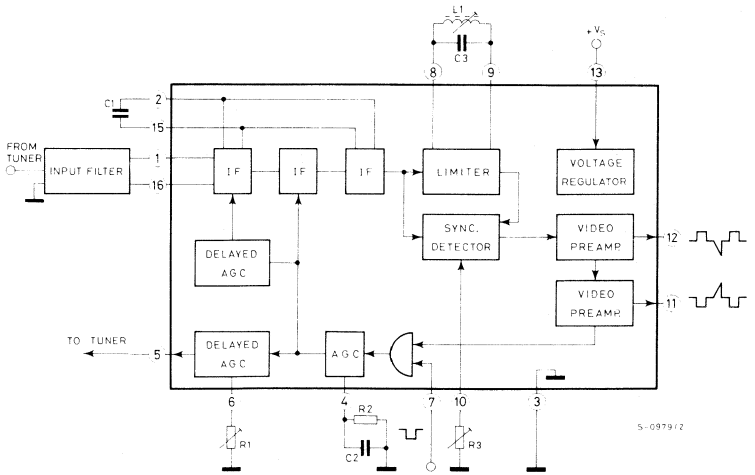
Dimensions in mm



## CONNECTION DIAGRAM (top view)




## BLOCK DIAGRAM



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to fig. 1 test circuit, $T_{amb}$ = 25°C)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | | |
| $V_s$ | Supply voltage range (pin 13) | | | 10 | 12 | 15 | V | |
| $I_s$ | Supply current (pin 13) | $V_s$ = 12V | | | 50 | | mA | 1a |
| $-I_{11}$ (1) | Output current | $V_s$ = 15V | $V_{11}$ = 8V | | 1.6 | | mA | 1b |
| $V_{11}$ (2) | Output voltage | $V_s$ = 12V | $R_5 = \infty$ | | | 4.5 | V | |
| | | | $R_5$ = 0 | 7 | | | | 1a |
| $V_{12}$ (2) | Output voltage | $V_s$ = 12V | $V_{11}$ = 5.5V | | 5.6 | | V | 1a |
| $\frac{\Delta V_{11}}{\Delta V_s}$ | Output voltage drift | $V_s$ = 11 to 14V | | | 3.5 | | % | 1b |
| **AC CHARACTERISTICS** (Refer to fig. 2 test circuit, $V_s$ = 12V, $T_{amb}$ = 25°C) | | | | | | | | |
| $I_5$ (3) | Tuner AGC current | $V_7$ = 0<br>$f_0$ = 38.9 MHz | $R_4$ = 2.5 KΩ | 6 | 9.5 | | mA | 3c |
| $V_7$ | AGC gating pulse input peak voltage | f = 15.6 kHz | | -1.5 | | -5 | V | – |
| $V_i$ (4) | Input sensitivity | $V_7$ = 0<br>$V_{11}$ = 3.3V peak to peak | $f_0$ = 38.9 MHz | 100 | 150 | 220 | μV | 3c |
| $\Delta V_i$ | AGC range | $V_7$ = 0<br>$f_0$ = 38.9 MHz<br>$V_{11}$ = 3.3V peak to peak | $\Delta V_o$ = 1 dB | 50 | 60 | | dB | |
| $V_o$ | Peak to peak output voltage at pin 11 | $V_7$ = 0<br>$f_0$ = 38.9 MHz<br>$V_i$ = see note (5) | $V_{11}$ = 5.5V | 3.3 | 3.5 | 3.7 | V | |

## ELECTRICAL CHARACTERISTICS (continued)

| | Parameter | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| $\Delta V_o$ | Video output variation over the AGC range (0 to 5.5 MHz) | $V_7$ = 0 $\Delta V_i$ = 50 dB<br>$V_{11}$ = 3.3V peak to peak<br>$f_0$ = 38.9 MHz<br>$f_m$ = 0 to 5.5 MHz | | 1 | 2 | dB | 3b |
| $V_{11}$, $V_{12}$ | Sound IF at video outputs (5.5 MHz) | $V_7$ = 0 $V_i$ = see note (5)<br>$f_0$ (vision) = 38.9 MHz<br>$f_0$ (sound) = 33.4 MHz | 30 | | | mV | 3d |
| | Differential error of the output voltage (B & W) | $V_7$ = 0 $f_0$ = 38.9 MHz<br>$V_{11}$ = 3.3V peak to peak | | | 15 | % | – |
| $V_{11}$, $V_{12}$ | Video carrier and video carrier 2nd harmonic leakage at video outputs | $V_7$ = 0<br>$V_i$ = see note (5)<br>$f_0$ = 38.9 MHz | | 15 | | mV | 3c |
| $V_{11}$, $V_{12}$ | Video carrier leakage at video outputs | | | 5 | | mV | |
| B | Frequency response (-3 dB) | | 8 | 10 | | MHz | 3d |
| $d_{im}$ | Intermodulation products at video outputs | $V_7$ = 0 $V_i$ = see note (5)<br>$f_0$ (vision) = 38.9 MHz<br>$f_0$ (sound) = 33.4 MHz<br>$f_0$ (chroma) = 34.5 MHz | | -50 | -40 | dB | 3a |
| $R_i$ | Input resistance (between pins 1 and 16) | $V_7$ = 0<br>$V_i$ = see note (5)<br>$f_0$ = 38.9 MHz | | 1.4 | | kΩ | – |
| $C_i$ | Input capacitance (between pins 1 and 16) | | | 2 | | pF | – |

**NOTES:**
(1) Current flowing out from pin 11 with the load connected to V = 8V.
(2) $V_{11}$ and $V_{12}$ are adjustable simultaneously by means of the resistance, or by a variable voltage $\leqslant$ 0.6V, connected between pin 10 and ground.
(3) Measured with an input voltage 10 dB higher than the $V_i$ at which the tuner AGC current starts.
(4) RMS values of the unmodulated video carrier (modulation down).
(5) The input voltage $V_i$ can have any value within the AGC range.

Fig. 1a - Test circuit for measurement of $I_S$, $V_{11}$, $V_{12}$

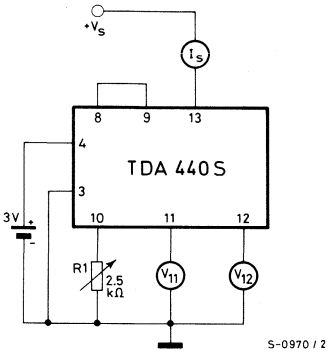



Fig. 1b - Test circuit for measurement of $-I_{11}$ and $\Delta V_{11}/\Delta V_s$

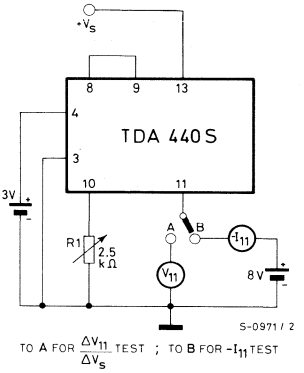
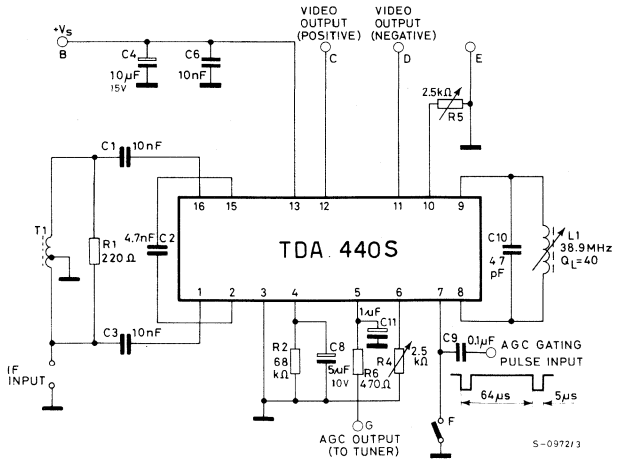



Fig. 2 - AC test circuit




**Note:** $T_1$ = 50/200Ω Balun transformer.
$V_i$ = Input voltage between pins 1 and 16.

Fig. 3a - Set-up for measurement of $d_{im}$

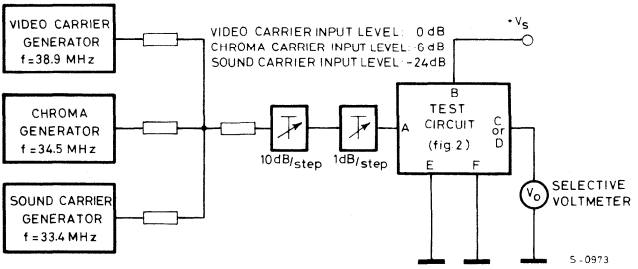



Fig. 3b - Set-up for measurement of $\Delta V_o$

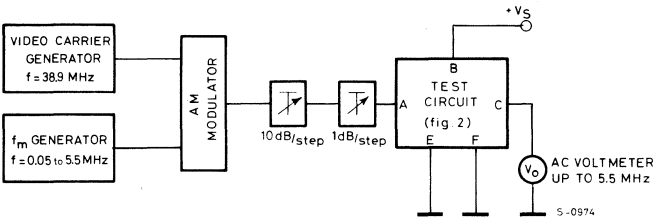



Fig. 3c - Set-up for measurement of $I_5$, $V_i$, $\Delta V_i$, $V_o$, $V_{11}$ and $V_{12}$

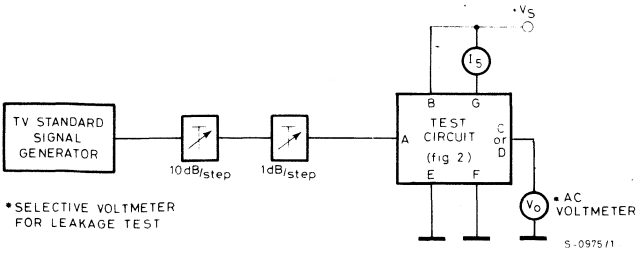


Fig. 3d - Set-up for measurement of B, $V_{11}$ and $V_{12}$

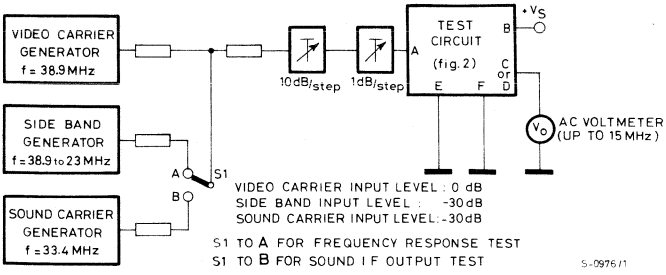



Fig. 4 - AGC voltage vs. input voltage variation

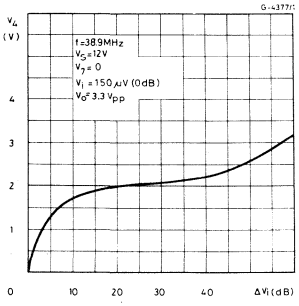



Fig. 5 - Tuner AGC output current vs. IF gain variation

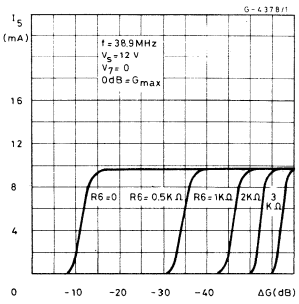
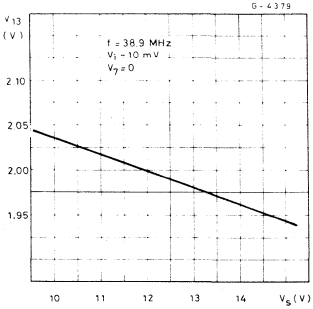



Fig. 6 - Output black level vs. supply voltage




## APPLICATION INFORMATION

The TDA 440S enables very compact IF amplifiers to be designed and provides the performance demanded by high quality receivers.

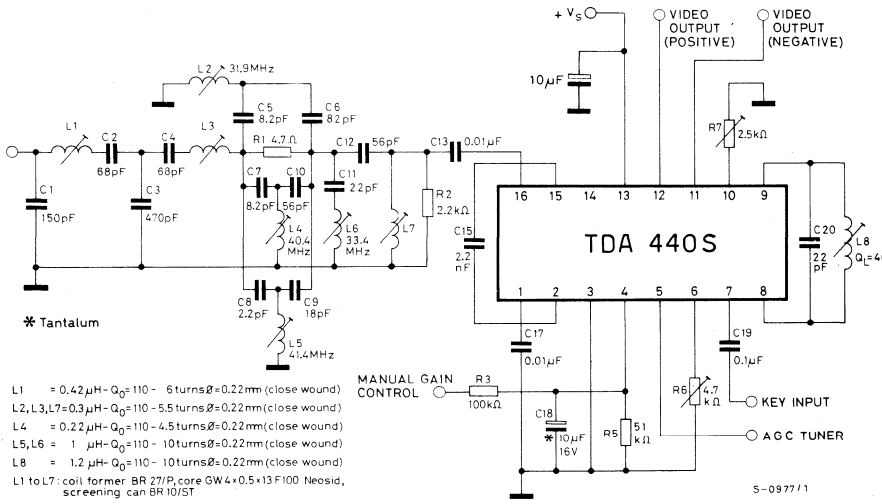
The input tuning-trapping circuitry and the detector network can be aligned independently with respect to each other.

The value of Q for the parallel tuned circuit between pin 8 and 9 is not critical, although the higher it is, the better is the chroma-sound beat rejection, but the tuning is more critical. Values of Q from 30 to 50 give good rejection with non-critical tuning.

The LC circuit between pins 8 and 9 is tuned to the vision carrier thus appreciably attenuating the sidebands. Hence a small amount of signal can be removed whose amplitude is almost constant over the whole working range of the AGC and it can be used to drive an AFC circuit.

The black level at the output is very stable against variations of $V_s$ and of temperature: this enables the contrast control to be kept simple. The AGC is of the gated type and can take the top of the synchronism or the black level (back porch) as its reference: when the latter is used, the output black level is particularly stable.

Fig. 8 - Typical application circuit.




**Typical performance of the Fig. 8 circuit**

| | | |
|---|---|---|
| Frequency response ($f_0$ vision = 38.9 MHz, $f_0$ sound = 33.4 MHz) standard CCIR | | |
| Sound carrier attenuation | 28 | dB |
| 31.9 MHz trap attenuation | ⩾ 60 | dB |
| 40.4 MHz trap attenuation | ⩾ 56 | dB |
| 41.4 MHz trap attenuation | ⩾ 44 | dB |
| AGC range | 55 | dB |
| Overall gain including IF filter and trap circuits (note 1) | 86 | dB |
| Intermodulation products over the whole AGC range (note 2) | - 55 | dB |

**NOTES:** (1) The gain is measured at video output 3.3V peak to peak and is defined as peak to peak output voltage to RMS input voltage (modulation down).

(2) Measured at 1.07 MHz, vision carrier level = 0 dB, chroma carrier level = -6 dB, sound carrier level = -6 dB.

Fig. 9 - Overall frequency response of the fig. 8 circuit

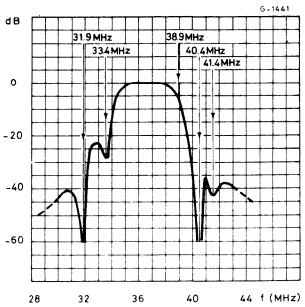
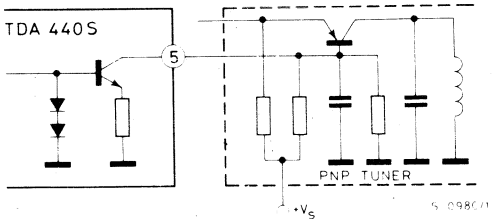
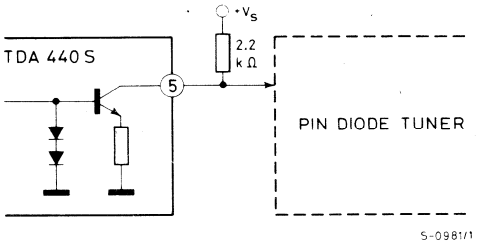
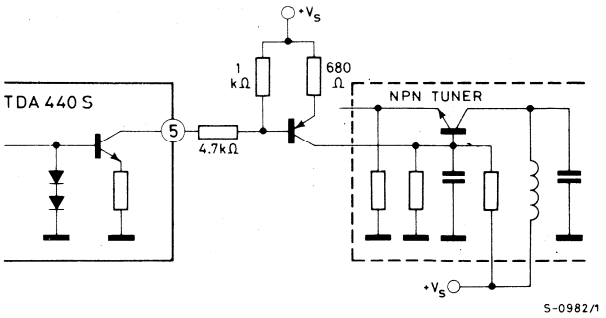


Fig. 10 - Circuit options for tuner AGC driving



## PREAMPLIFIER WITH ALC FOR CASSETTE RECORDERS

- EXCELLENT VERSATILITY in USE ($V_s$ from 4 to 20V)
- HIGH OPEN LOOP GAIN
- LOW DISTORTION
- LOW NOISE
- LARGE AUTOMATIC LEVEL CONTROL RANGE
- GOOD SUPPLY RIPPLE REJECTION
- STEREO MATCHING BETTER THAN 3 dB

The TDA 1054M is a monolithic integrated circuit in a 16-lead dual in-line plastic package. The functions incorporated are:
– Low noise preamplifier
– Automatic level control system (ALC)
– High gain equalization amplifier
– Supply voltage rejection facility (SVRF).
It is intended as preamplifier in cassette tape recorders and players, dictaphones, compressor and expander in industrial equipments, Hi-Fi preamplifiers and in wire diffusion receivers; for stereo applications the ALC matching is better than 3 dB.

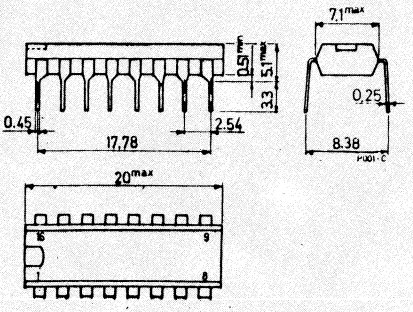
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 20 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 50°C$ | 500 | mW |
| $T_{stg}, T_j$ | Storage and junction temperature | -40 to 150 | °C |

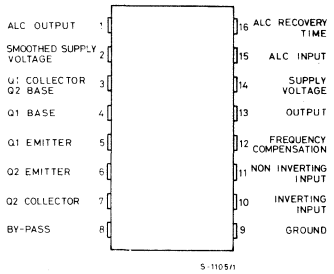
**ORDERING NUMBERS:** TDA 1054M mono applications
2 TDA 1054M stereo applications

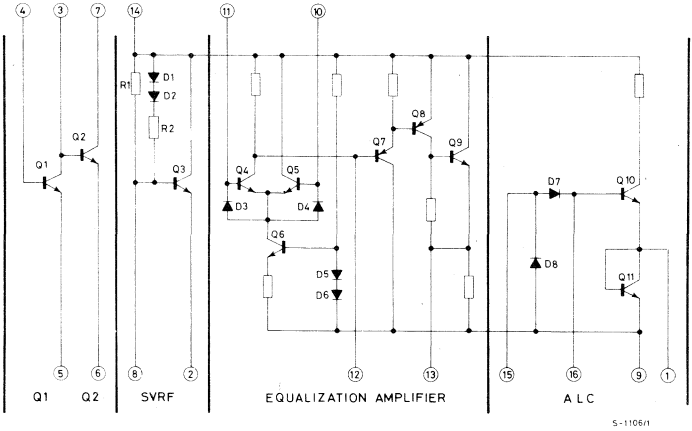
## MECHANICAL DATA

Dimensions in mm

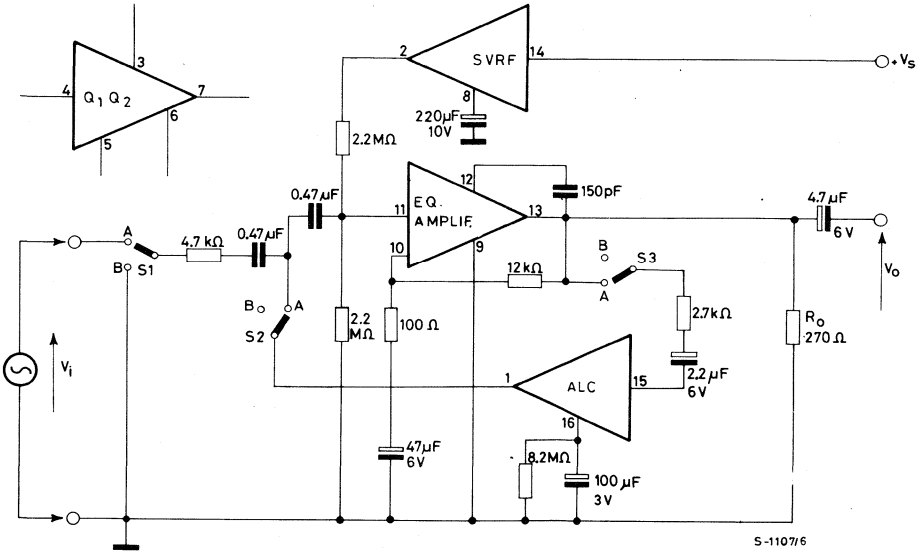


## CONNECTION AND SCHEMATIC DIAGRAMS
(top view)




## TEST CIRCUIT



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 200 | °C/W |

## ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, $T_{amb}$ = 25°C)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 4 | | 20 | V |
| $I_d$ | Quiescent drain current | $V_s$ = 9V $R_L = \infty$<br>S1 = S2 = S3 = B | | 6 | | mA |
| $h_{FE}$ | DC current gain | $I_C$ = 0.1 mA $V_{CE}$ = 5V | 300 | 500 | | – |
| $e_N$ | Input noise voltage (Q1) | $I_C$ = 0.1 mA $V_{CE}$ = 5V<br>f = 1 kHz | | 2 | | $\frac{nV}{\sqrt{Hz}}$ |
| $i_N$ | Input noise current (Q1) | | | 0.5 | | $\frac{pA}{\sqrt{Hz}}$ |
| NF | Noise figure (Q1) | $I_C$ = 0.1 mA $V_{CE}$ = 5 V<br>$R_g$ = 4.7 kΩ<br>B (-3 dB) = 20 to 10,000 Hz | | 0.5 | 4 | dB |
| $G_V$ | Open loop voltage gain (for equalization amplifier) | $V_s$ = 9V f = 1 kHz | | 60 | | dB |
| $V_o$ | Output voltage with A.L.C. | $V_s$ = 9V $V_i$ = 100mV<br>f = 1 kHz S1 = S2 = S3 = A | | 1.1 | | V |
| R1 | (for SVRF system) | see schematic diagram | | 7.5 | | kΩ |
| R2 | (for SVRF system) | | | 120 | | Ω |
| $e_N$ | Input noise voltage (for equalization amplifier pin 11) | $V_s$ = 9V $R_g$ = 4.7 kΩ<br>$G_V$ = 40 dB S1 = B<br>B (-3 dB)= 22 Hz to 22 KHz | | 1.3 | | μV |
| $V_{DR}$ | Drop-out (between pins 14 and 2) | $V_s$ = 9V $I_d$ = 6 mA | | 0.8 | | V |

Fig. 1 - Equivalent input spot voltage and noise current vs. bias current (input transistor $Q_1$)

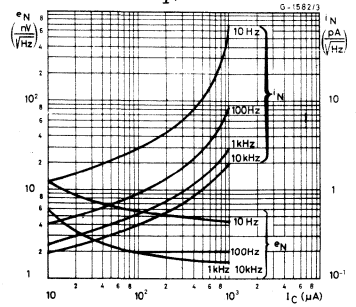



Fig. 2 - Equivalent input noise current vs. frequency (input transistor $Q_1$)

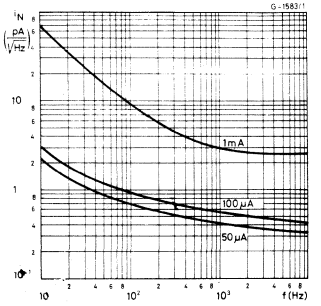



Fig. 3 - Equivalent input noise voltage vs. frequency (input transistor $Q_1$)

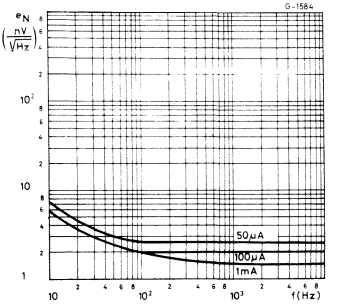



Fig. 4 - Noise figure vs. bias current (input transistor $Q_1$)

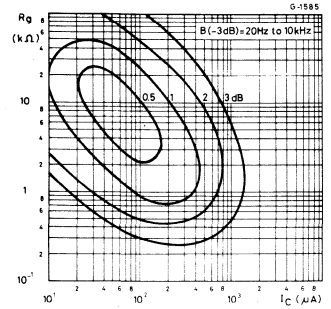



Fig. 5 - Optimum source resistance and minimum NF vs. bias current (input transistor $Q_1$)

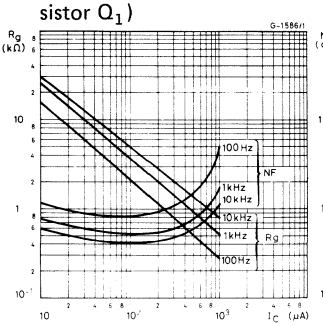



Fig. 6 - Current gain vs. collector current (input transistor $Q_1$)

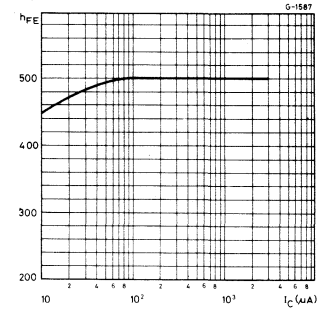



Fig. 7 - Open loop gain vs. frequency (equalization amplifier)

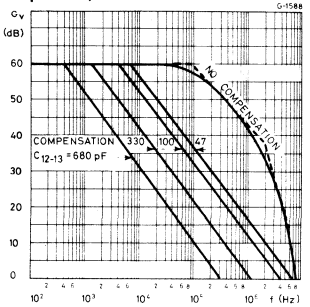
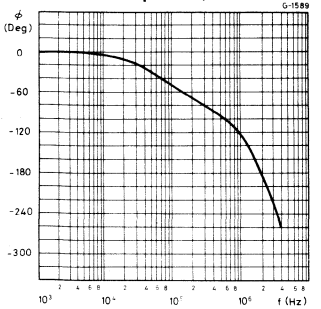



Fig. 8 - Open loop phase response vs. frequency (equalization amplifier)



## APPLICATION INFORMATION

Fig. 9 - Application circuit for battery/mains cassette player and recorder

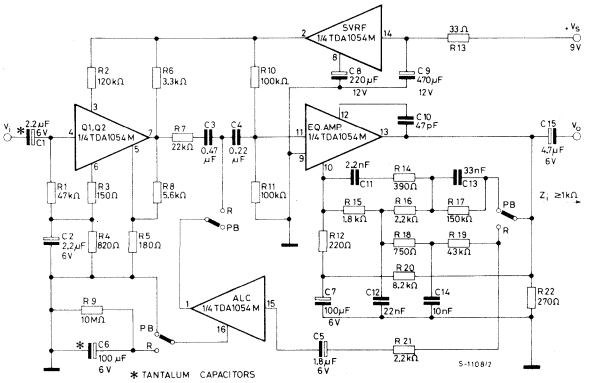
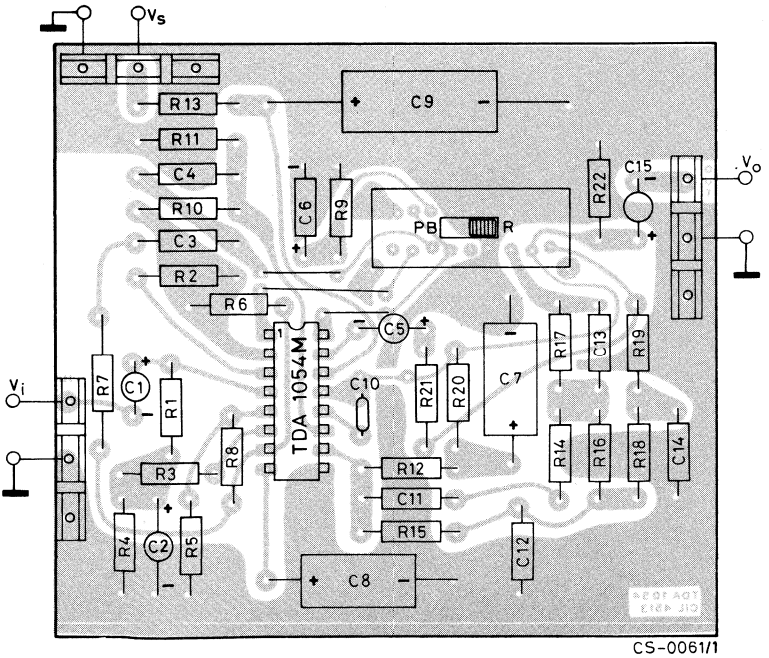



Fig. 10 - P.C. board and component layout for the circuit fig. 9 (1:1 scale)



## Typical performance of circuit in fig. 9

($T_{amb}$ = 25°C, $V_s$ = 9V)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **PLAYBACK** | | | | | | |
| $G_v$ | Voltage gain (open loop) | f = 20 to 20,000 Hz | | 110 | | dB |
| $G_v$ | Voltage gain (closed loop) | f = 1 kHz | | 57 | | dB |
| $\|Z_i\|$ | Input impedance | f = 100 Hz<br>f = 1 kHz<br>f = 10 kHz | | 10<br>41<br>43 | | kΩ<br>kΩ<br>kΩ |
| $\|Z_o\|$ | Output impedance | f = 1 kHz | | 12 | 35 | Ω |
| B | Frequency response | | | see fig. 12 | | |
| d | Distortion | $V_o$ = 1V f = 1 kHz | | 0.1 | | % |
| | Output background noise | $Z_g$ = 300 Ω + 120 mH (DIN 45405) | | 1.3 | | mV |
| *** | Output weighted background noise | | | 1.3 | | mV |
| $\frac{S+N}{N}$ | Signal to noise ratio | $V_o$ = 1.3V<br>$Z_g$ = 300 Ω + 120 mH | | 60 | | dB |
| SVR | Supply voltage ripple rejection at the output | $f_{ripple}$ = 100 Hz | | 30 | | dB |
| $t_{on}$** | Switch-on time | $V_o$ = 1V | | 500 | | ms |
| **RECORDING** | | | | | | |
| $G_v$ | Voltage gain (open loop) | f = 20 to 20,000 Hz | | 110 | | dB |
| $G_v$ | Voltage gain (closed loop) | f = 1 kHz | | 70 | | dB |
| B | Frequency response | | | see fig. 14 | | |
| d* | Distortion without ALC | $V_o$ = 1.1V f = 1 kHz | | 0.3 | | % |
| d | Distortion with ALC | $V_o$ = 1.1V f = 10 kHz | | 0.4 | | % |
| ALC | Automatic level control range (for 3 dB of output voltage variation) | $V_i \leqslant$ 40 mV f = 10 kHz | | 54 | | dB |
| $V_o$ | Output voltage before clipping without ALC | f = 1 kHz | | 2.3 | | V |
| $V_o$ | Output voltage with ALC | $V_i$ = 30 mV f = 10 kHz | | 1.1 | | V |

## Typical performance of circuit in fig. 9 (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_l$ ** | Limiting time (see fig. 11) | $\Delta V_i$ = +40 dB f = 1 kHz | | 75 | | ms |
| $t_{set}$ ** | Level setting time (see fig. 11) | | | 300 | | ms |
| $t_{rec}$ ** | Recovery time (see fig. 11) | $\Delta V_i$ = -40 dB f = 1 kHz | | 150 | | s |
| $t_{on}$ ** | Switch-on time | $V_o$ = 1.1V | | 500 | | ms |
| $\frac{S+N}{N}$ **** | Signal to noise ratio with ALC | $V_o$ = 1.1V $R_g$ = 470 Ω | | 64 | | dB |

* Measured with selective voltmeter
** This value depends on external network
*** When the DIN 45511 norm for frequency response is not mandatory the equalization peak at 10 kHz can be avoided – so halving the output noise
**** Weighted noise measurement (DIN 45405)

Fig. 11 - Limiting, level setting, recovery time

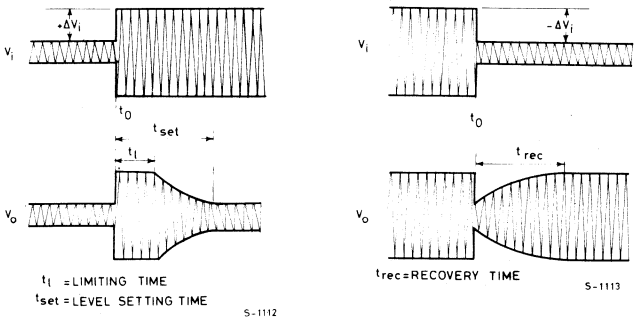



Fig. 12 - Relative frequency response for the circuit in fig. 9 (playback)

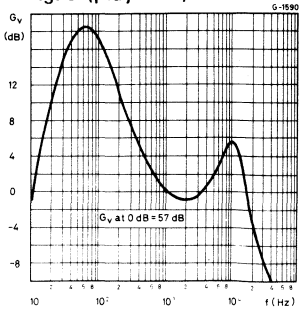



Fig. 13 - Distortion vs. frequency for the circuit in fig. 9 (playback)

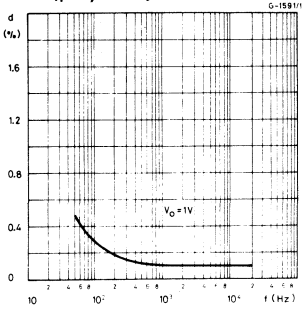



Fig. 14 - Relative frequency response for the circuit in fig. 9 (recording)

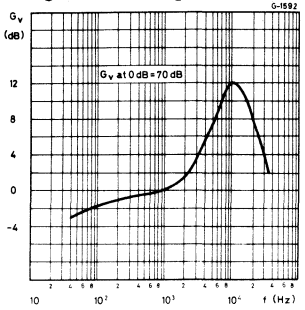


Fig. 15 - Output voltage variation and distortion with ALC vs. input voltage for the circuit in fig. 9 (recording)

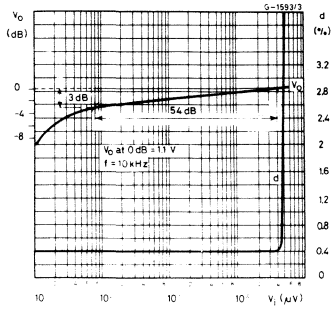



Fig. 16 - Distortion vs. frequency with ALC for the circuit in fig. 9 (recording)

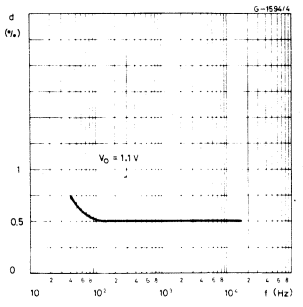



Fig. 17 - Limiting and level setting time vs. input signal variation

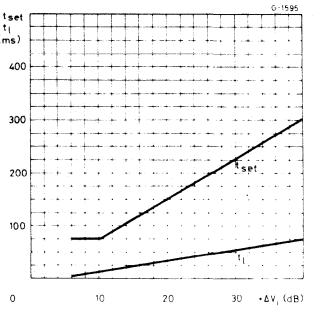



Fig. 18 - Low cost application circuit

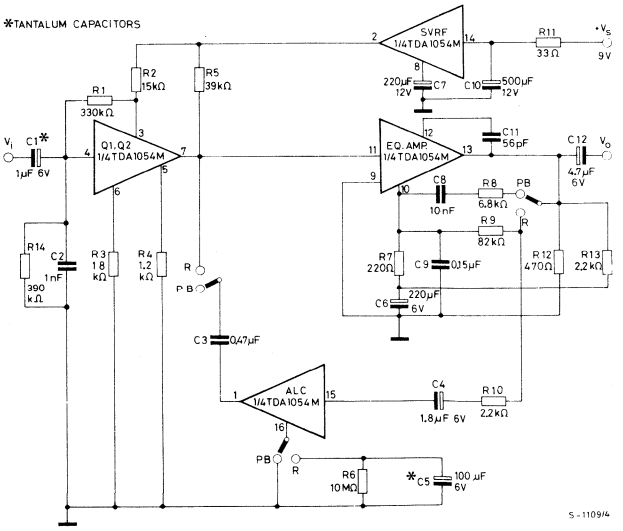
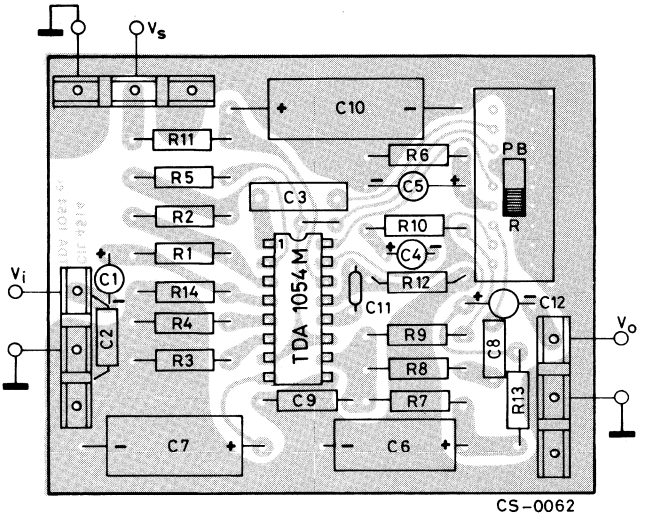


Fig. 19 - P.C. board and component layout for the circuit in fig. 18 (1:1 scale)




## Typical performance of circuit in fig. 18

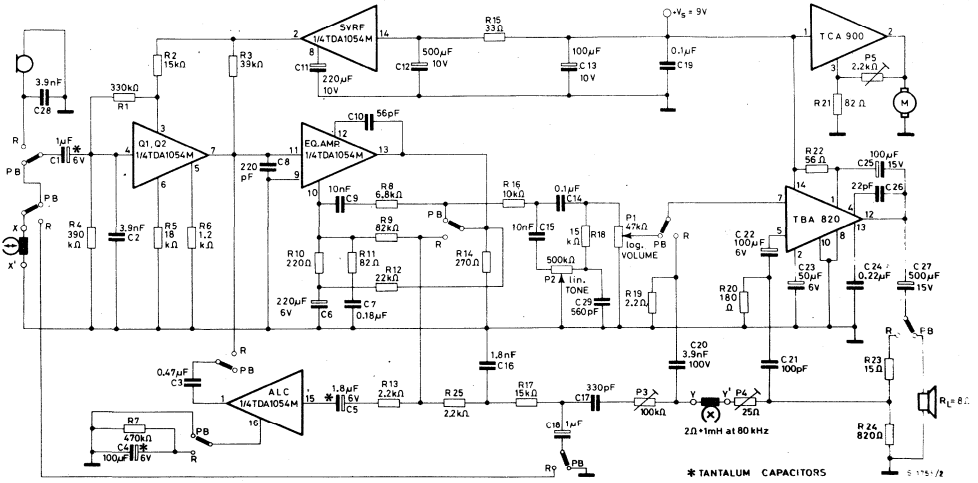
($T_{amb}$ = 25°C, $V_s$ = 9V)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **PLAYBACK** | | | | | | |
| $V_s$ | Supply voltage | | 5 | | 12 | V |
| $I_d$ | Quiescent drain current | | | 18 | | mA |
| $G_v$ | Voltage gain (closed loop) | f = 1 kHz | | 54 | | dB |
| B | Frequency response | f = 100 Hz<br>f = 1 kHz<br>f = 6 kHz<br>f = 10 kHz<br>f = 60 kHz | | 12<br>0<br>5<br>11<br>10 | | dB<br>dB<br>dB<br>dB<br>dB |
| d | Distortion | $V_o$ = 1V f = 1 kHz | | 0.6 | | % |
| $e_N$ | Output weighted background noise | $Z_g$ = 300 Ω + 120 mH (DIN 45405) | | 1.3 | | mV |

## Typical performance of circuit in fig. 18 (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **RECORDING** | | | | | | |
| $G_V$ | Voltage gain (closed loop) | f = 1 kHz | | 70 | | dB |
| B | Frequency response | f = 140 Hz<br>f = 1 kHz<br>f = 10 kHz | | -3<br>0<br>4 | | dB<br>dB<br>dB |
| d | Distortion | $V_O$ = 1.1V f = 10 kHz | | 0.7 | | % |
| ALC | Range for 3 dB of output voltage variation | $V_i \leqslant 40$ mV f = 10 kHz | | 54 | | dB |

Fig. 20 - Complete cassette player and recorder



## MOTOR SPEED REGULATOR

- EXCELLENT VERSATILITY IN USE
- HIGH OUTPUT CURRENT (UP TO 800 mA)
- LOW QUIESCENT CURRENT (1.7 mA)
- LOW REFERENCE VOLTAGE (1.2V)
- EXCELLENT PARAMETERS STABILITY VERSUS TEMPERATURE

The TDA 1151 is a monolithic integrated circuit in Jedec TO-126 plastic package. It is intended for use as speed regulator for DC motors of record players, tape and cassette recorders, movie cameras, toys etc.

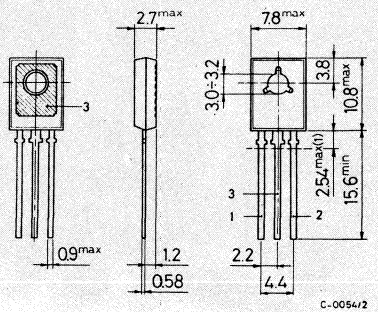
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 20 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb}$ = 70°C | 0.8 | W |
| | at $T_{case}$ = 100°C | 5 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA 1151

## MECHANICAL DATA

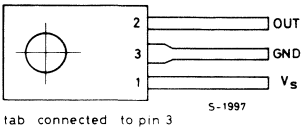
Dimensions in mm



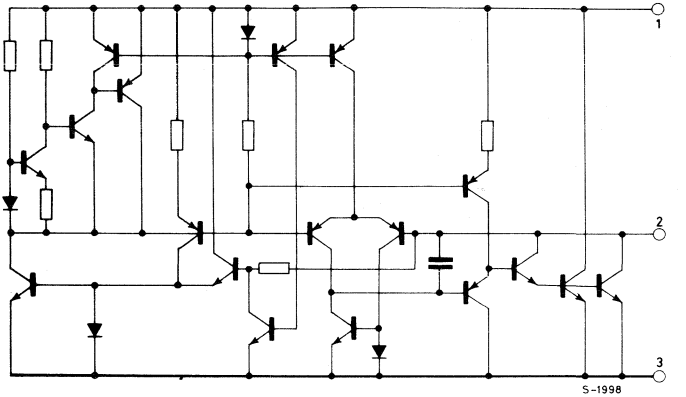

(1) Within this region the cross-section of the leads is uncontrolled

TO-126 (SOT 32)

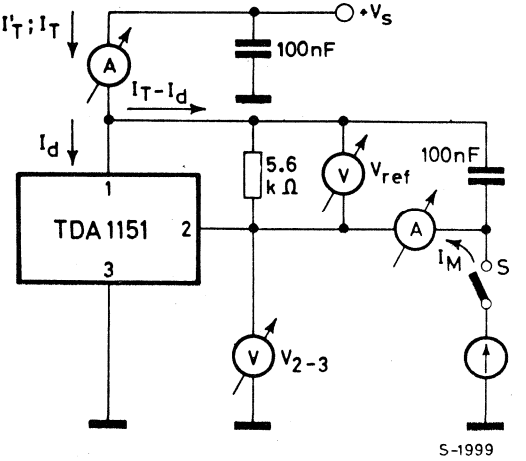
## CONNECTION AND SCHEMATIC DIAGRAMS




tab connected to pin 3




## TEST CIRCUIT



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 10 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb}$= 25°C)

| | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{ref}$ | Reference voltage (between pins 1 and 2) | $V_s$ = 6V $I_M$= 0.1A | 1.1 | 1.2 | 1.3 | V |
| $I_d$ | Quiescent drain current | $V_s$ = 6V $I_M$= 100 μA | | 1.7 | | mA |
| $I_{MS}$ | Starting current | $V_s$ = 5V $\Delta V_{ref}/V_{ref}$= -50% | 0.8 | | | A |
| $V_{1-3}$ | Minimum supply voltage | $I_M$= 0.1A $\Delta V_{ref}/V_{ref}$= -5% | | | 2.5 | V |
| $K=I_M/I_T$ | Reflection coefficient | $V_s$ = 6V $I_M$= 0.1A | 18 | 20 | 22 | — |
| $\frac{\Delta K}{K}/\Delta V_s$ | | $V_s$ = 6V to 18V $I_M$= 0.1A | | 0.45 | | %/V |
| $\frac{\Delta K}{K}/\Delta I_M$ | | $V_s$ = 6V $I_M$= 25 to 400 mA | | 0.005 | | %/mA |
| $\frac{\Delta K}{K}/\Delta T$ | | $V_s$ = 6V $I_M$= 0.1A $T_{amb}$= -20 to 70°C | | 0.02 | | %/°C |
| $\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_s$ | Line regulation | $V_s$ = 6V to 18V $I_M$= 0.1A | | 0.02 | | %/V |
| $\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_M$ | Load regulation | $V_s$ = 6V $I_M$= 25 to 400 mA | | 0.009 | | %/mA |
| $\frac{\Delta V_{ref}}{V_{ref}}/\Delta T$ | Temperature coefficient | $V_s$ = 6V $I_M$= 0.1A $T_{amb}$= -20 to 70°C | | 0.02 | | %/°C |

Fig. 1 - Quiescent drain current vs. power supply

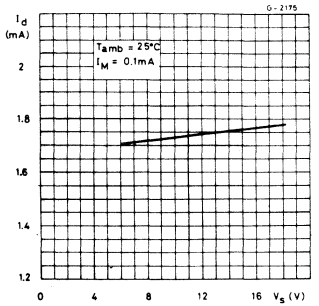



Fig. 2 - Quiescent drain current vs. ambient temperature

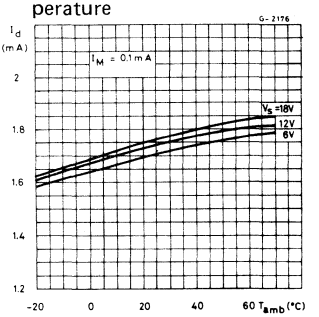



Fig. 3 - Reference voltage vs. supply voltage

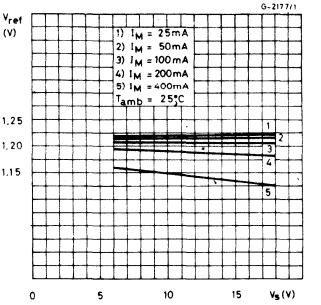



Fig. 4 - Reference voltage vs. motor current

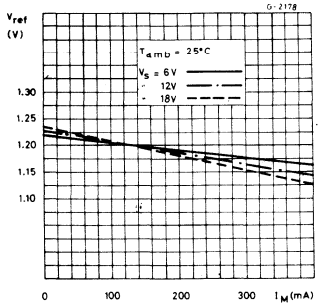



Fig. 5 - Reference voltage vs. ambient temperature

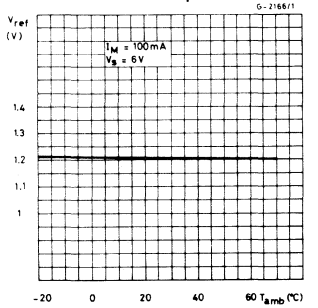



Fig. 6 - Reflection coefficient vs. supply voltage

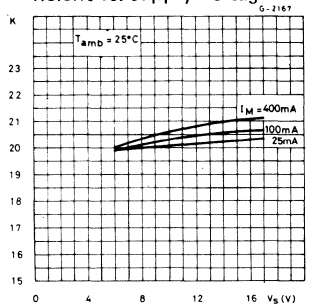



Fig. 7 - Reflection coefficient vs. motor current

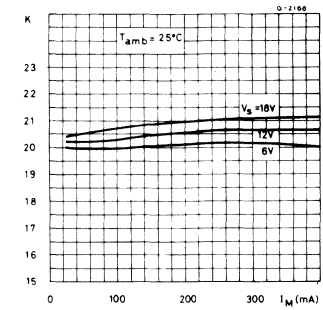



Fig. 8 - Reflection coefficient vs. ambient temperature

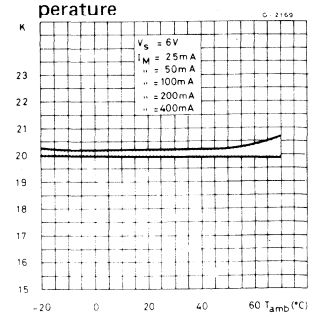
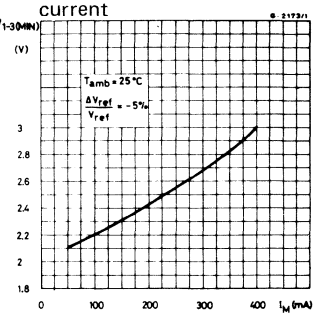
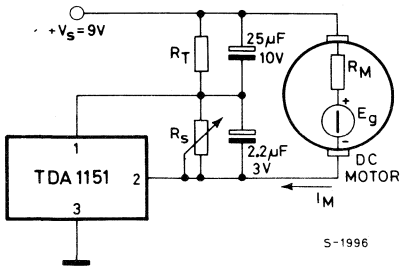



Fig. 9 - Typical minimum supply voltage vs. motor current



## APPLICATION INFORMATION

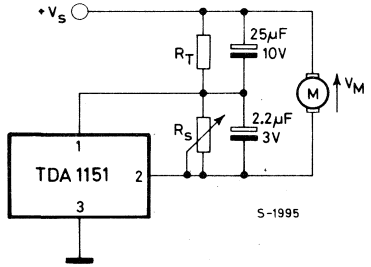



$I_M$ = Motor current at rated speed
$R_M$ = Motor resistance
$E_g$ = Back electromotive force

$$R_{S\ min} = \frac{V_{ref} \cdot R_T}{E_g - (V_{ref} - I_d \cdot R_T)}$$

$R_T = K \cdot R_M$
$R_T = K_{typ} \cdot R_{M\ typ}$
If $R_{T\ max} > KR_{M\ min}$ instability may occur

Application circuit




$V_s$ = +9V
$R_M$ = 14.2Ω
$R_T$ = 280Ω
$R_S$ = 1 kΩ
$E_g$ = 2.9V
$I_M$ = 150 mA
$V_M = R_M \cdot I_M + E_g = 5.03V$

Note: A ceramic capacitor of 10 nF between pins, 1 and 2 improves stability in some applications.

Fig. 10 - Speed variation vs. supply voltage

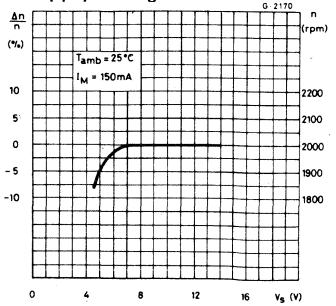



Fig. 11 - Speed variation vs. motor current

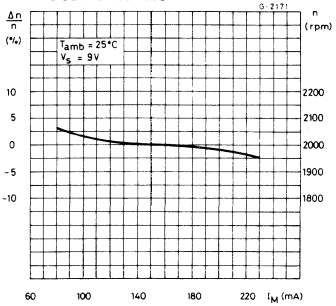
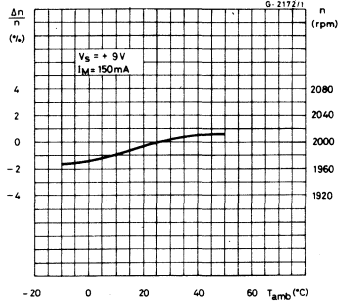
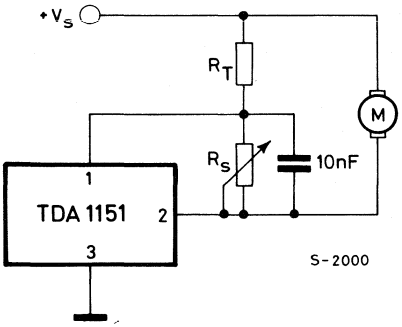



Fig. 12 - Speed variation vs. ambient temperature



## APPLICATION INFORMATION (continued)

Low cost application circuit




$V_S$ = +12V
$R_M$ = 14.7Ω
$R_T$ = 290Ω
$R_S$ = 1 kΩ
$E_g$ = 2.65V
$I_M$ = 110 mA

Fig. 13 - Speed variation vs. supply voltage

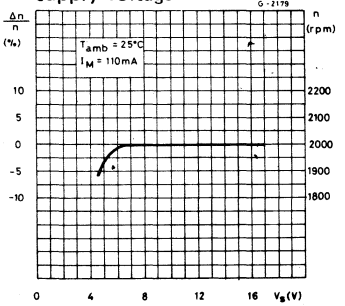



Fig. 14 - Speed variation vs. motor current

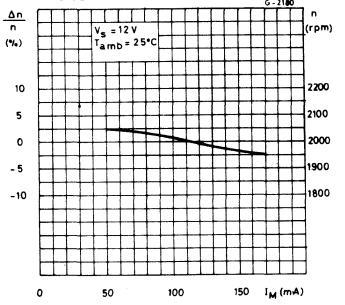
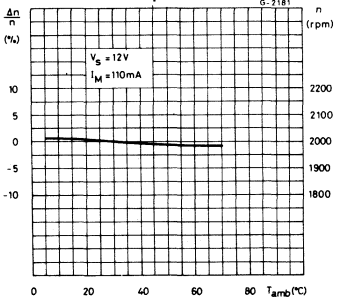



Fig. 15 - Speed variation vs. ambient temperature



# TDA1170D

# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS

The TDA 1170D is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It is intended for use in black and white and colour TV receivers. **Low-noise makes this device particularly suitable for use in monitors.** The functions incorporated are: synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.

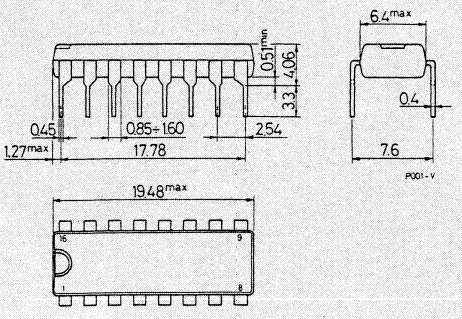
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage at pin 2 | 35 | V |
| V6, V7 | Flyback peak voltage | 60 | V |
| V14 | Power amplifier input voltage | + 10 | V |
| | | - 0.5 | V |
| $I_o$ | Output peak current (non repetitive) at t = 2 msec | 2 | A |
| $I_o$ | Output peak current at f = 50 Hz t $\leqslant$ 10 $\mu$sec | 2.5 | A |
| $I_o$ | Output prak current at f = 50 Hz t > 10 $\mu$sec | 1.5 | A |
| $I_3$ | Pin 3 DC current at V6 < V2 | 100 | mA |
| $I_3$ | Pin 3 peak to peak flyback current for f = 50 Hz, $t_{fly} \leqslant$ 1.5 msec | 1.8 | A |
| $I_{10}$ | Pin 10 current | ± 20 | mA |
| $P_{tot}$ | Power dissipation: at $T_{tab}$ = 90°C | 4.3 | W |
| | at $T_{amb}$ = 70°C (free air) | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

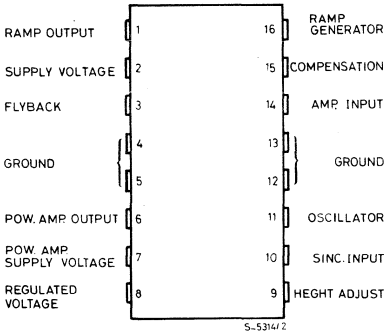
**ORDERING NUMBERS:** TDA 1170D

## MECHANICAL DATA

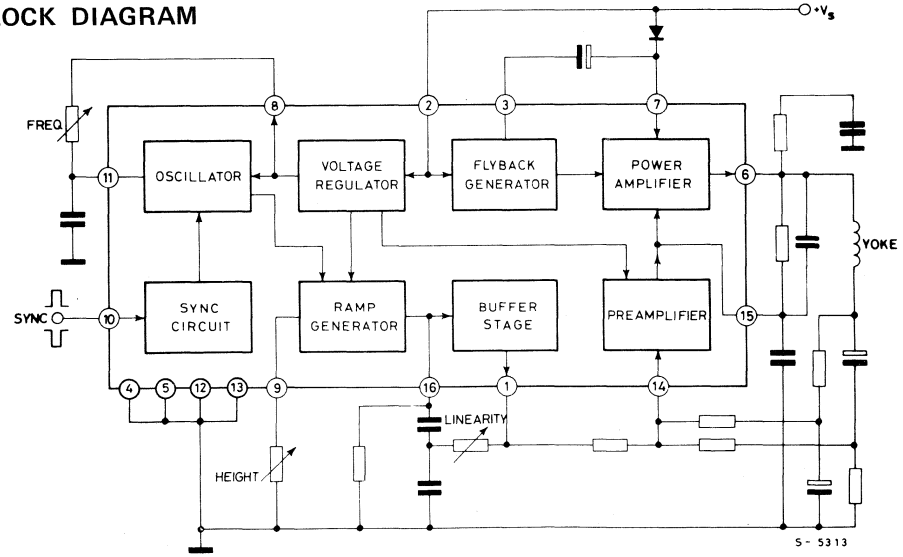
. Dimensions in mm



## CONNECTION DIAGRAM




## BLOCK DIAGRAM

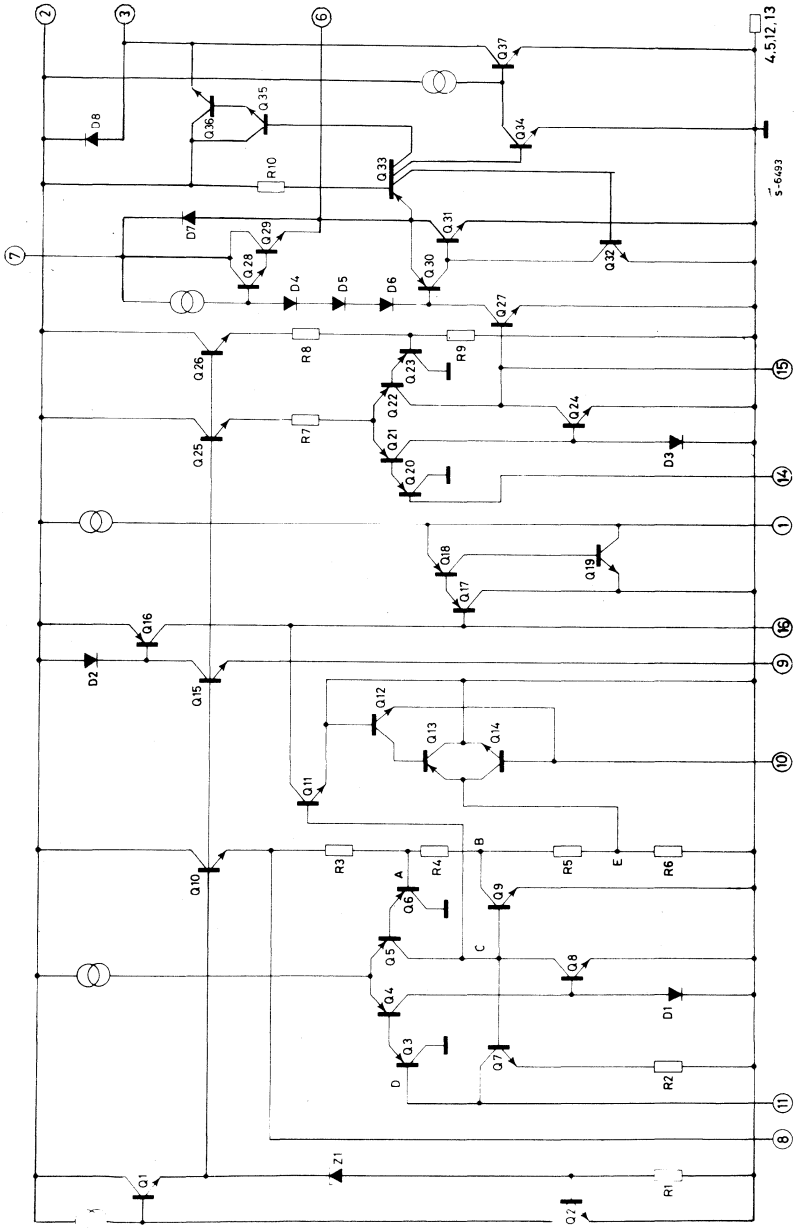



## THERMAL DATA

| | | | |
|---|---|---|---|
| $R_{th\ j\text{-}tab}$ | Thermal resistance junction-pins | max | 14 °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 80 °C/W (◦) |

(◦) Obtained with pins 4, 5, 12, 13 soldered to printed circuit with minimized copper area.

## SCHEMATIC DIAGRAM



## ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_s$ = 35V, $T_{amb}$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | |
| $I_2$ | Pin 2 quiescent current | $I_3$ = 0 | | 7 | 14 | mA | 1b |
| $I_7$ | Pin 7 quiescent current | $I_6$ = 0 | | 8 | 17 | mA | 1b |
| $-I_{11}$ | Oscillator bias current | V11= 1V | | 0.1 | 1 | μA | 1a |
| $-I_{14}$ | Amplifier input bias current | V14= 1V | | 1 | 10 | μA | 1b |
| $-I_{16}$ | Ramp generator bias current | V16= 0 | | 0.02 | 0.3 | μA | 1a |
| $-I_{16}$ | Ramp generator current | $I_7$ = 20 μA V16= 0 | 18.5 | 20 | 21.5 | μA | 1b |
| $\frac{\Delta I_{16}}{I_{16}}$ | Ramp generator non-linearity | ΔV16= 0 to 12V<br>$I_9$ = 20 μA | | 0.2 | 1 | % | 1b |
| $V_s$ | Supply voltage range | | 10 | | 35 | V | – |
| V1 | Pin 1 saturation voltage to ground | $I_1$ = 1 mA | | 1 | 1.4 | V | – |
| V3 | Pin 3 saturation voltage to ground | $I_3$ = 10 mA | | 300 | 450 | mV | 1a |
| V6 | Quiescent output voltage | $V_s$= 10V R1= 1 KΩ<br>R2 = 1 KΩ | 4.1 | 4.4 | 4.65 | V | 1a |
| | | $V_s$= 35V R1= 3 KΩ<br>R2 = 1 KΩ | 8.3 | 8.8 | 9.2 | V | 1a |
| V6L | Output saturation voltage to ground | $-I_6$= 0.1A | | 0.9 | 1.2 | V | 1c |
| | | $-I_6$= 0.8A | | 1.9 | 2.3 | V | 1c |
| V6H | Output saturation voltage to supply | $I_6$= 0.1A | | 1.4 | 2.1 | V | 1d |
| | | $I_6$= 0.8A | | 2.8 | 3.2 | V | 1d |
| V8 | Regulated voltage at pin 8 | | 6.1 | 6.5 | 6.9 | V | 1b |
| V9 | Regulated voltage at pin 9 | $I_9$= 20 μA | 6.2 | 6.6 | 7 | V | 1b |
| $\frac{\Delta V8}{\Delta V_s}$ ; $\frac{\Delta V9}{\Delta V_s}$ | Regulated voltage drift with supply voltage | $\Delta V_s$= 10 to 35V | | 1 | | mV/V | 1b |
| V14 | Amplifier input reference voltage | | 2.07 | 2 2 | 2.3 | V | – |
| R10 | Pin 10 input resistance | V10 ⩽ 0.4V | 1 | | | MΩ | 1a |

Fig. 1 - DC test circuit

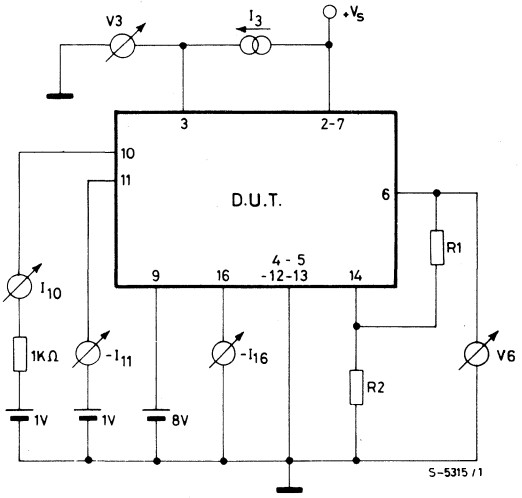



Fig. 1a

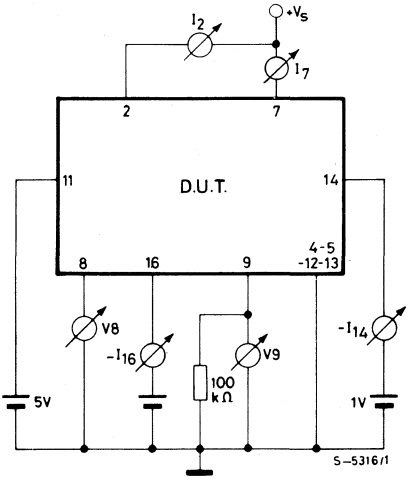



Fig. 1b

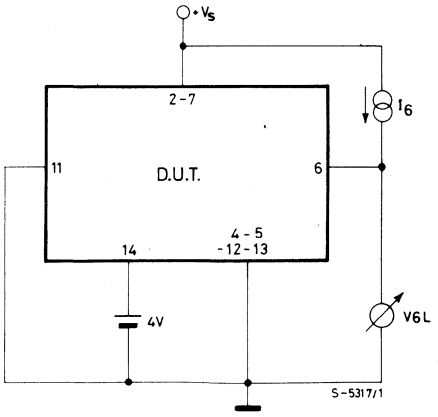



Fig. 1c

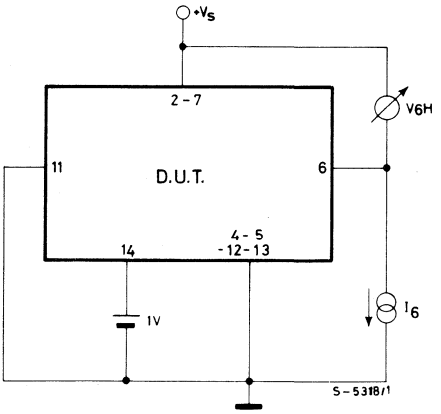



Fig. 1d

## ELECTRICAL CHARACTERISTICS (Refer to the AC test circuit, $V_s$ = 22V; f = 50 Hz; $T_{amb}$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | | |
| $I_s$ | Supply current | $I_y$ = 1 App | | 140 | | mA |
| $I_{10}$ | Sync. input current (positive or negative) | | 500 | | | μA |
| V6 | Flyback voltage | $I_y$ = 1 App | | 45 | | V |
| $t_{fly}$ | Flyback time | $I_y$ = 1 App | | 0.7 | | ms |
| $V_{ON}$ | Peak to peak output noise | Pin 11 connected to GND | | | 40 | mV pp |
| $f_o$ | Free running frequency | (P1 + R1) = 260 KΩ C2 = 0.1 μF | | 52.4 | | Hz |
| | | (P1 + R1) = 300 KΩ C2 = 100 nF | | 43.7 | | Hz |
| Δf | Synchronization range | $I_8$ = 0.5 mA | 14 | | | Hz |
| $\frac{\Delta f}{\Delta V_s}$ | Frequency drift with supply voltage | $V_s$ = 10 to 35V | | 0.005 | | Hz/V |
| $\frac{\Delta f}{\Delta T_{pins}}$ | Frequency drift vs. pins 4, 5, 12 and 13 temp. | $T_{tab}$ = 40 to 120°C | | 0.01 | | Hz/°C |

Fig. 2 - AC test circuit

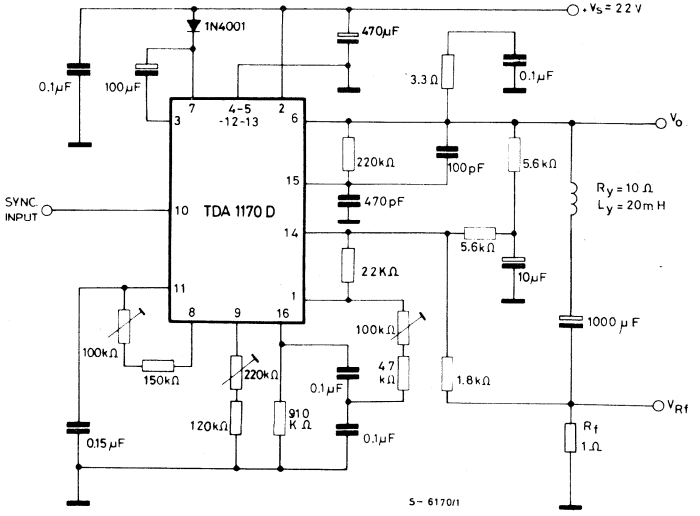


Fig. 3 - Typical application circuit for small screen B/W TV SET (Ry= 2.9Ω, Ly= 6 mH, Iy= 1.1 App)

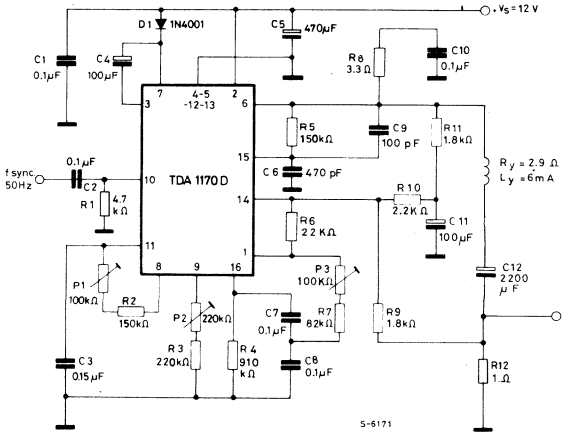
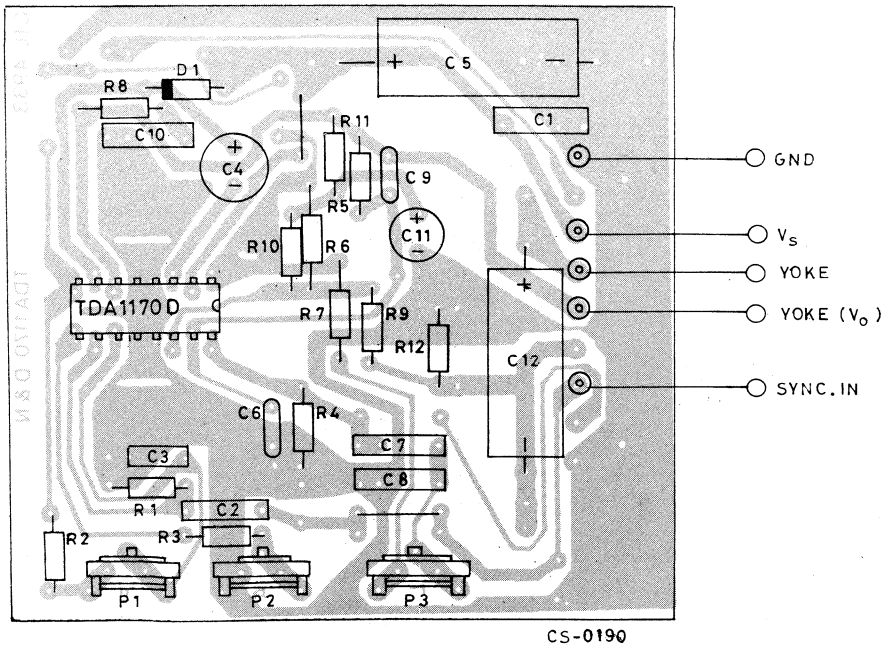



Fig. 4 - P.C. board and components layout of the circuit of fig. 3 (1:1 scale)



## MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA 1170D can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 5) or to an external heatsink (Fig. 6).
The diagram of figure 7 shows the maximum dissipable power $P_{tot}$ and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 5 - Example of P.C.board copper area which is used as heatsink.

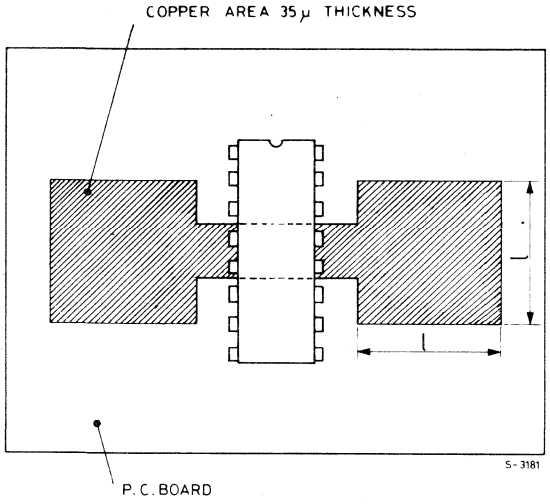



Fig. 6 - External heatsink mounting example

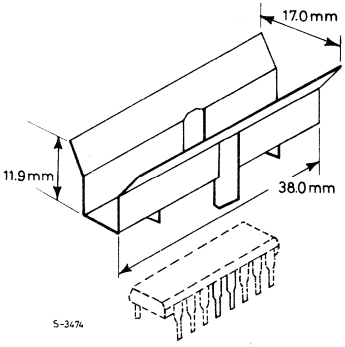



Fig. 7 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

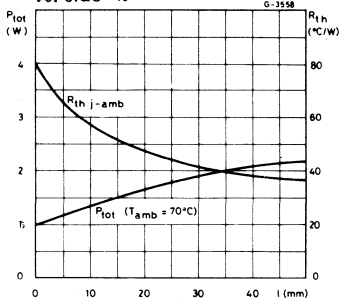
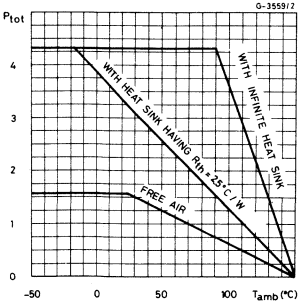



Fig. 8 - Maximum allowable power dissipation vs. ambient temperature



# TDA1170N

# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## LOW-NOISE TV VERTICAL DEFLECTION SYSTEM

- COMPLETE VERTICAL DEFLECTION SYSTEM
- LOW NOISE
- SUITABLE FOR HIGH DEFINITION MONITORS

The TDA 1170N is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers. **Low-noise makes this device particularly suitable for use in monitors.** The functions incorporated are: synchronization circuit, oscillator and ramp generator, high power gain amplifier, flyback generator, voltage regulator.

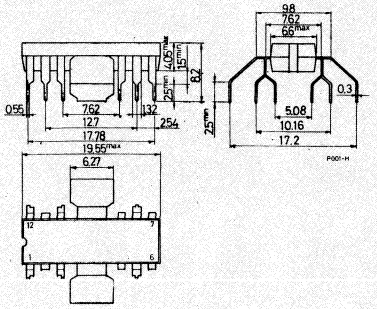
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage at pin 2 | 35 | V |
| V4, V5 | Flyback peak voltage | 60 | V |
| V10 | Power amplifier input voltage | + 10 | V |
| | | - 0.5 | V |
| $I_o$ | Output peak current (non repetitive) at t = 2 msec | 2 | A |
| $I_o$ | Output peak current at f = 50 Hz t $\leqslant$ 10 $\mu$sec | 2.5 | A |
| $I_o$ | Output peak current at f = 50 Hz t $>$ 10 $\mu$sec | 1.5 | A |
| $I_3$ | Pin 3 DC current at V4 $<$ V2 | 100 | mA |
| $I_3$ | Pin 3 peak to peak flyback current for f = 50 Hz, $t_{fly} \leqslant$ 1.5 msec | 1.8 | A |
| $I_8$ | Pin 8 current | $\pm$ 20 | mA |
| $P_{tot}$ | Power dissipation: at $T_{tab}$ = 90°C | 5 | W |
| | at $T_{amb}$ = 80°C (free air) | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

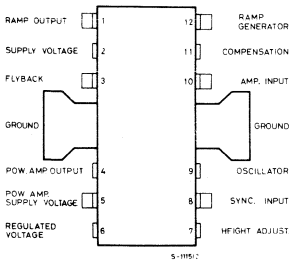
**ORDERING NUMBER:** TDA 1170N

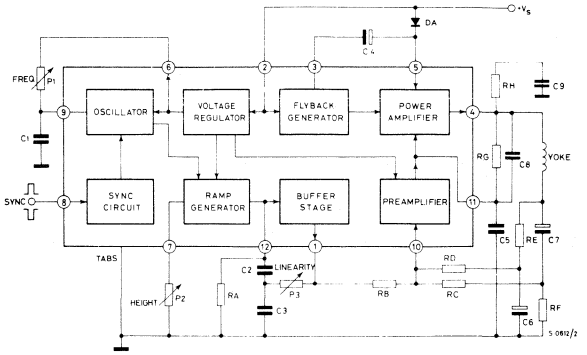
## MECHANICAL DATA

Dimensions in mm

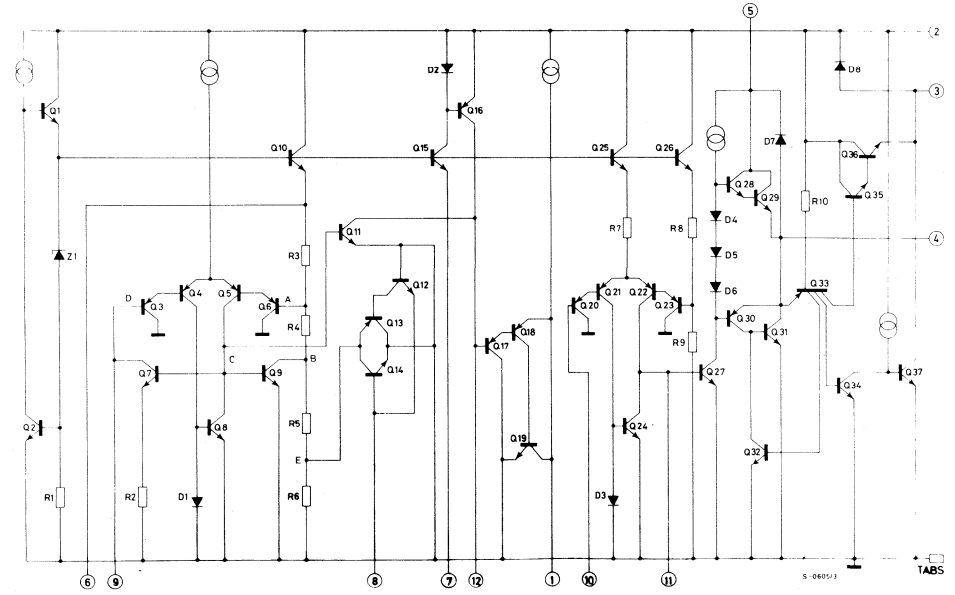


## CONNECTION AND BLOCK DIAGRAMS




## SCHEMATIC DIAGRAM




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}tab}$ | Thermal resistance junction-tab | max | 12 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70 | °C/W(o) |

(o) Obtained with tabs soldered to printed circuit with minimized copper area.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_s$ = 35V, $T_{amb}$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | |
| $I_2$ | Pin 2 quiescent current | $I_3$ = 0 | | 7 | 14 | mA | 1b |
| $I_5$ | Pin 5 quiescent current | $I_4$ = 0 | | 8 | 17 | mA | 1b |
| $-I_9$ | Oscillator bias current | V9 = 1V | | 0.1 | 1 | μA | 1a |
| $-I_{10}$ | Amplifier input bias current | V10= 1V | | 1 | 10 | μA | 1b |
| $-I_{12}$ | Ramp generator bias current | V12= 0 | | 0.02 | 0.3 | μA | 1a |
| $-I_{12}$ | Ramp generator current | $I_7$ = 20 μA V12= 0 | 18.5 | 20 | 21.5 | μA | 1b |
| $\frac{\Delta I_{12}}{I_{12}}$ | Ramp generator non-linearity | ΔV12= 0 to 12V<br>$I_7$ = 20 μA | | 0.2 | 1 | % | 1b |
| $V_s$ | Supply voltage range | | 10 | | 35 | V | – |
| V1 | Pin 1 saturation voltage to ground | $I_1$ = 1 mA | | 1 | 1.4 | V | – |
| V3 | Pin 3 saturation voltage to ground | $I_3$ = 10 mA | | 300 | 450 | mV | 1a |
| V4 | Quiescent output voltage | $V_s$= 10V R1= 1 KΩ<br>R2 = 1 KΩ | 4.1 | 4.4 | 4.65 | V | 1a |
| | | $V_s$= 35V R1= 3 KΩ<br>R2 = 1 KΩ | 8.3 | 8.8 | 9.2 | V | 1a |
| V4L | Output saturation voltage to ground | $-I_4$= 0.1A | | 0.9 | 1.2 | V | 1c |
| | | $-I_4$= 0.8A | | 1.9 | 2.3 | V | 1c |
| V4H | Output saturation voltage to supply | $I_4$ = 0.1A | | 1.4 | 2.1 | V | 1d |
| | | $I_4$ = 0.8A | | 2.8 | 3.2 | V | 1d |
| V6 | Regulated voltage at pin 6 | | 6.1 | 6.5 | 6.9 | V | 1b |
| V7 | Regulated voltage at pin 7 | $I_7$ = 20 μA | 6.2 | 6.6 | 7 | V | 1b |
| $\frac{\Delta V6}{\Delta V_s}$ ; $\frac{\Delta V7}{\Delta V_s}$ | Regulated voltage drift with supply voltage | $\Delta V_s$= 10 to 35V | | 1 | | mV/V | 1b |
| V10 | Amplifier input reference voltage | | 2.07 | 2 2 | 2.3 | V | – |
| R8 | Pin 8 input resistance | V8 ⩽ 0.4V | 1 | | | MΩ | 1a |

Fig. 1 - DC test circuits

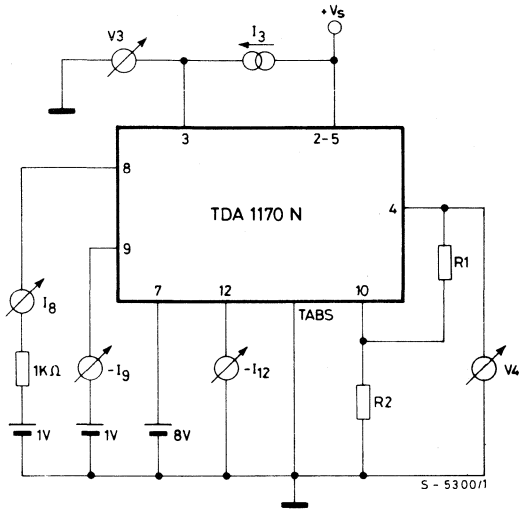



Fig. 1a

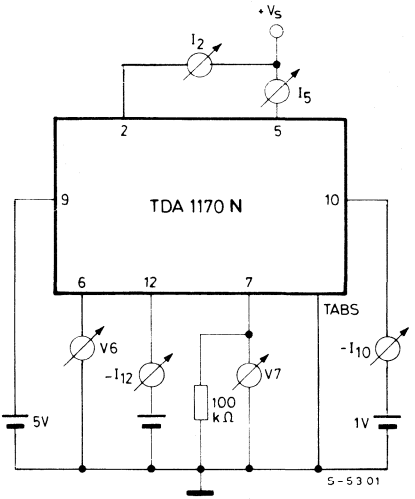



Fig. 1b

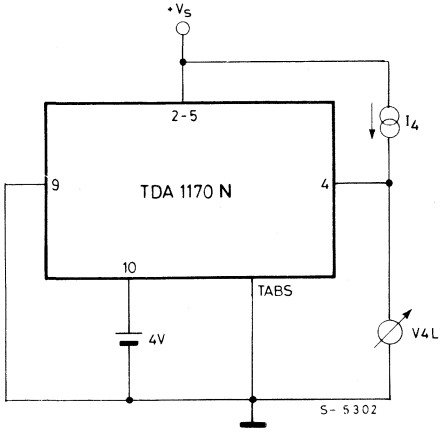



Fig. 1c

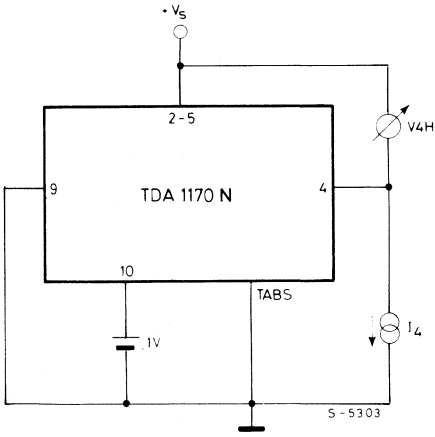



Fig. 1d

## ELECTRICAL CHARACTERISTICS (Refer to the AC test circuit, $V_S$ = 22V; f = 50 Hz; $T_{amb}$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | | |
| $I_s$ | Supply current | $I_y$ = 1 App | | 140 | | mA |
| $I_8$ | Sync. input current (positive or negative) | | 500 | | | μA |
| V4 | Flyback voltage | $I_y$ = 1 App | | 45 | | V |
| $t_{fly}$ | Flyback time | $I_y$ = 1 App | | 0.7 | | ms |
| $V_{oN}$ | Peak to peak output noise | Pin 9 connected to GND | | | 40 | mV pp |
| $f_o$ | Free running frequency | (P1 + R1) = 300 KΩ C2 = 0.1 μF | | 52.4 | | Hz |
| | | (P1 + R1) = 360 KΩ C2 = 100 nF | | 43.7 | | Hz |
| Δf | Synchronization range | $I_8$ = 0.5 mA | 14 | | | Hz |
| $\frac{\Delta f}{\Delta V_s}$ | Frequency drift with supply voltage | $V_s$ = 10 to 35V | | 0.005 | | Hz/V |
| $\left\lvert\frac{\Delta f}{\Delta T_{tab}}\right\rvert$ | Frequency drift with tab temperature | $T_{tab}$ = 40 to 120°C | | 0.01 | | Hz/°C |

Fig. 2 - AC test and application circuit for large screen B/W TV set 10Ω/20 mH/1 App.

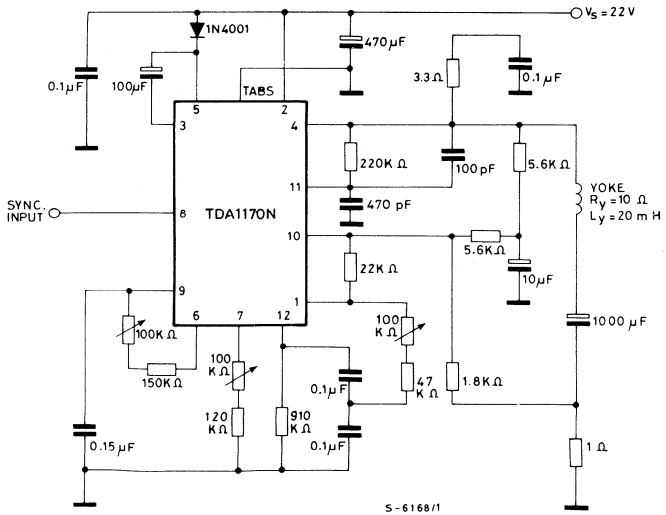


Fig. 3 - Typical application circuit for small screen 90° TVC set (Ry = 15Ω, Ly = 30 mH, Iy = 0.82 App)

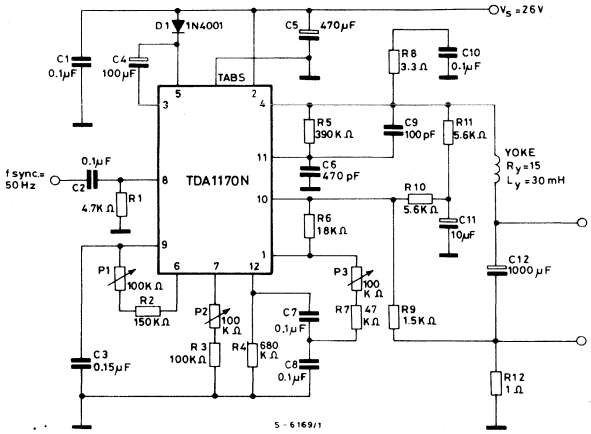
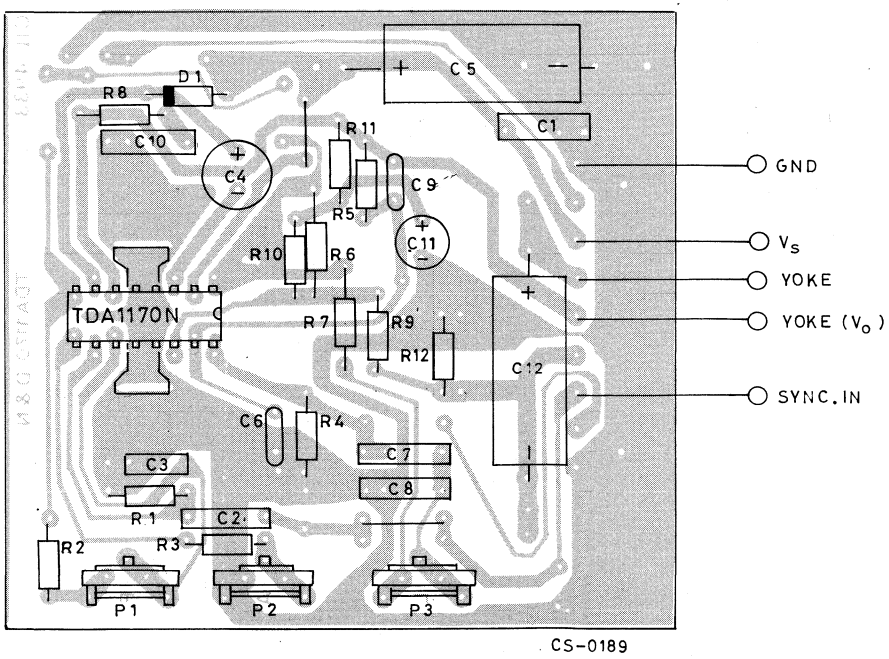



Fig. 4 - P.C. board and components layout of the circuit of fig. 3 (1:1 scale)



## MOUNTING INSTRUCTIONS

During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

The junction to ambient thermal resistance can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 5) or to an external heatsink (fig. 6).

The diagram of fig. 7 shows the maximum dissipable power $P_{tot}$ and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35 $\mu$ (1.4 mil).

Fig. 5 - Example of P.C. board copper area used as heatsink.

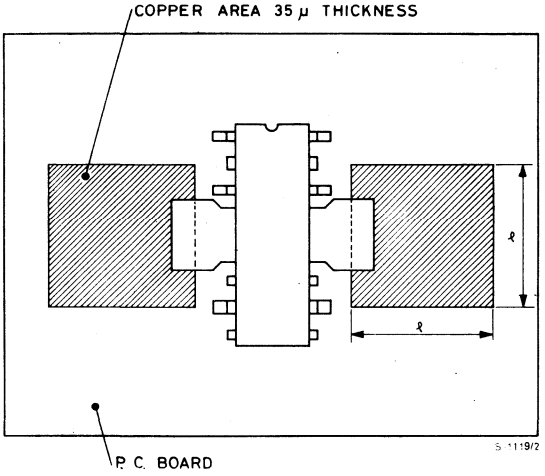



Fig. 6 - Example of external heatsink.

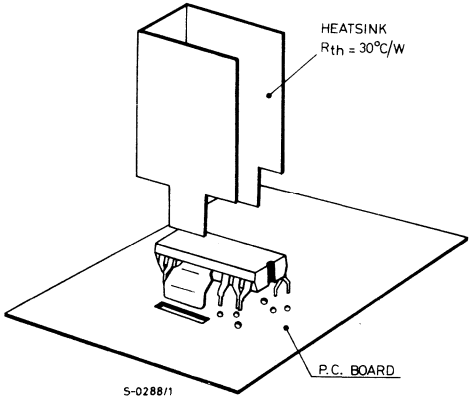



Fig. 7 - Maximum Power dissipation and junctional-ambient thermal resistance vs. "ℓ"

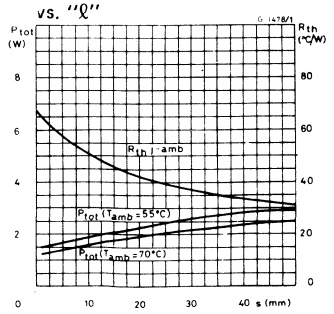
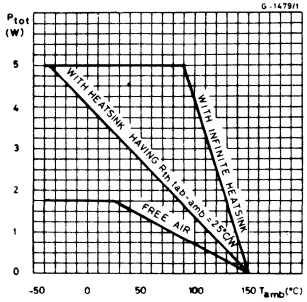



Fig. 8 - Maximum allowable power dissipation versus ambient temperature



# TDA1170S

## TV VERTICAL DEFLECTION SYSTEM

The TDA 1170S is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It is intended for use in black and white and colour TV receivers.
The functions incorporated are:

- synchronization circuit
- oscillator and ramp generator
- high power gain amplifier
- flyback generator
- voltage regulator

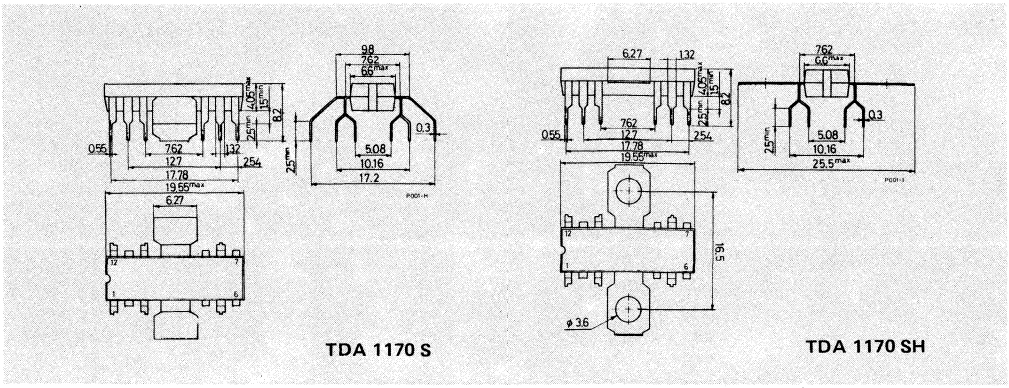
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage at pin 2 | 35 | V |
| $V_4, V_5$ | Flyback peak voltage | 60 | V |
| $V_{10}$ | Power amplifier input voltage | + 10 | V |
| | | - 0.5 | V |
| $I_o$ | Output peak current (non repetitive) at t = 2 msec | 2 | A |
| $I_o$ | Output peak current at f = 50 Hz $t \leqslant 10\ \mu sec$ | 2.5 | A |
| $I_o$ | Output peak current at f = 50 Hz $t > 10\ \mu sec$ | 1.5 | A |
| $I_3$ | Pin 3 DC current at $V_4 < V_2$ | 100 | mA |
| $I_3$ | Pin 3 peak to peak flyback current for f = 50 Hz, $t_{fly} \leqslant 1.5$ msec | 1.8 | A |
| $I_8$ | Pin 8 current | ± 20 | mA |
| $P_{tot}$ | Power dissipation: at $T_{tab}$ = 90°C, at $T_{amb}$ = 80°C } TDA1170S | 5 | W |
| | | 1 | W |
| $T_{stg}, T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBERS:** TDA 1170 S
TDA 1170 SH

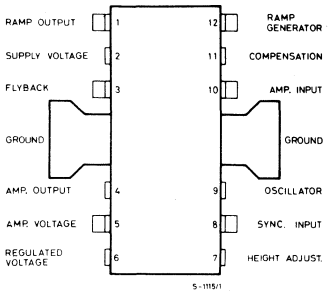
## MECHANICAL DATA

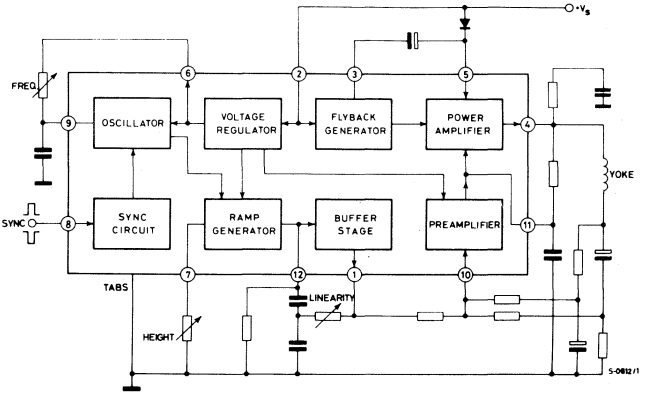
Dimensions in mm



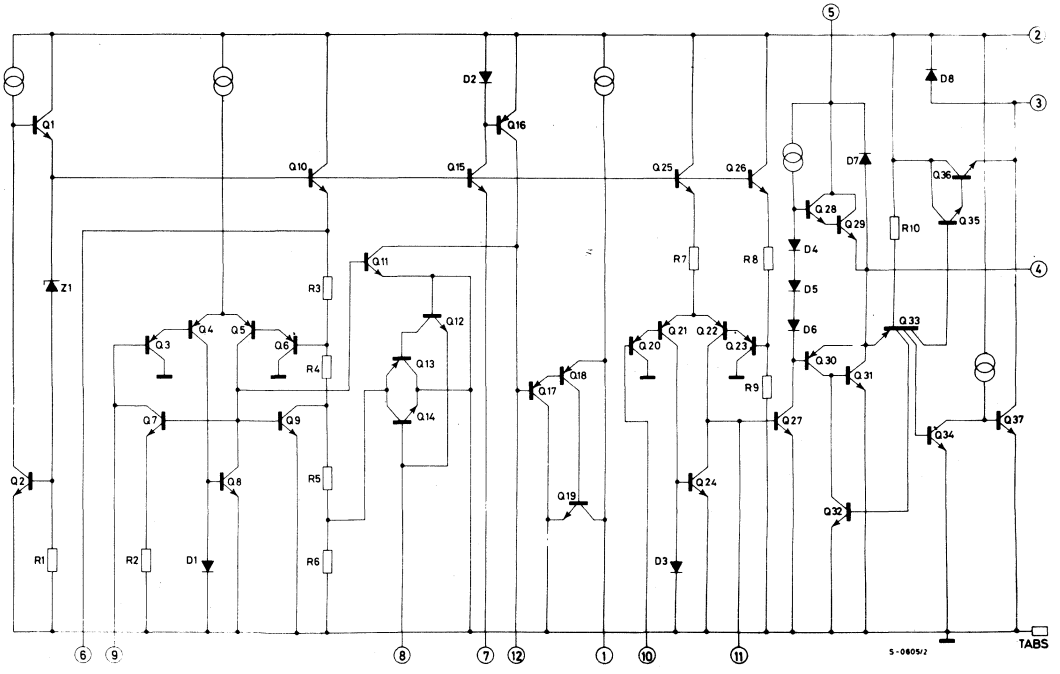
# TDA1170S

## CONNECTION AND BLOCK DIAGRAMS




## SCHEMATIC DIAGRAM



## THERMAL DATA

| | | TDA 1170S | TDA 1170SH |
|---|---|---|---|
| $R_{th\ j\text{-}tab}$ | Thermal resistance junction-tab | max 12°C/W | max 10°C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max 70°C/W(°) | max 80°C/W |

(°) Obtained with tabs soldered to printed circuit with minimized copper area.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_s$= 35V, $T_{amb}$= 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | |
| $I_2$ | Pin 2 quiescent current | $I_3$ = 0 | | 7 | 14 | mA | 1b |
| $I_5$ | Pin 5 quiescent current | $I_4$ = 0 | | 8 | 15 | mA | 1b |
| $-I_9$ | Oscillator bias current | $V_9$ = 1V | | 0.1 | 1 | μA | 1a |
| $-I_{10}$ | Amplifier input bias current | $V_{10}$= 1V | | 0.1 | 1 | μA | 1b |
| $-I_{12}$ | Ramp generator bias current | $V_{12}$= 0 | | 0.02 | 0.3 | μA | 1a |
| $-I_{12}$ | Ramp generator current | $I_7$ = 20 μA $V_{12}$= 0 | 19 | 20 | 24 | μA | 1b |
| $\frac{\Delta I_{12}}{I_{12}}$ | Ramp generator non-linearity | $\Delta V_{12}$= 0 to 12V<br>$I_7$ = 20 μA | | 0.2 | 1 | % | 1b |
| $V_s$ | Supply voltage range | | 10 | | 36 | V | – |
| $V_1$ | Pin 1 saturation voltage to ground | $I_1$ = 1 mA | | 1 | 1.4 | V | – |
| $V_3$ | Pin 3 saturation voltage to ground | $I_3$ = 10 mA | | 1.7 | 2.6 | V | 1a |
| $V_4$ | Quiescent output voltage | $V_s$= 10V $R_1$=10 KΩ<br>$R_2$=10 KΩ | 4.17 | 4.4 | 4.63 | V | 1a |
| | | $V_s$= 35V $R_1$=30 KΩ<br>$R_2$= 10 KΩ | 8.35 | 8.8 | 9.25 | V | 1a |
| $V_{4L}$ | Output saturation voltage to ground | $-I_4$ = 0.1A | | 0.9 | 1.2 | V | 1c |
| | | $-I_4$ = 0.8A | | 1.9 | 2.3 | V | 1c |
| $V_{4H}$ | Output saturation voltage to supply | $I_4$ = 0.1A | | 1.4 | 2.1 | V | 1d |
| | | $I_4$ = 0.8A | | 2.8 | 3.2 | V | 1d |
| $V_6$ | Regulated voltage at pin 6 | | 6.1 | 6.5 | 6.9 | V | 1b |
| $V_7$ | Regulated voltage at pin 7 | $I_7$ = 20 μA | 6.2 | 6.6 | 7 | V | 1b |
| $\frac{\Delta V_6}{\Delta V_s}$ ; $\frac{\Delta V_7}{\Delta V_s}$ | Regulated voltage drift with supply voltage | $\Delta V_s$= 10 to 35V | | 1 | | mV/V | 1b |
| $V_{10}$ | Amplifier input reference voltage | | 2.07 | 2.2 | 2.3 | V | – |
| $R_8$ | Pin 8 input resistance | $V_8 \leq 0.4V$ | 1 | | | MΩ | 1a |

Fig. 1 - DC test circuits

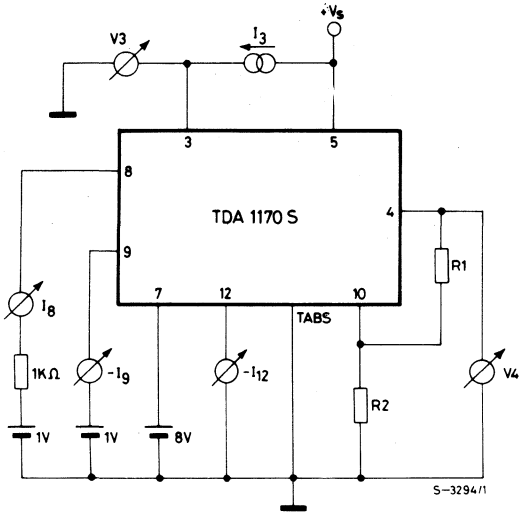



Fig. 1a

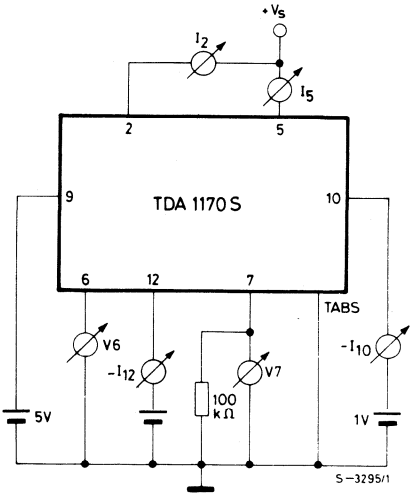



Fig. 1b

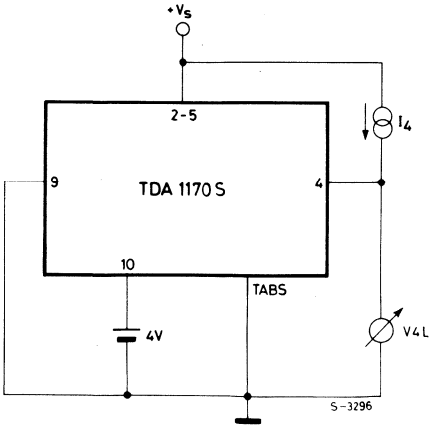



Fig. 1c

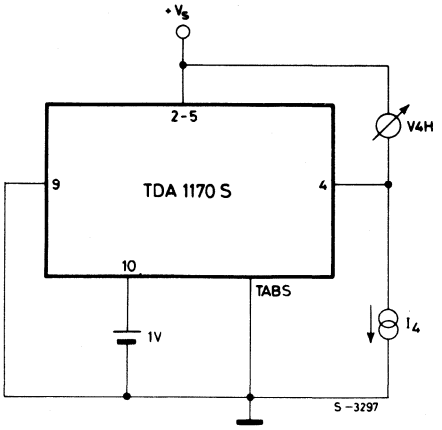



Fig. 1d

## AC CHARACTERISTICS (Refer to the test circuit, $V_S$= 25V; f = 50 Hz; $T_{amb}$= 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| $I_s$ | Supply current | $I_y$ = 1 App | | 140 | | mA | 2 |
| $I_8$ | Sync. input current (positive or negative) | | 500 | | | μA | 2 |
| $V_4$ | Flyback voltage | $I_y$ = 1 App | | 51 | | V | 2 |
| $V_9$ | Peak to peak oscillator sawtooth voltage | | | 2.4 | | V | 2 |
| $t_{fly}$ | Flyback time | $I_y$ = 1 App | | 0.7 | | ms | 2 |
| $f_o$ | Free running frequency | $(P_1 + R_1)$ = 300 KΩ<br>$C_2$ = 100 nF | | 44 | | Hz | 2 |
| | | $(P_1 + R_1)$ = 260 KΩ<br>$C_2$ = 100 nF | | 52 | | Hz | 2 |
| Δf | Synchronization range | $I_8$ = 0.5 mA | 14 | | | Hz | 2 |
| $\frac{\Delta f}{\Delta V_s}$ | Frequency drift with supply voltage | $V_s$ = 10 to 35V | | 0.005 | | Hz/V | 2 |
| $\left\lvert\frac{\Delta f}{\Delta T_{tab}}\right\rvert$ | Frequency drift with tab temperature | $T_{tab}$= 40 to 120°C | | 0.01 | | Hz/°C | 2 |

Fig. 2 - AC test circuit

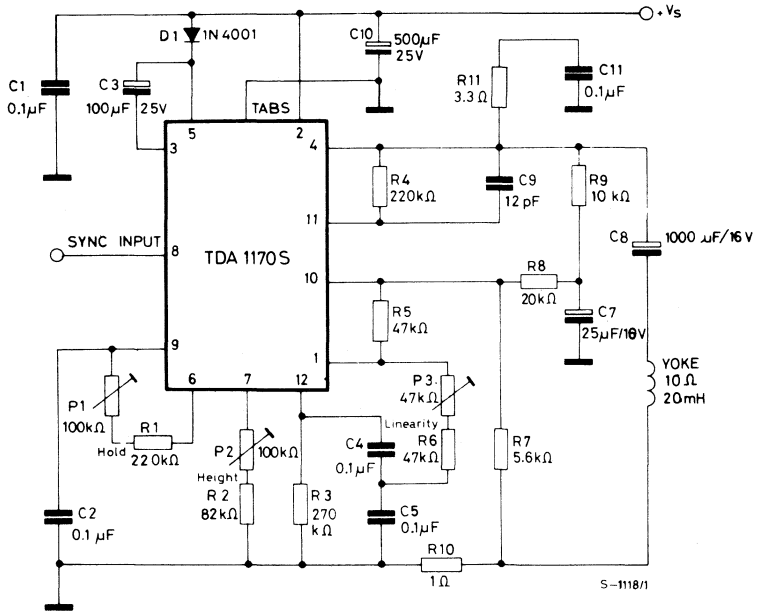
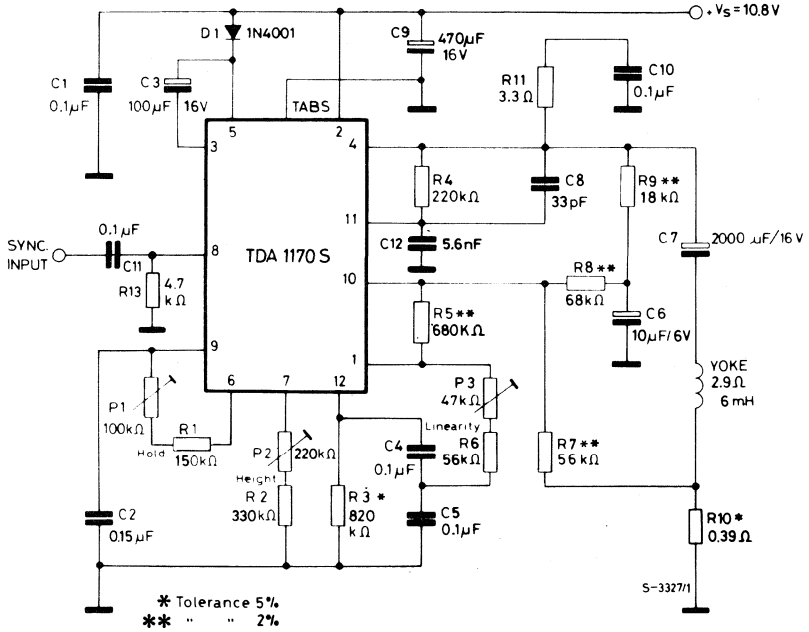


Fig. 3 - Typical application circuit for small screen B/W TV set ($R_y$ = 2.9Ω, $L_y$= 6 mH; $I_y$= 1.1 App)

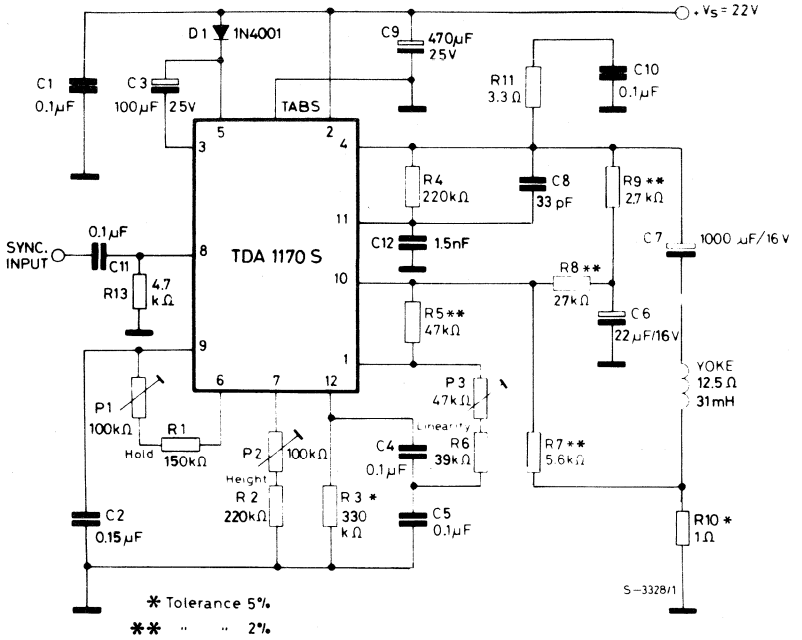



## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Operating supply voltage | 10.8 | V |
| $I_s$ | Supply current | 155 | mA |
| $t_{fly}$ | Flyback time | 0.5 | ms |
| $P_{tot}$ | TDA 1170S power dissipation | 1.35 | W |
| $I_y$ | Maximum scanning current (peak to peak) | 1.30 | A |

For safe working up to $T_{amb}$= 60°C a heatsink of $R_{th}$= 30°C/W is required.

Fig. 4 - Typical application circuit for small screen 90° PIL TVC set ($R_y$= 12.5Ω ; $L_y$= 31 mH; $I_y$= 0.8 App)

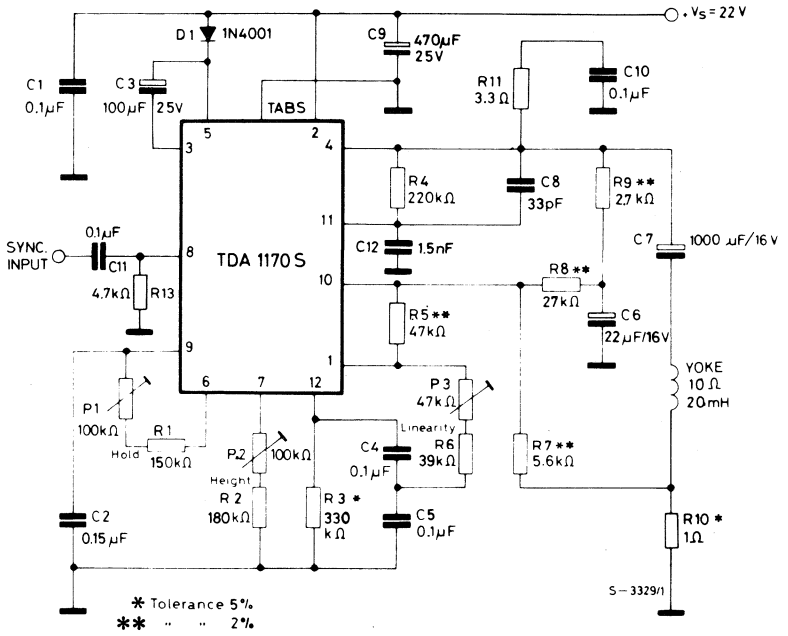



## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Operating supply voltage | 22 | V |
| $I_s$ | Supply current | 120 | mA |
| $t_{fly}$ | Flyback time | 0.8 | ms |
| $P_{tot}$ | TDA 1170S power dissipation | 1.95 | W |
| $I_y$ | Maximum scanning current (peak to peak) | 1.0 | A |

For safe working up to $T_{amb}$= 60°C a heatsink of $R_{th}$= 18°C/W is required.

Fig. 5 - Typical application circuit for large screen B/W TV set ($R_y$= 10Ω ; $L_y$= 20 mH; $I_y$= 1 App)

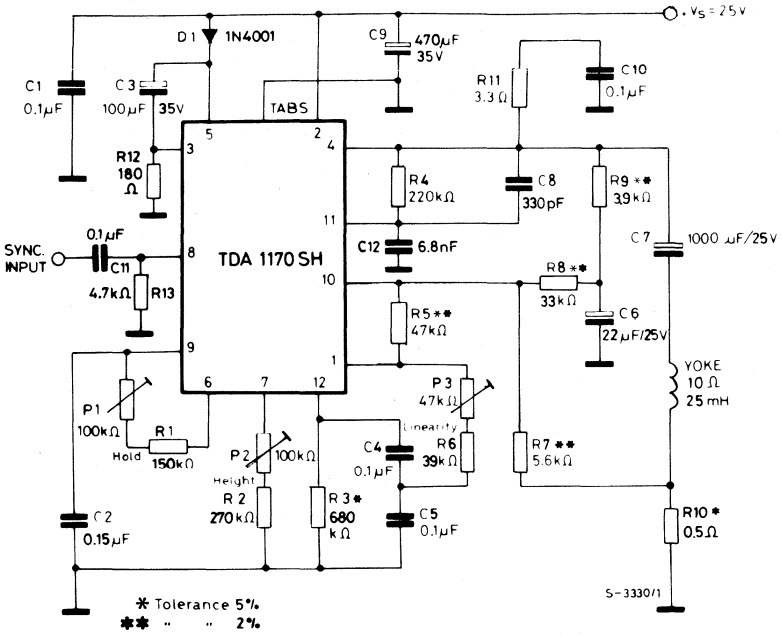



## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Operating supply voltage | 22 | V |
| $I_s$ | Supply current | 145 | mA |
| $t_{fly}$ | Flyback time | 0.7 | ms |
| $P_{tot}$ | TDA 1170S power dissipation | 2.3 | W |
| $I_y$ | Maximum scanning current (peak to peak) | 1.2 | A |

For safe working up to $T_{amb}$= 60°C a heatsink of $R_{th}$= 14°C/W is required.

Fig. 6 - Typical application circuit for large screen 110° PIL TVC set ($R_y$= 10Ω ; $L_y$= 25 mH; $I_y$= 1.25 App)

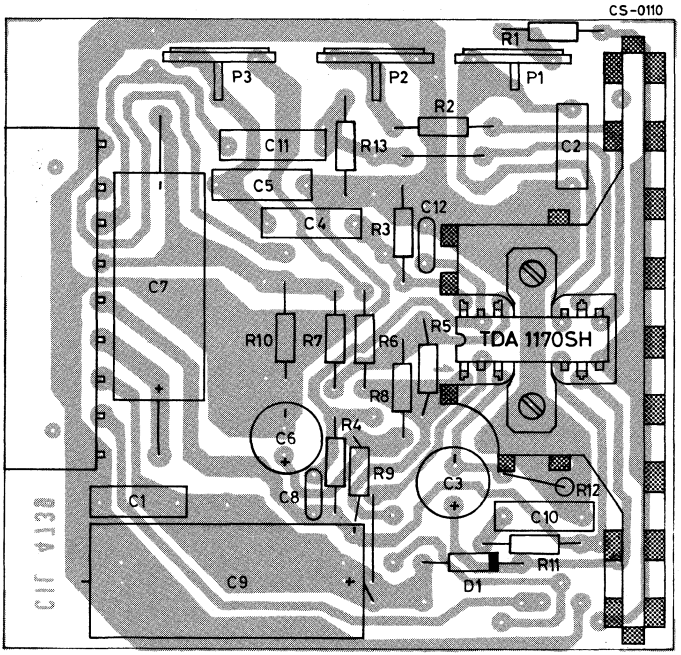



## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Operating supply voltage | 25 | V |
| $I_s$ | Supply current | 175 | mA |
| $t_{fly}$ | Flyback time | 1 | ms |
| $P_{tot}$ | TDA 1170SH power dissipation | 3.25 | W |
| $I_y$ | Maximum scanning current (peak to peak) | 1.4 | A |

For safe working up to $T_{amb}$= 60°C a heatsink of $R_{th}$= 8.5°C/W is required.

Fig. 7 - P.C. board and component layout of the circuit of fig. 6 (1 : 1 scale)




Note: For the heatsink (1170 S and 1170 SH) see mounting instructions

## MOUNTING INSTRUCTIONS

During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

## TDA 1170S

The junction to ambient thermal resistance of the TDA 1170S can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (fig. 8) or to an external heatsink (fig. 9).
The diagram of fig. 10 shows the maximum dissipable power $P_{tot}$ and the $R_{th\ j\text{-}amb}$ as a function of the side "s" of two equal square copper areas having a thickness of 35 $\mu$ (1.4 mil).

## MOUNTING INSTRUCTIONS (continued)

Fig. 8 - Example of P.C. board copper area used as heatsink.

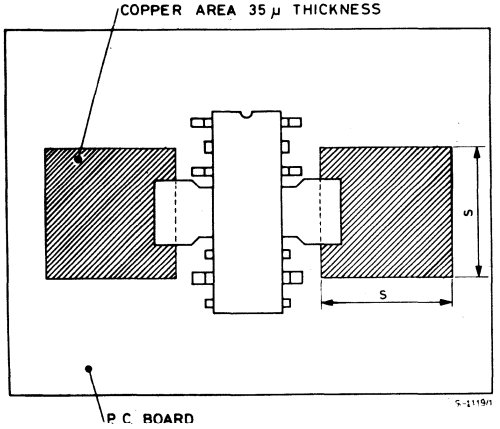



Fig. 9 - Example of TDA 1170 S with external heatsink.

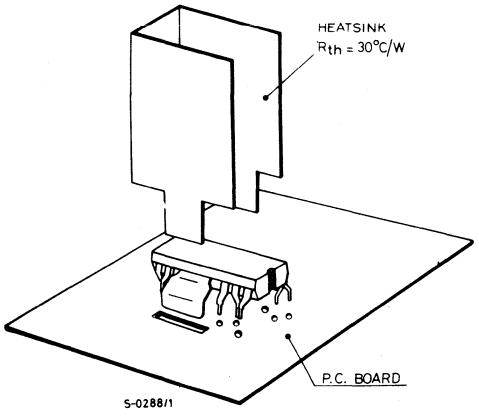



Fig. 10 - Maximum Power dissipation and junctional-ambient thermal resistance vs. "S"

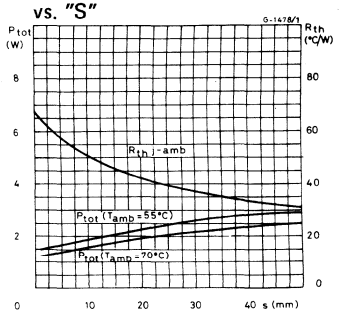



Fig. 11 - Maxim. allowable power dissipation vs. ambient temp. (TDA1170S)

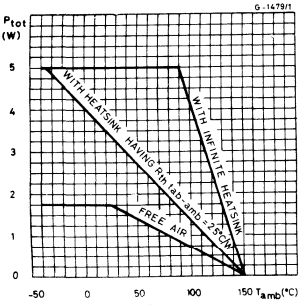
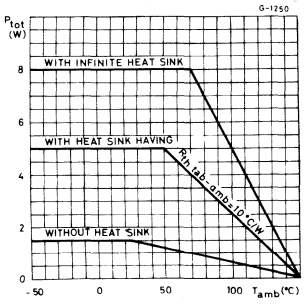



Fig. 12 - Maxim. allowable power dissipation vs. ambient temp. (TDA1170SH)

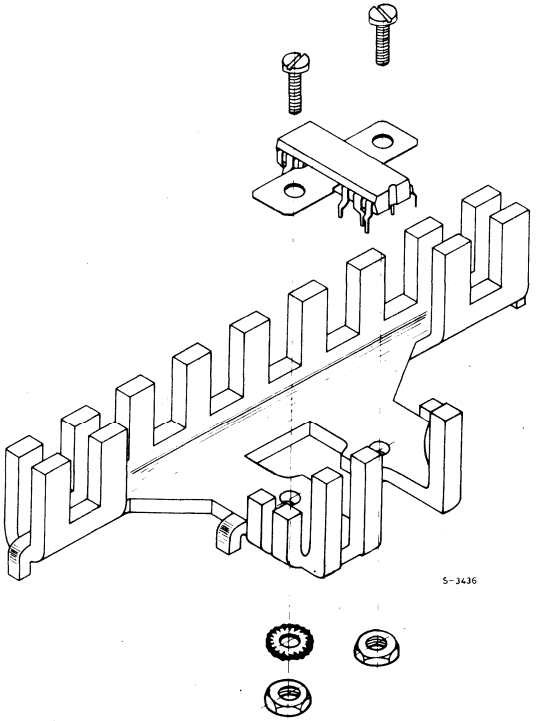



## TDA 1170SH

The power dissipated in the circuit may be removed by connecting the tabs to an external heatsink according to fig. 12. The desired thermal resistance may be obtained by fixing the TDA1170SH to a suitable dimensioned plate as shown in fig. 13.

## MOUNTING INSTRUCTIONS (continued)

Fig. 13 - Mounting example.



# TDA1180P

## TV HORIZONTAL PROCESSOR

The TDA 1180P is a horizontal processor circuit for b.w. and colour television receiver. It is a monolithic integrated circuit encapsulated in 16-lead dual in-line plastic package. The TDA 1180P combines the following functions:

- Noise gated horizontal sync separator.
- Noise gated vertical sync separator.
- Horizontal oscillator with frequency range limiter.
- Phase comparator between sync pulses and oscillator pulses (PLL).
- Phase comparator between flyback pulses and oscillator pulses (PLL).
- Loop gain and time constant switching (VCR).
- Composite blanking and key pulse generator.
- Protection circuits.
- Output stages with high current capability.

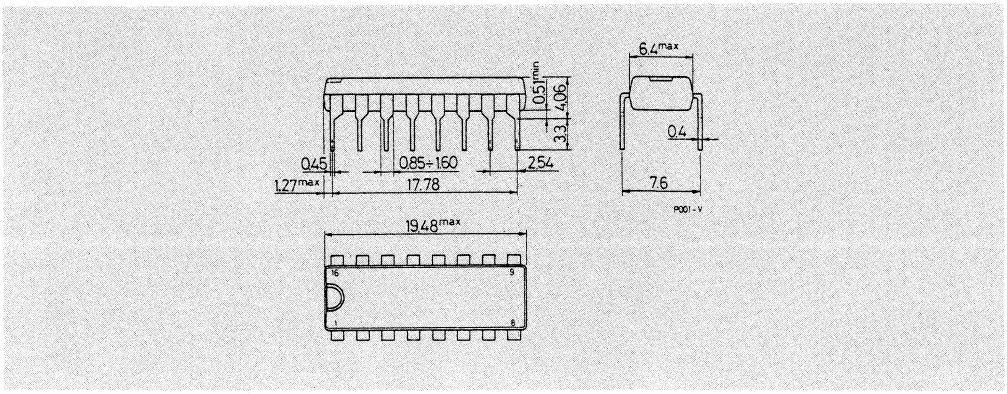
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 1) | 15 | V |
| $V_2$ | Voltage at pin 2 | 18 | V |
| $V_4$ | Voltage at pin 4 | $V_s$ | |
| $V_8$ | Voltage at pin 8 | $\begin{cases} V_s \\ -6 \end{cases}$ | V |
| $V_9$ | Voltage at pin 9 | $\begin{cases} +6 \\ -6 \end{cases}$ | V |
| $V_{11}$ | Voltage at pin 11 | $V_s$ | |
| $I_2$ | Pin 2 peak current | 1 | A |
| $I_3$ | Pin 3 peak current | 0.5 | A |
| $I_6$ | Pin 6 current | 30 | mA |
| $I_7$ | Pin 7 current | 20 | mA |
| $I_{10}$ | Pin 10 current | 30 | mA |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 70°C$ | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA 1180P

## MECHANICAL DATA

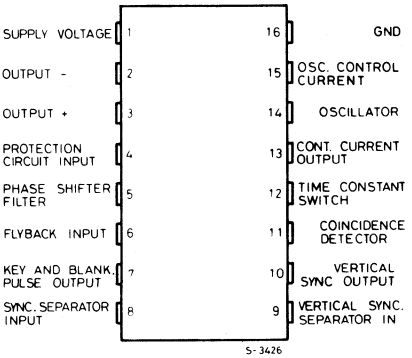
Dimensions in mm



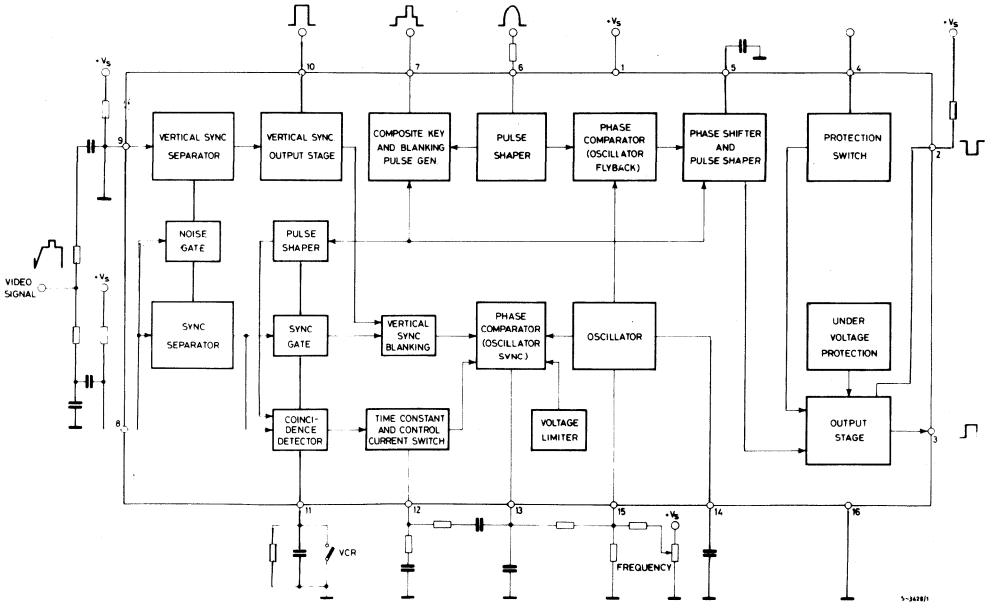
# TDA1180P

## CONNECTION DIAGRAM

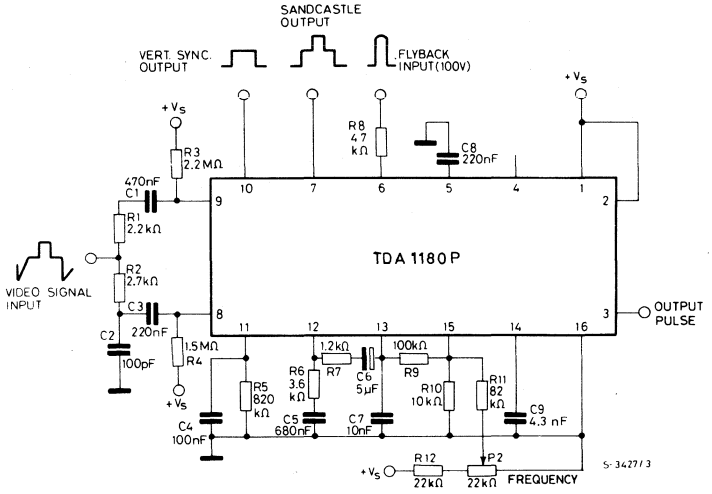
(top view)




## BLOCK DIAGRAM



## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 80 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s$= 12V, $T_{amb}$= 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage range | | 10 | 12 | 13.2 | V |
| $I_s$ | Supply current | $I_3$= 0 | | 40 | 52 | mA |
| $V_s$ | Supply voltage at which the output pulses (at pin 2 and 3) are switched off | | | | 4 | V |
| **HORIZONTAL SYNC. SEPARATOR AND NOISE GATE** | | | | | | |
| $V_i$ | Peak to peak input signal | | 1 | 3 | 6 | V |
| $V_8$ | Input switching voltage | $I_8$ = 80 µA | | 1.5 | | V |
| $I_8$ | Input switching current | $V_8$ = 1.4V | | 10 | | µA |
| $I_8$ | Input blocking current for noise suppression | | | 0.9 | | mA |
| $V_8$ | Input switching voltage for noise suppression | | | 2.1 | | V |
| $I_8$ | Leakage current | $V_8$ = -5V | | | 1 | µA |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **VERTICAL SYNC. SEPARATOR** | | | | | | |
| $V_I$ | Peak to peak input signal | | 1 | 3 | 6 | V |
| $V_9$ | Input switching voltage | $I_9$ = 80 μA | | 1.5 | | V |
| $I_9$ | Input switching current | $V_9$ = 1.4V | | 5 | | μA |
| $I_9$ | Leakage current | $V_9$ = -5V | | | 1 | μA |
| $V_{10}$ | Vertical sync. pulse output voltage | No load at pin 10 | 11 | | | V |
| $R_{10}$ | Output resistance | | | 10 | | KΩ |
| $t_{LV}$ | Delay between leading edge of input and output signals | | | 17 | | μs |
| $t_{TV}$ | Delay between trailing edge of input and output signals | | | 50 | | μs |
| $t_V$ | Vertical sync pulse duration | | | 190 | | μs |
| **PROTECTION CIRCUIT** | | | | | | |
| $V_4$ | Input voltage for switching off the output pulses | Output pulses OFF | | | 0.5 | V |
| | | Output pulses ON | 1 | | | |
| $R_4$ | Input resistance | | | 200 | | KΩ |
| $I_4$ | Input current | | 5 | | | μA |
| **FLYBACK PULSE** | | | | | | |
| $V_6$ | Input threshold voltage of blanking generator | | | 1.5 | | V |
| $V_6$ | Input threshold voltage of phase comparator | | | 7.6 | | V |
| $I_6$ | Input switching current | $V_6 \geq 1.7V$ | | 0.23 | | mA |
| **OUTPUT PULSE** | | | | | | |
| $V_3$ | Peak to peak output voltage | $I_3$ = 150 mApp | | 10 | | V |
| $I_3$ | Output current | $V_3$ = 5V | | 500 | | mA |
| $R_3$ | Output resistance | at leading edge of output pulse | | 3 | | Ω |
| | | at trailing edge of output pulse | | 20 | | |
| $t_p$ | Output pulse duration | | 20 | 22 | 26 | μs |
| **COMPOSITE BLANKING AND KEY PULSE** | | | | | | |
| $V_{7K}$ | Key pulse output peak voltage | | 9 | 11 | | V |
| $V_{7B}$ | Blanking pulse output voltage | | 4.2 | 4.5 | 4.8 | V |
| $R_7$ | Output resistance | | | 100 | | Ω |
| $t_{SK}$ | Phase relation between trailing edge of key pulse and middle of sync input pulse | | | 2.7 | | μs |
| $t_K$ | Key pulse duration | | 3.5 | 3.8 | | μs |
| $t_{fb}$ | Delay between flyback pulse and blanking pulse | $V_6$ = 1.7 V | | | 0.2 | μs |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **INTERNAL GATING PULSE** | | | | | |
| $t_g$ Gating pulse duration | | | 7.5 | | µs |
| t Phase relation between middle of sync pulse and trailing and leading edge of gating pulse | | | 3.75 | | µs |
| **COINCIDENCE DETECTOR** | | | | | |
| $V_{11}$ Output voltage | with coincidence | | 6.8 | | V |
| | without coincidence | | | 4 | |
| $I_{11}$ Peak output current | | | 0.5 | | mA |
| **VCR SWITCH** | | | | | |
| $V_{11}$ Input voltage | | 0 to 4 or 8.5 to 12 | | | V |
| $-I_{11}$ Output current | | 35 | | | µA |
| $I_{11}$ Output current | | 0.4 | | | mA |
| **TIME CONSTANT SWITCH** | | | | | |
| $V_{12}$ Output voltage | | | 3 | | V |
| $R_{12}$ Output resistance | $4.5V < V_{11} < 8V$ | | 100 | | Ω |
| | $V_{11} > 8.5V$ or $V_{11} < 4V$ | | 40 | | KΩ |
| **OSCILLATOR** | | | | | |
| $V_{14}$ Low level threshold voltage | | | 5.4 | | V |
| $V_{14}$ High level threshold voltage | | | 8.2 | | V |
| $I_{14}$ Charge current | | | 0.6 | | mA |
| $I_{14}$ Discharge current | | | 0.3 | | mA |
| $V_{15}$ Current source supply voltage | | | 3 | | V |
| $I_{15}$ Current source supply current | | | 0.3 | | mA |
| $f_o$ Free running frequency | | | 15625 | | Hz |
| $\frac{\Delta f_o}{f_o}$ Adjustment range | | | ± 10 | | % |
| $\frac{\Delta f_o}{\Delta I_{15}}$ Frequency control sensitivity | | | 52 | | $\frac{Hz}{\mu A}$ |
| $\Delta f_o$ Frequency change when $V_s$ drops to 4V | | | | ± 10 | % |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **OSCILLATOR-FLYBACK PULSE PHASE COMPARATOR** | | | | | | |
| $V_5$ | Control voltage range | | | 9.4 to 8.2 | | V |
| $I_5$ | Peak control current | | | | ± 0.5 | mA |
| $I_5$ | Input current (blocked phase detector) | | | | 5 | μA |
| $t_d$ | Permissible delay between output pulse leading edge and flyback pulse leading edge | | | $t_p - t_f$ | | μs |
| $\frac{\Delta t}{\Delta t_d}$ | Static control error | | | | 0.2 | % |
| **SYNC PULSE-OSCILLATOR PHASE COMPARATOR** | | | | | | |
| $V_{13}$ | Control voltage range | | | 4.6 to 1.4 | | V |
| $I_{13}$ | Control peak current | | | ±2 | | mA |
| $\frac{\Delta f}{\Delta t}$ | Phase lock loop gain | | | 2 | | $\frac{KHz}{\mu s}$ |
| f | Catching and holding range | | | ± 700 | | Hz |
| **OVERALL PHASE RELATIONSHIP** | | | | | | |
| $t_o$ | Phase relation between middle of flyback pulse and middle of sync pulse | | | 2.6 | | μs |
| $\frac{\Delta V_5}{\Delta t_o}$ | Adjustment sensitivity | | | 65 | | $\frac{mV}{\mu s}$ |
| $\frac{\Delta I_5}{\Delta t_o}$ | Adjustment sensitivity | | | 10 | | $\frac{\mu A}{\mu s}$ |

Fig. 1 - Vertical sync. output pulse

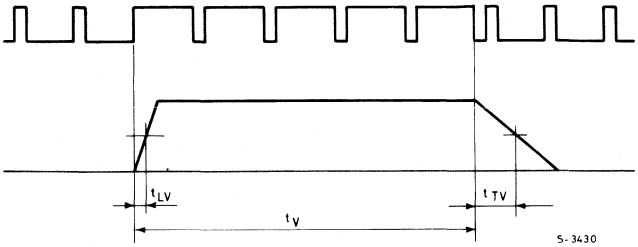



Fig. 2 - Relationship of main waveform phases

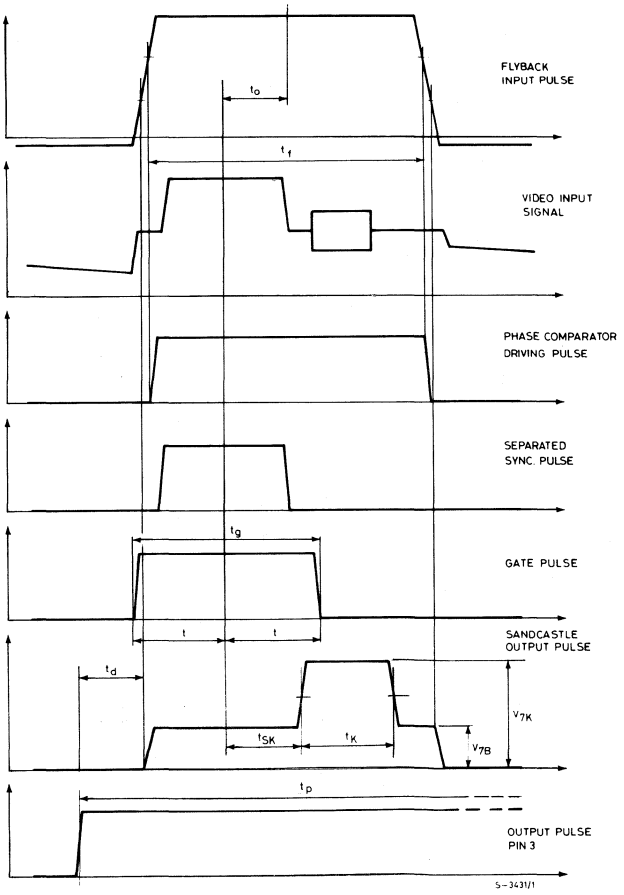


Fig. 3 - Free running frequency vs. supply voltage

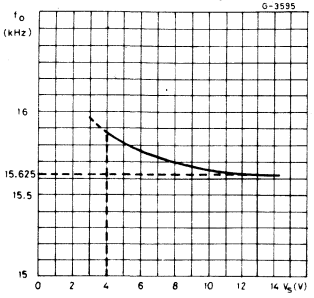



Fig. 4 - Overall phase relation vs. supply voltage

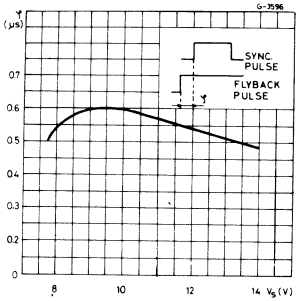
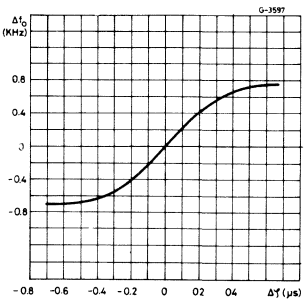



Fig. 5 - Loop gain




## APPLICATION INFORMATION

### Pin 1 — Positive supply

The operating supply voltage of the device ranges from 10V to 13.2V.

### Pin 2 and 3 — Output

The outputs of TDA 1180P are suitable for driving transistor output stages, they deliver positive pulse at pin 3 and negative pulse at pin 2.
The negative pulse is used for direct driving of the output stage, while positive pulse is useful when a driver stage is required.
The rise and fall times of the output pulses are about 150 ns so that interference due to radiation are avoided.
Furthermore the output stages are internally protected against short circuit.

### Pin 4 — Protection circuit input

By connecting pin 4 of the IC to earth the output pulses at pin 2 and 3 are shut off; this function has been introduced to protect the final stages from overloads.
The same pulses are also shut off when the supply voltage falls below 4V.

### Pin 5 — Phase shifter filter

To compensate for the delay introduced by the line final stages, the flyback pulses to pin 6 and the oscillator waveform are compared in the oscillator-flyback pulse phase comparator.
The result of the comparison is a control current which, after it has been filtered by the external capacitor connected to pin 5, is sent to a phase shifter which adequately regulates the phase of the output pulses.
The maximum phase shift allowed is:

$$t_d = t_p - t_f$$

where $t_f$ is the flyback pulse duration.
Pin 5 has high input and output resistance (current generator).

## APPLICATION INFORMATION (continued)

### Pin 6 – Flyback input

The flyback pulse drives the high impedance input through a resistor in order to limit the input current to suitable maximum values.
The flyback input pulses are processed by a double threshold circuit; this generates the blanking pulses by sensing low level flyback voltage and the pulses to drive the phase comparator by sensing high level flyback voltage, therefore phase jitter caused by ringing normally associated with the flyback pulse, is avoided.

### Pin 7 – Key and blanking pulse output

The key pulse for taking out the burst from the chrominance signal is generated from the oscillator ramp and has therefore a fixed phase position with respect to the sync.
The key pulse is then added internally to the blanking pulse obtained by correctly forming the flyback pulse present at pin 6.
The sum of the two signals (sandcastle pulse) is available on low impedance at output pin 7.

### Pin 8 and 9 – Sync separators inputs

The video signal is applied by means of two distinct biasing networks to pins 8 and 9 of the IC and therefore to the respective vertical and horizontal sync separators.
The latter take the sync pulses out of the video signal and make them available to the rest of the circuit for further processing.
An amplitude detector also connected to pin 8, blocks operation of the sync separators when interference or noise peaks exceed a certain preset value.

### Pin 10 – Vertical sync output

The vertical sync pulse, obtained by internal integration of the synchronizing signal, is available at this pin.
The output impedance is typically 10KΩ and the lowest amplitude without load is 11V.

### Pin 11 – Coincidence detector

From the oscillator waveform a gate pulse 7 μs wide is taken whose phase position is centered on the horizontal syncronism.
The gate pulse not only controls a logic block which permits the sync to reach the oscillator-sync phase comparator only for as long as its duration, but also allows the latching and de-latching conditions of the oscillator to be established.
This function is obtained by a coincidence detector which compares the phase of the gate pulses with that of the sync.
When the two signals are not accurately aligned in time it means that the oscillator is not synchronized. In this case the detector acts on the logic block to eliminate its filtering effect and on the time constant switching block to establish a high impedance on pin 12 (small time constant of low-pass filter).
This latter block also acts on the oscillator-sync phase detector to increase its sensitivity and with it the loop gain of the synchronizing system.
In this conditions the phase lock has low noise immunity (wide equivalent noise bandwidth) and rapid pull-in time which allows fairly short synchronization times.

## APPLICATION INFORMATION (continued)

Once locking has taken place the coincidence detector enables the logic block, causes a low impedance on pin 12 and reduces the sensitivity of the phase comparator.
In these conditions the phase lock has high noise immunity (narrow equivalent noise bandwidth) due to the complete elimination of interference which occurs during the scanning period and the greater inertia with which the oscillator can change its frequency.
To optimize the behaviour of the IC if a video recorder is used, the state of the detector can be forced by connecting pin 11 to earth or to $+V_s$. The characteristics of the phase lock thus correspond to the lack of synchronization.

### Pin 12 – Time constant switch, (see pin 11)

### Pin 13 – Control current output

The oscillator is synchronized by comparing the phase of its waveform with that of the sync pulses in the oscillator-sync phase comparator and sending its output current $I_{13}$ (proportional to the phase difference between the two signals) to pin 15 of the oscillator after it has been filtered properly with an external low-pass circuit.
The time constant of the filter can be switched between two values according to the impedance presented by pin 12.
The voltage limiter at the output of the phase comparator limits the voltage excursion on pin 13 and therefore the frequency range in which the oscillator remains held-in.
The output resistance of pin 13 is :

low when $V_{13} > 4.3V$ or $V_{13} < 1.6V$
high when $1.6V < V_{13} < 4.3V$

To prevent the vertical sync from reaching the oscillator-sync phase comparator along with the horizontal sync, a signal which inhibits the phase detector during the vertical interval is taken from the vertical output stage; inhibition remains even if the video signal is not present.
The free running frequency of the oscillator is determined by the values of the capacitor and of the resistor connected to pins 14 and 15 respectively.
To generate the line frequency output pulses, two thresholds are fixed along the fall ramp of the triangular waveform of the oscillator.

### Pin 14 – Oscillator (see pin 13)

### Pin 15 – Oscillator control current input (see pin 13)

### Pin 16 – Ground

Fig. 6 - Application circuit for large screen b.w. and colour TV

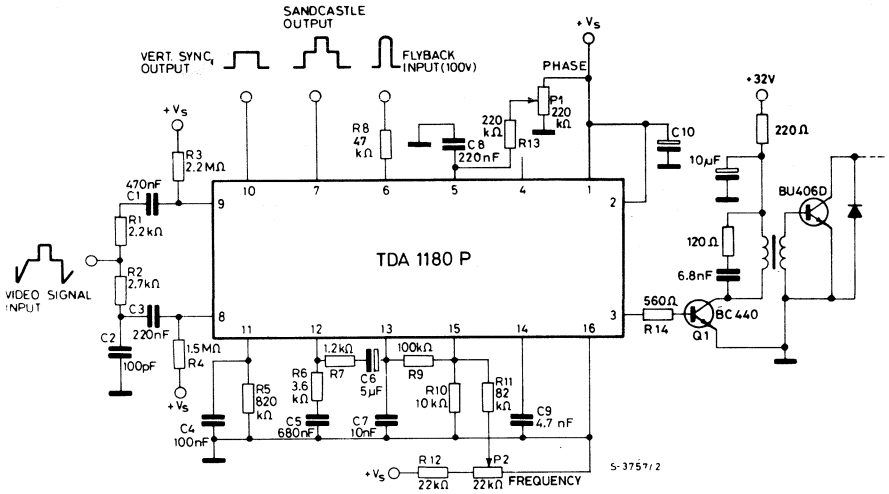



Fig. 7 - P.C. board and component layout for the circuit in fig. 6 (1:1 scale)

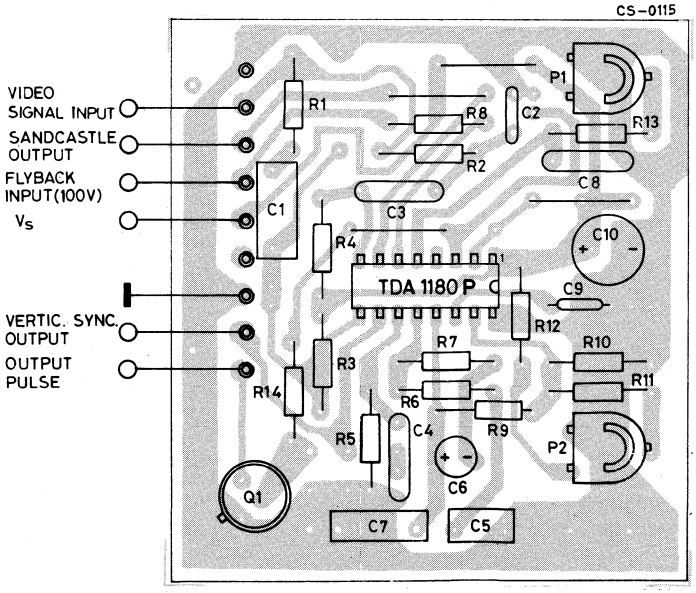


Fig. 8 - Application circuit for small screen b.w. TV.

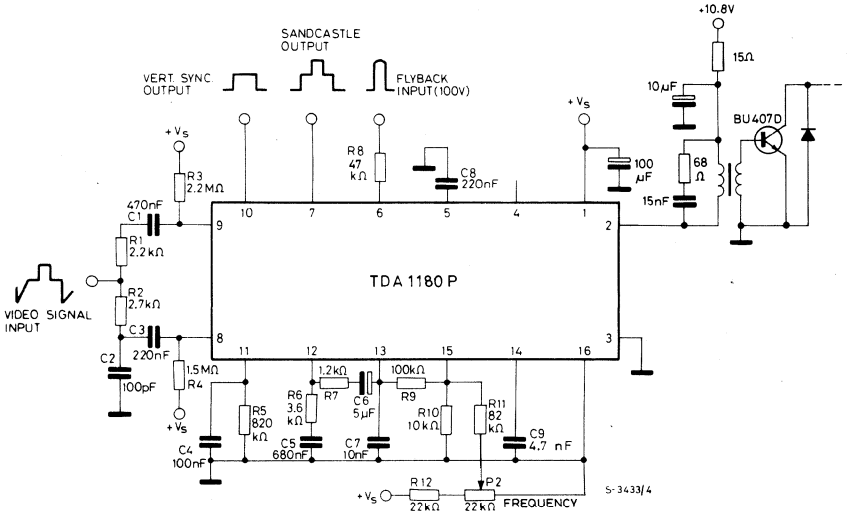
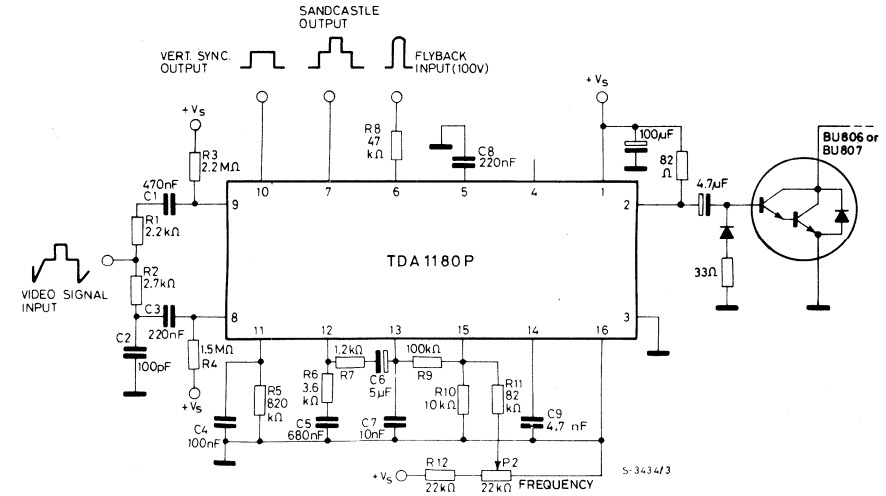



Fig. 9 - Application circuit for Darlington output stage



# TDA1190Z

## COMPLETE TV SOUND CHANNEL

The TDA 1190Z is a monolithic integrated circuit in a 12-lead quad in-line plastic package. It performs all the functions needed for the TV sound channel:

- IF limiter-amplifier
- Active low-pass filter
- FM detector
- DC volume control
- AF preamplifier
- AF output stage

The TDA 1190Z can give an output power of 4.2W (d = 10% ) into a 16Ω load at $V_s$ = 24V, or 1.5W (d = 10% ) into an 8Ω load at $V_s$ = 12V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables the device to be used in almost every type of television receivers.
The device has no irradiation problems, hence no external screening is needed.

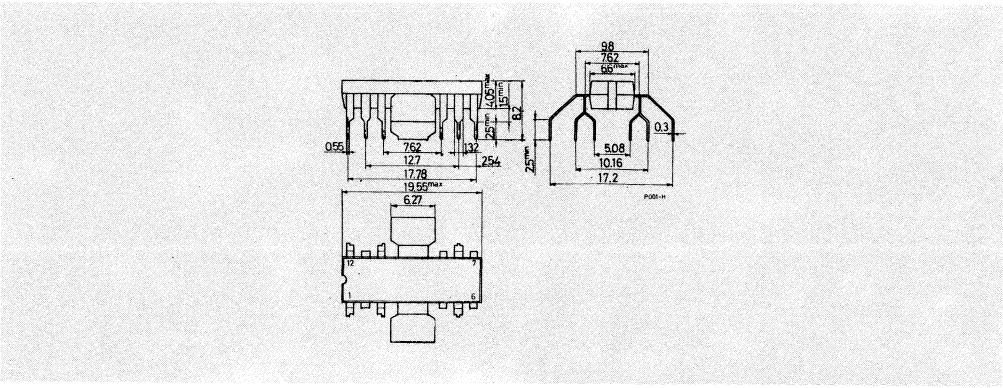
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 10) | 28 | V |
| $V_i$ | Input signal voltage (pin 1) | 1 | V |
| $I_o$ | Output peak current (non-repetitive) | 2 | A |
| $I_o$ | Output peak current (repetitive) | 1.5 | A |
| $P_{tot}$ | Power dissipation: at $T_{tab}$ = 90°C | 5 | W |
| | at $T_{amb}$ = 80° (free air) | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA 1190Z

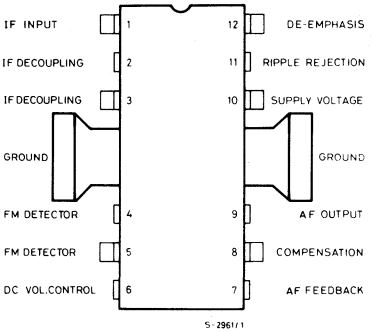
## MECHANICAL DATA

Dimensions in mm

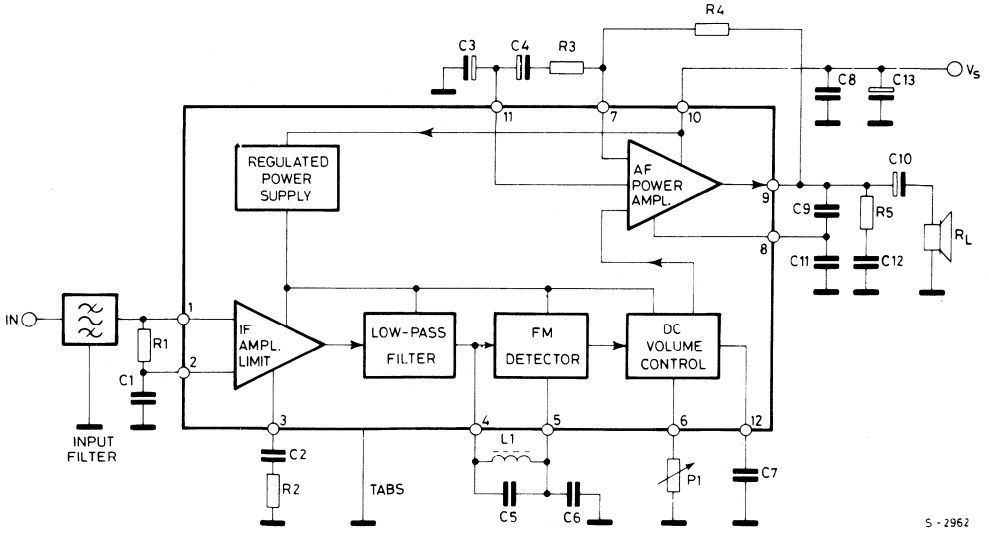


# TDA1190Z

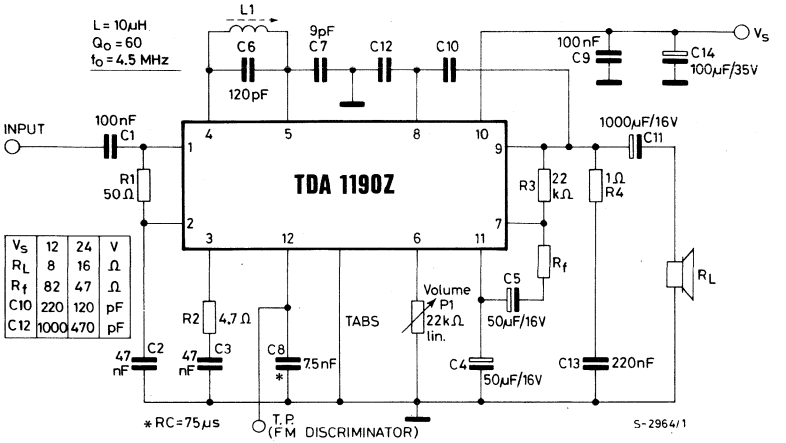
## CONNECTION DIAGRAM
(top view)




## BLOCK DIAGRAM



## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}tab}$ | Thermal resistance junction-tab | max. | 12 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max. | 70* | °C/W |

* Obtained with tabs soldered to printed circuit with minimized copper area.

## ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, $V_s$ = 24V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage (pin 10) | | 9 | | 28 | V |
| $V_o$ | Quiescent output voltage (pin 9) | $V_s$ = 24V<br>$V_s$ = 12V | 11<br>5.1 | 12<br>6 | 13<br>6.9 | V<br>V |
| $I_d$ | Quiescent drain current | $P_1$ = 22 KΩ<br>$V_s$ = 24V<br>$V_s$ = 12V | 11 | 22<br>19 | 45<br>40 | mA<br>mA |
| $P_o$ | Output power | d = 10% $f_m$ = 400 Hz<br>$f_o$ = 4.5 MHz Δf = ±25 kHz<br>$V_s$ = 24V $R_L$ = 16Ω<br>$V_s$ = 12V $R_L$ = 8Ω | | <br><br>4.2<br>1.5 | | <br><br>W<br>W |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $P_o$ | Output power | d = 2% $f_m$ = 400 Hz<br>$f_o$ = 4.5 MHz $\Delta f$ = +25 kHz<br>$V_s$ = 24V $R_L$ = 16Ω<br>$V_s$ = 12V $R_L$ = 8Ω | | <br><br>3.5<br>1.4 | | <br><br>W<br>W |
| $V_i$ | Input limiting voltage (-3 dB) at pin 1 | $f_o$ = 4.5 MHz $\Delta f$ = ±7.5 kHz<br>$f_m$ = 400 Hz<br>$P_1$ = 0 | | <br><br>40 | <br><br>100 | <br><br>μV |
| d | Distortion | $P_o$ = 50 mW $f_m$ = 400 Hz<br>$f_o$ = 4.5 MHz $\Delta f$ = ±7.5 kHz<br>$V_s$ = 24V $R_L$ = 16Ω<br>$V_s$ = 12V $R_L$ = 8Ω | | <br><br>0.75<br>1 | | <br><br>%<br>% |
| B | Frequency response of audio amplifier (-3 dB) | $R_L$ = 16Ω $C_{10}$ = 120 pF<br>$C_{12}$ = 470 pF $P_1$ = 22 kΩ<br>$R_f$ = 82Ω<br>$R_f$ = 47Ω | | <br><br>70 to 12 000<br>70 to 7 000 | | <br><br>Hz<br>Hz |
| $V_o$ | Recovered audio voltage (PIN. 12) | $V_i$ ⩾ 1 mV $f_o$ = 4.5 MHz<br>$f_m$ = 400 Hz $\Delta f$ = ±7.5 kHz<br>$P_1$ = 0 | | <br><br>120 | | <br><br>mV |
| AMR | Amplitude modulation rejection | $V_i$ ⩾ 1 mV $f_o$ = 4.5 MHz<br>$f_m$ = 400 Hz $\Delta f$ = ±25 kHz<br>m = 0.3 | | <br><br>55 | | <br><br>dB |
| $\frac{S+N}{N}$ | Signal to noise ratio | $V_i$ ⩾ 1 mV $V_o$ = 4 V<br>$f_o$ = 4.5 MHz $f_m$ = 400 Hz<br>$\Delta f$ = ±25 kHz | <br><br>50 | <br><br>65 | | <br><br>dB |
| $R_f$ | External feedback resistance (between pins 7 and 9) | | | | 25 | kΩ |
| $R_i$ | Input resistance (pin 1) | $V_i$ = 1 mV<br>$f_o$ = 4.5 MHz | | 30 | | kΩ |
| $C_i$ | Input capacitance (pin 1) | | | 5 | | pF |
| SVR | Supply voltage rejection | $R_L$ = 16Ω<br>$f_{ripple}$ = 120 Hz<br>$P_1$ = 22 kΩ | | <br><br>46 | | <br><br>dB |
| A | DC volume control attenuation | $P_1$ = 12 kΩ | | 90 | | dB |

Fig. 1 - Relative audio output voltage and output noise vs. input signal

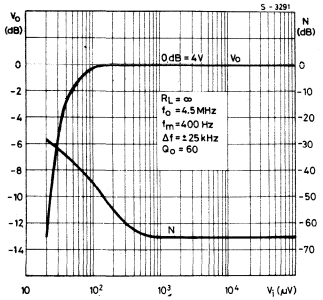



Fig. 2 - Output voltage attenuation vs. DC volume control resistance

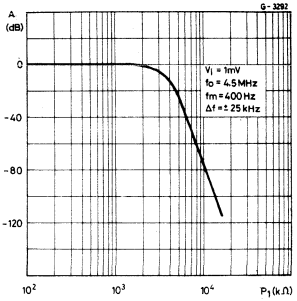



Fig. 3 - Amplitude modulation rejection vs. input signal

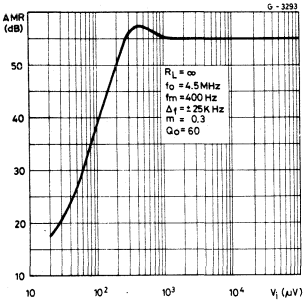



Fig. 4 - ΔAMR vs. tuning frequency change

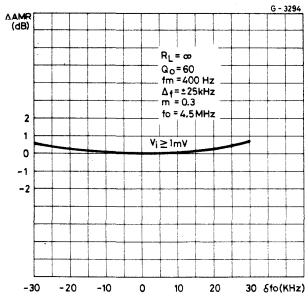



Fig. 5 - Recovered audio voltage vs. unloaded Q factor of the detector coil

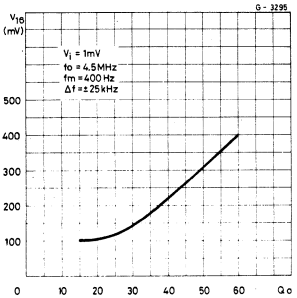



Fig. 6 - Distortion vs. output power

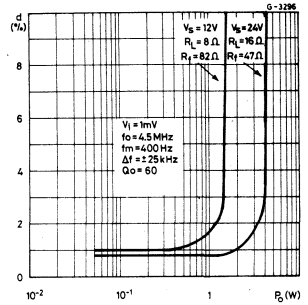



Fig. 7 - Distortion vs. frequency deviation

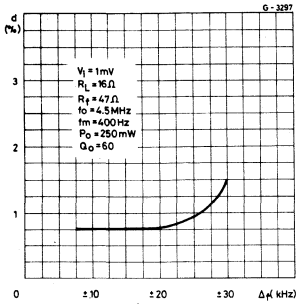



Fig. 8 - Distortion vs. tuning frequency change

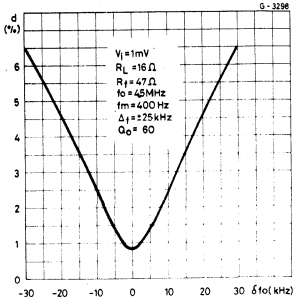



Fig. 9 - Audio amplifier frequency response

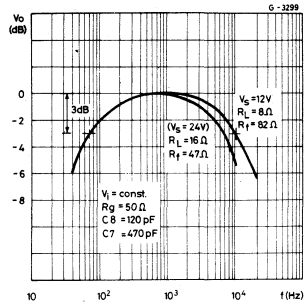


Fig. 10 - Supply voltage ripple rejection vs. ripple frequency

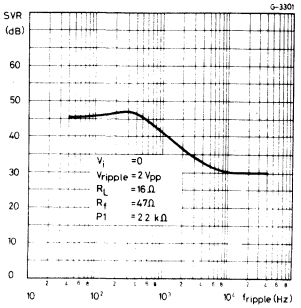



Fig. 11 - Supply voltage ripple rejection vs. volume control attenuation

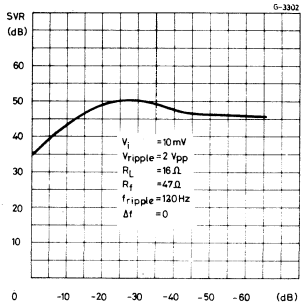



Fig. 12 - Output power vs. supply voltage

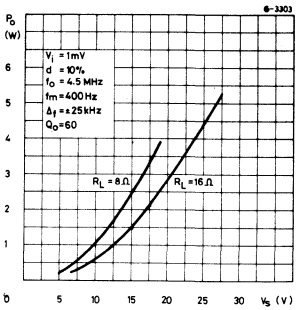



Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

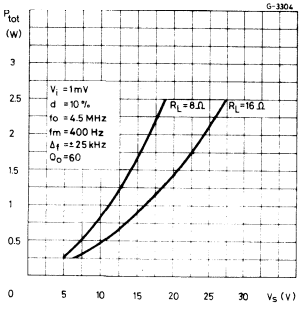



Fig. 14 - Power dissipation and efficiency vs. output power

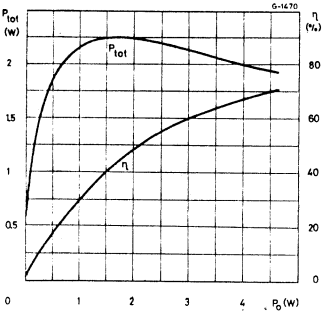
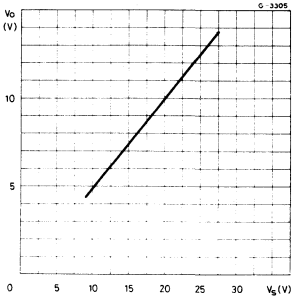



Fig. 15 - Quiescent output voltage (pin 9) vs. supply voltage




## APPLICATION INFORMATION

The electrical characteristics of the TDA 1190Z remain almost constant over the frequency range of 4.5 to 6 MHz, therefore it can be used in all television standard (FM mod.). The TDA 1190Z has a high input impedance, so it can function with a ceramic filter or with a tuned circuit that provide the necessary input selectivity.

The value of the resistors connected to pin 7, determine the AC gain of the audio frequency amplifier. This enables the desired gain to be selected in relation to the frequency deviation at which the output stage of the AF amplifier must enter into clipping.

The capacitor connected between pins 9 and 8 determines the upper cut-off frequency of the audio band. If larger bandwidth is required $C_{10}$, $C_{12}$ must be reduced keeping $C_{12}/C_{10}$ as in Fig. 16.

The capacitor connected between pin 12 and ground, toghether with the internal resistor of 10 KΩ, forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by inductive load and the wires connecting the loudspeaker.

## APPLICATION INFORMATION (continued)

Fig. 16 - Typical application circuit

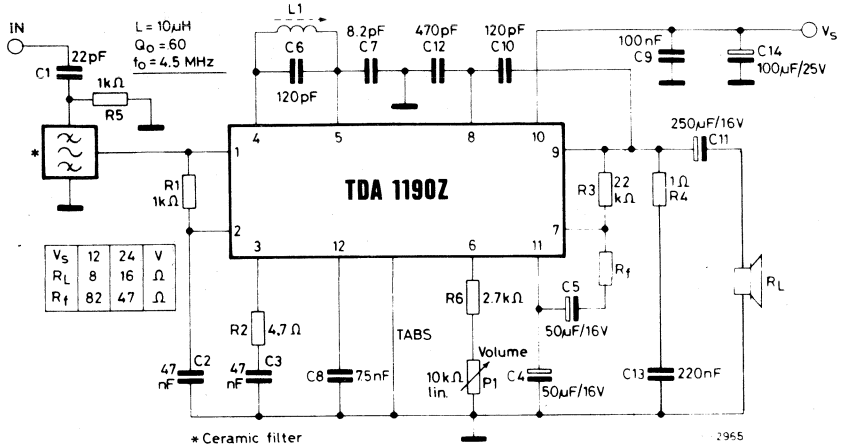
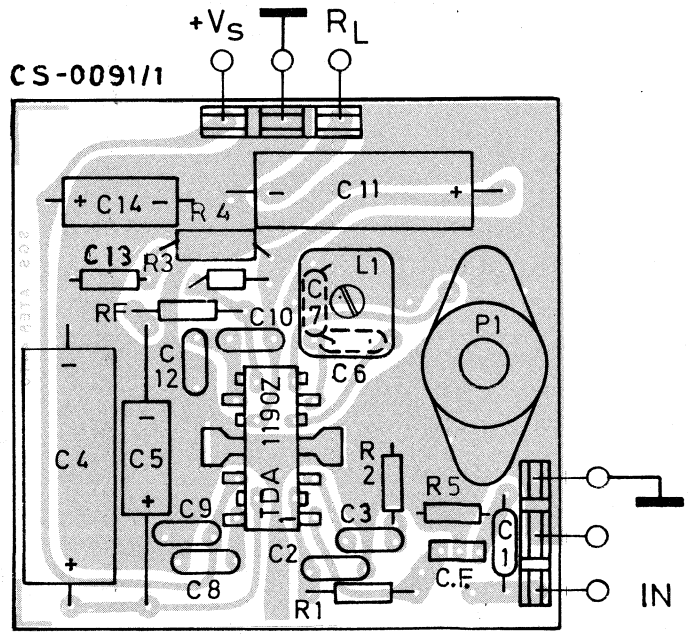



Fig. 17 - P.C. board and component layout of the circuit shown in Fig. 16



## MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA 1190Z can be reduced by soldering the tabs to a suitable copper area of the printed circuit board (Fig. 18) or to an external heatsink (Fig. 19).
The diagram of figure 20 shows the maximum dissipable power $P_{tot}$ and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 18 - Example of P.C. board copper area which is used as heatinsk

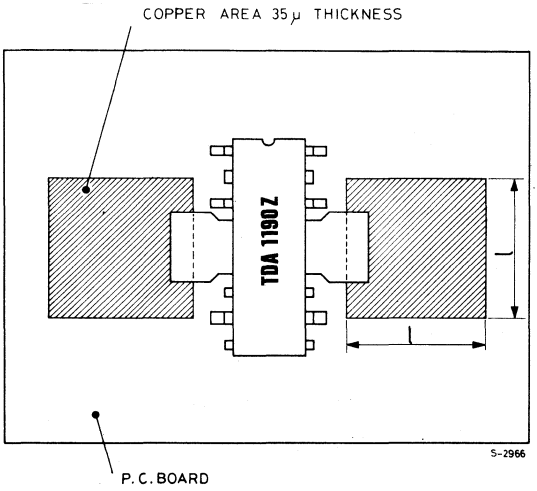



Fig. 19 - External heatsink mounting example

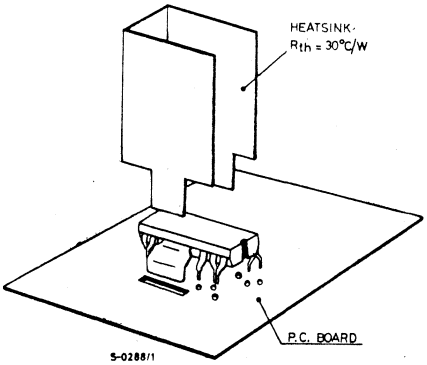



Fig. 20 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

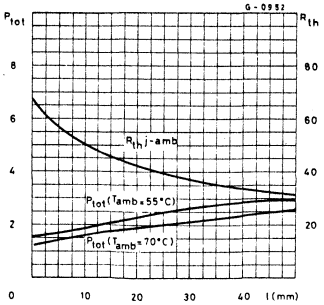
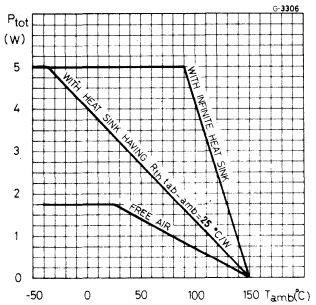



Fig. 21 - Maximum allowable power dissipation vs. ambient temperature



# LINEAR INTEGRATED CIRCUITS

**TDA1220A**

**NOT FOR NEW DESIGN**

## AM-FM RADIO

The TDA 1220A is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed for use in portable and home AM-FM radio sets.
The functions incorporated are:

**AM SECTION**
- Preamplifier and double balanced mixer
- Local oscillator
- IF amplifier with internal AGC
- Balanced detector
- AF preamplifier

**FM SECTION**
- IF amplifier
- Quadrature detector
- AF preamplifier

The TDA 1220A is suitable for all AM and FM broadcasting bands and it features:

- Very low noise
- High sensitivity
- Wide supply voltage range (3 to 16V)
- Low quiescent current (9 mA)
- Very simple DC switching of AM-FM sections

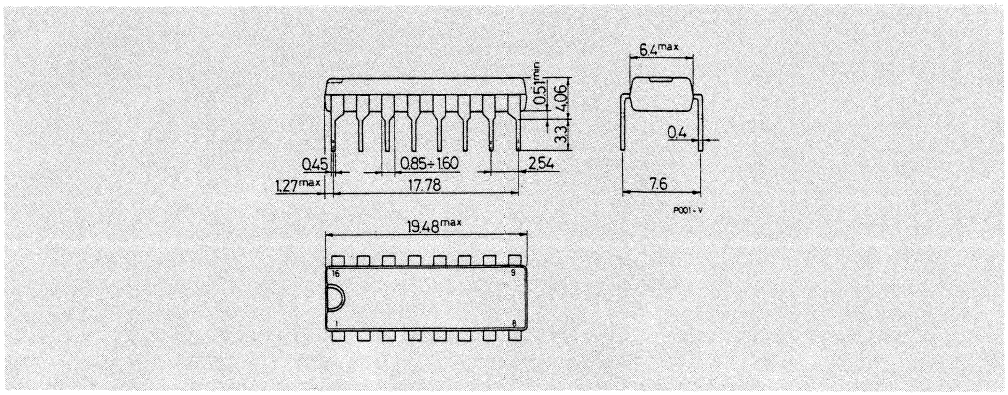
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 16 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 110\,°C$ | 400 | mW |
| $T_{op}$ | Operating temperature | -20 to 85 | °C |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -55 to 150 | °C |

**ORDERING NUMBER:** TDA 1220A

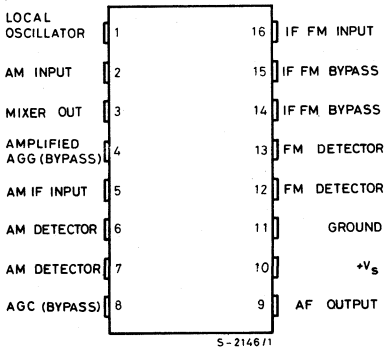
## MECHANICAL DATA

Dimensions in mm

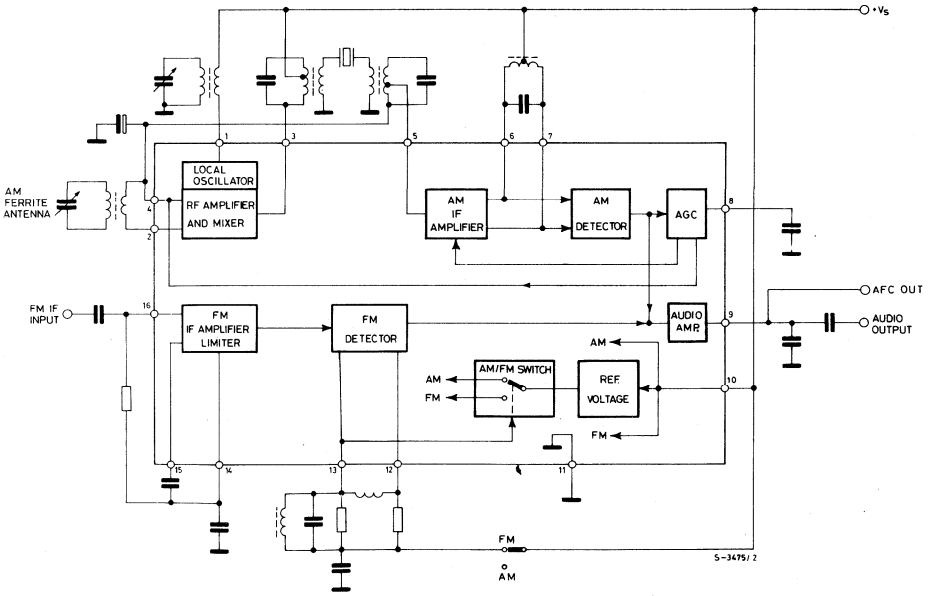


# TDA1220A

## CONNECTION DIAGRAM (top view)




## BLOCK DIAGRAM




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$= 25°C, $V_s$ = 9V unless otherwise specified, refer to test circuit)

| Parameter | | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $V_s$ | Supply Voltage | | 3 | | 16 | V |
| $I_d$ | Drain current | AM section | | 9 | 15 | mA |
| | | FM section | | 9 | 15 | |
| **AC CHARACTERISTICS** | | | | | | |
| **AM SECTION ($f_o$ = 1 MHz; $f_m$ = 1 KHz)** | | | | | | |
| $V_i$ | Input sensitivity | S/N = 26 dB m = 0.3 | | 12 | 25 | μV |
| S/N | Ultimate quieting | $V_i$ = 10 mV m = 0.3 | 50 | 60 | | dB |
| $\Delta V_i$ | AGC range | $\Delta V_{out}$= 10 dB m = 0.3 | 80 | | | dB |
| $V_o$ | Recovered audio signal (pin 9) | $V_i$ = 1 mV m = 0.3 | 40 | 80 | 160 | mV |
| d | Distortion | $V_i$ = 1 mV m = 0.8 | | 1 | 3 | % |
| d | Distortion | $V_i$ = 1 mV m = 0.3 | | 0.4 | 1 | % |
| $V_H$ | Max input signal handling capability | m = 0.8 d = 10% | | 80 | | mV |
| $R_i$ | Input resistance between pins 2 and 4 | m = 0 | | 7.5 | | KΩ |
| $C_i$ | Input capacitance between pins 2 and 4 | m = 0 | | 18 | | pF |
| $R_o$ | Output resistance (pin 9) | | | 7 | | KΩ |
| **FM SECTION ($f_o$ = 10.7 MHz; $f_m$ = 1 KHz)** | | | | | | |
| $V_i$ | Input limiting voltage | -3 dB limiting point | | | 36 | μV |
| AMR | Amplitude modulation rejection | Δf = ± 22.5 KHz $V_i$ = 3 mV | 35 | 48 | | dB |
| S/N | Ultimate quieting | Δf = ± 22.5 KHz $V_i$ = 1 mV | 55 | 70 | | dB |
| d | Distortion (single tuned) | Δf = ± 75 KHz $V_i$ = 1 mV | | 0.7 | 3 | % |
| d | Distortion (double tuned) | Δf = ± 22.5 KHz $V_i$ = 1 mV | | 0.2 | | |
| $V_o$ | Recovered audio signal (pin 9) | Δf = ± 22.5 KHz $V_i$ = 1 mV | 40 | 80 | 160 | mV |
| $R_i$ | Input resistance between pin 16 and ground | Δf = 0 | | 6.5 | | KΩ |
| $C_i$ | Input capacitance between pin 16 and ground | Δf = 0 | | 14 | | pF |
| $R_o$ | Output resistance (pin 9) | | | 7 | | KΩ |

## TEST CIRCUIT

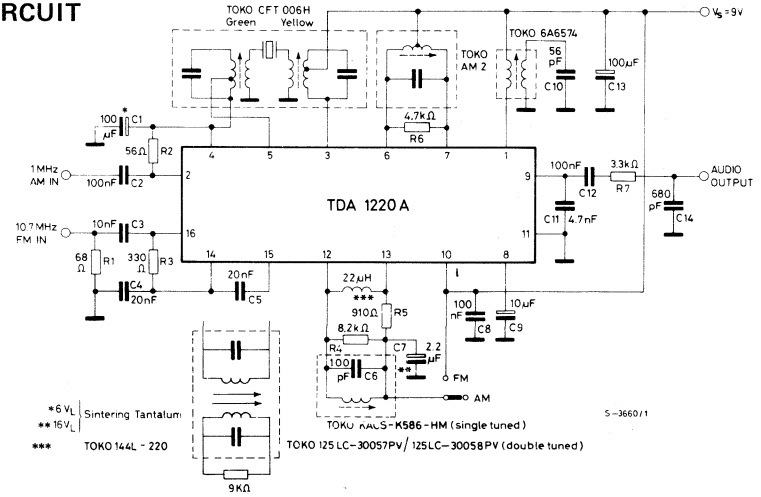



Fig. 1 - PC board and component layout (1 : 1 scale) of the test circuit

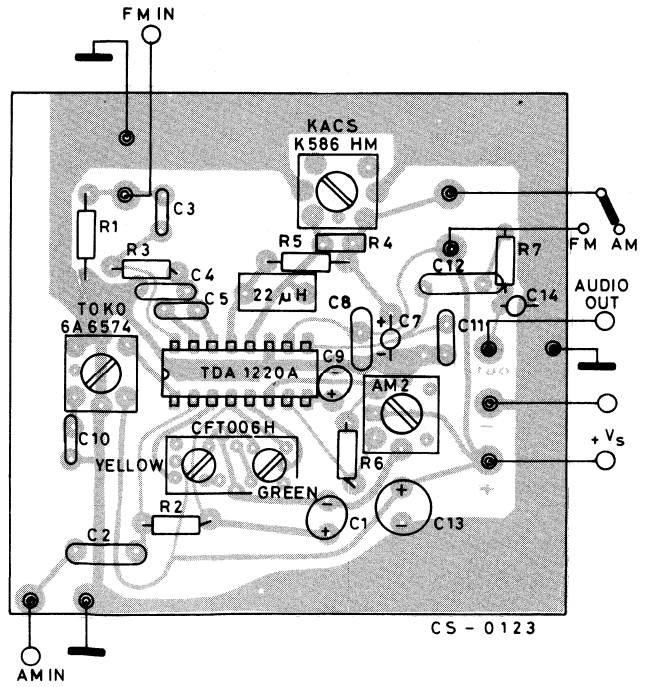


Fig. 2 - Audio output and signal to noise ratio vs. input signal (AM section)

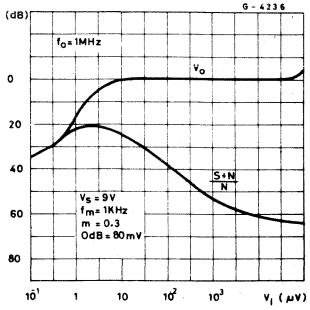



Fig. 3 - Audio output vs. supply voltage (AM section)

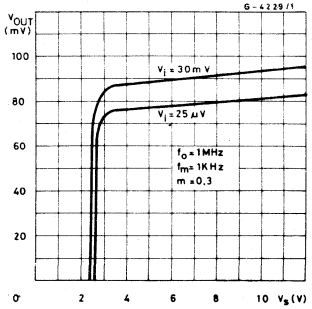



Fig. 4 - Distortion vs. input signal (AM section)

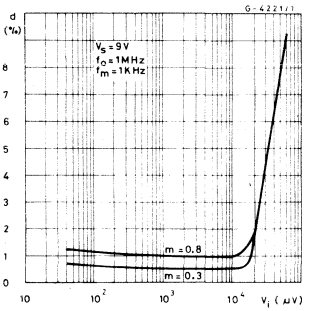



Fig. 5 - Audio output and signal to noise ratio vs. input signal (FM section)

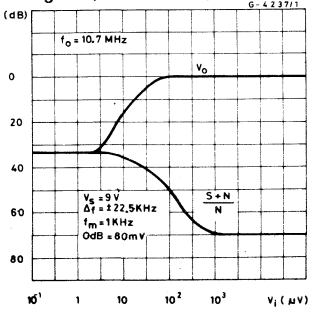



Fig. 6 - Audio output vs. supply voltage (FM section)

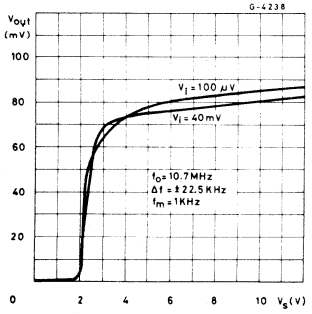



Fig. 7 - Amplitude modulation rejection vs. input signal (FM section)

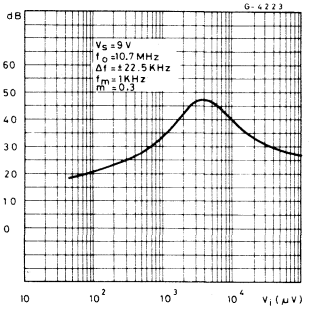



Fig. 8 - Δ DC voltage (pin 9) vs. ambient temperature (FM section)

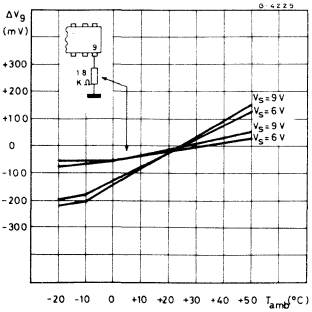



Fig. 9 -- DC output voltage (pin 9) vs. supply voltage (FM section)

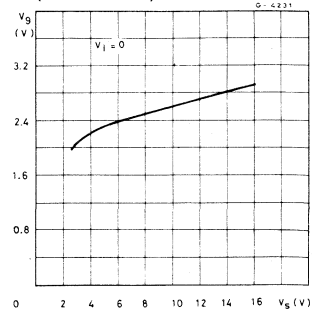
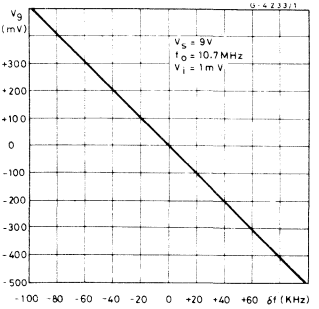



Fig. 10 - Δ DC output voltage (pin 9) vs. frequency shift (FM section)



## APPLICATION INFORMATION

### FM Section

#### IF Amplifier and limiter

The 10.7 MHz IF signal from the ceramic filter is amplified and limited by a chain of four differential stages.
Pin 16 is the amplifier input and has a typical input impedance of 6.5 KΩ in parallel with 14 pF at 10.7 MHz.
Bias for the first stage is available at pin 14 and provides 100% DC feedback for stable operating conditions. Pin 15 is the second input to the amplifier and is decoupled to pin 14, which is grounded by a 20 nF capacitor.
An RLC network is connected to the amplifier output and gives a 90° phase shift (at the IF centre frequency) between pins 13 and 12. The signal level at pin 13 is about 150 mV rms.

#### FM Detector

The circuit uses a quadrature detector and the choise of component values is determined by the acceptable level of distortion at a given recovered audio level.
With a double tuned network the linearity improves (distortion is reduced) and the phase shift can be optimized; however this leads to a reduction in the level of the recovered audio. A satisfactory compromise for most FM receiver applications is shown in the test circuit.

Care should be taken with the physical layout.
The main recommandations are:

- Locate the phase shift coil as near as possible to pin 13.
- Shunt pins 14 and 16 with a low value resistor (between 56Ω and 330Ω).
- Ground the decoupling capacitor of pin 14 and the 10.7 MHz input filter at the same point.

If the supply voltage goes under 6V add a DC level shift resistor of 18 KΩ from pin 9 to ground and change C11 to 8 nF.

### AM-FM Switching

AM-FM switching is achieved by applying a DC voltage at pin 13, to switch the internal reference.

**Typical DC Voltages (refer to the test circuit)**

| Pins | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AM | 9 | 1.3 | 9 | 1.3 | 1.3 | 9 | 9 | 0.7 | 2 | 9 | 0 | 0 | 0 | 8.4 | 8.4 | 8.4 | V |
| FM | 9 | 0.4 | 9 | 0.4 | 0 | 9 | 9 | 0 | 2.6 | 9 | 0 | 9 | 9 | 8.1 | 8.1 | 8.1 | V |

## APPLICATION INFORMATION (continued)

### AM Section

**RF Amplifier and mixer stages**

The RF amplifier stage (pin 2) is connected directly to the secondary winding of the ferrite rod antenna or input tuned circuit. Bias is provided at pin 4 which must be adequately decoupled. The RF amplifier provides stable performance extending beyond 30 MHz.
The Mixer employed is a double - balanced multiplier and the IF output at pin 3 is connected directly to the IF filter coil.

**Local oscillator**

The local oscillator is a cross coupled differential stage which oscillates as the frequency determined by the load on pin 1.
The oscillator resonant circuit is transformer coupled to pin 1 to improve the **Q** factor and frequency stability.
The oscillator level at pin 1 is about 100 mV rms and the performance extends beyond 30 MHz, however to enhance the stability and reduce to a minimum pulling effects of the AGC operation or supply voltage variations, a high C/L ratio should be used above 10 MHz.
An external oscillator can be injected at pin 1. The level should be 50 mV rms and pin 1 should be connected to the supply via a 100Ω resistor.

**IF Amplifier Detector**

The IF amplifier is a wide band amplifier with a tuned output stage.
The outputs are at pins 6 and 7 which drive the balanced load and the differential positive peak AM detector, which is biased to reduce distortion at high modulation levels. At the output of balanced detectors of this type there is a low level signal at double the IF frequency (about 920 KHz). To avoid feedback of this signal by radiation from the detector coil, the shield around this coil must be grounded and the ferrite antenna placed in a suitable position.
The Audio output is at pin 9 (for either AM or FM); the IF frequency is filtered by an external capacitor which is also used as the FM mono de-enphasis network. The audio output impedance is about 7 KΩ and a high impedance load (~ 50 KΩ) must be used.

**AGC**

Both the RF and the first IF amplifiers have the same differential amplifier circuit configuration. The AGC action is obtained by control of the collector current of these stages.
At pin 8 there is a carrier envelope signal which is filtered by an external capacitor to remove the Audio and RF content and obtain a mean DC signal to drive the AGC circuit.

## APPLICATION INFORMATION (continued)

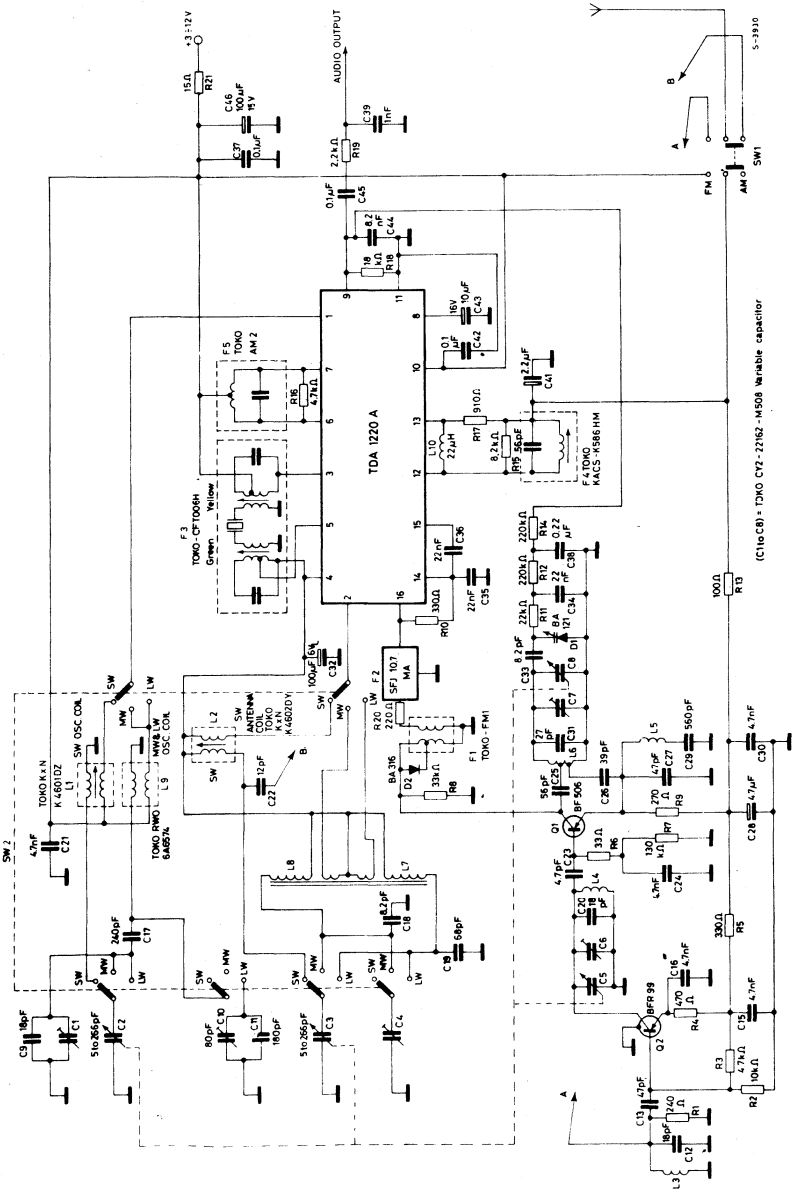
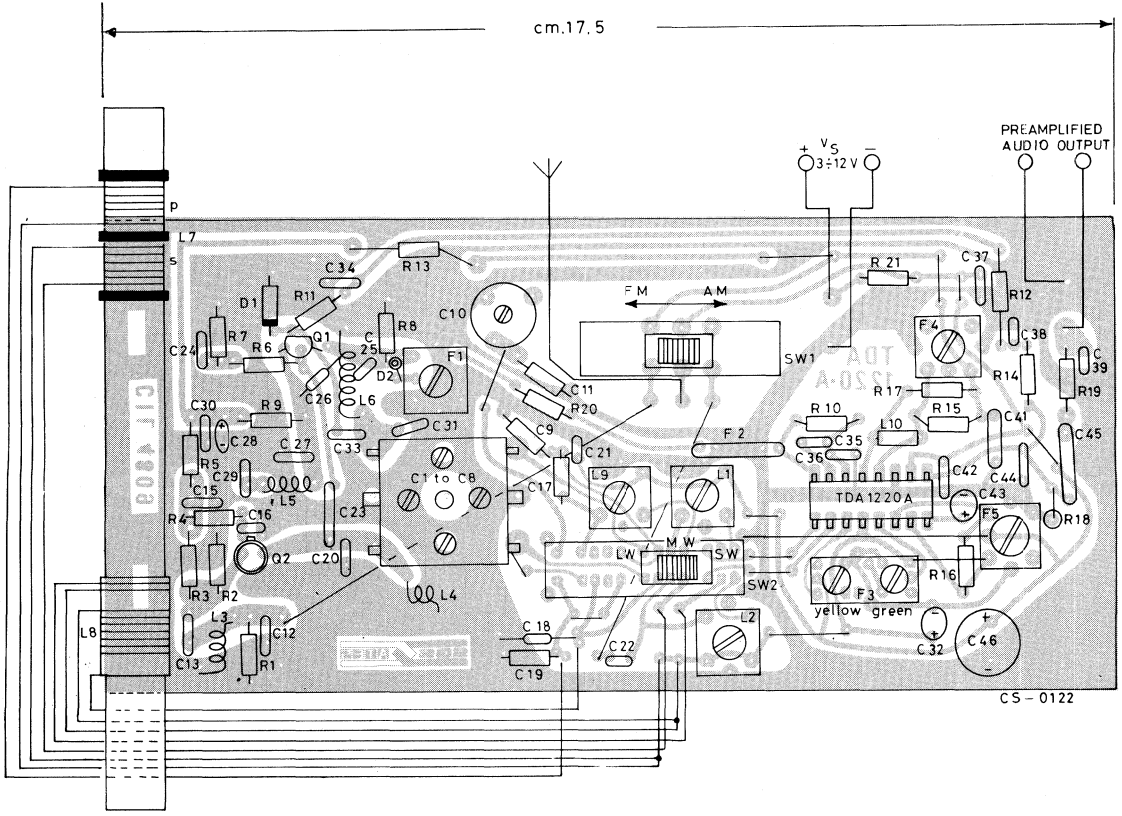



Fig. 11 - LW - MW - SW - FM - radio

**L3 FM Antenna Coil** - 6 Turns copper wire 0.9 mm diameter. Inner diameter 4 mm - winding pitch 1 m.
**L4 FM Tuning Coil** - 5 Turns copper wire 0.9 mm diameter. Inner diameter 4 mm - winding pitch 0.5 mm.
**L5** - 18 Turns copper wire 0.6 mm. diameter. Inner diameter 2.5 mm. Closely wound.
**L6 FM oscillator Coil** - 4 Turns silvered copper wire 1 mm. diameter. ,nner diameter 4 mm. - winding pitch 2.5 mm.
**L7** - LW antenna coil - Televox.
**L8** - MW antenna coil - Televox.
**SW3** - ALPS type SSA 0.63.

## APPLICATION INFORMATION (continued)

Fig. 12 - PC board and component layout of the four band radio (fig. 11)

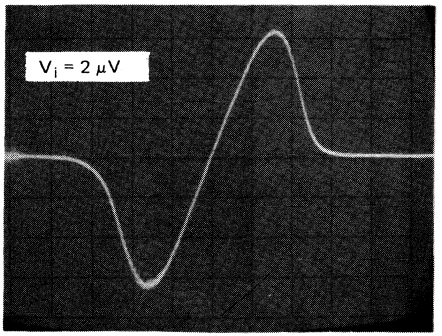


## APPLICATION INFORMATION (continued)

### FOUR BAND RADIO PERFORMANCE

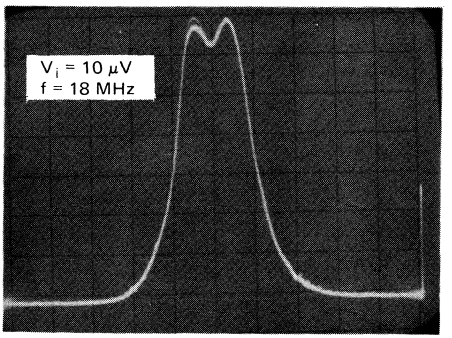
| Parameter | Test conditions | Values |
|---|---|---|
| **AM SECTION (*)** | | |
| $\lvert\frac{S+N}{N}\rvert$ | $V_i$ = 10 μV m = 0.3 | 26 dB |
| | $V_i$ = 1 mV m = 0.3 | 55 dB |
| BW | -3 dB | 10 KHz |
| Distortion | $V_i$ = 20 μV m = 0.3 | 0.5 % |
| | $V_i$ = 100 μV m = 0.3 | 0.5 % |
| | $V_i$ = 1 mV m = 0.3 | 0.5 % |
| | $V_i$ = 20 μV m = 0.8 | 0.9 % |
| | $V_i$ = 1 mV m = 0.8 | 1 % |
| **FM SECTION** | | |
| AMR | $V_i$ = 30 μV Δf = 22.5 KHz m = 0.3 $f_m$ = 1 KHz | 45 dB |
| | $V_i$ = 100 μV Δf = 22.5 KHz m = 0.3 $f_m$ = 1 KHz | 47 dB |
| Distortion | $V_i$ = 10 μV Δf = 22.5 KHz | 0.3 % |
| | $V_i$ = 100 μV Δf = 22.5 KHz | 0.2 % |
| | $V_i$ = 1 mV Δf = 22.5 KHz | 0.2 % |
| | $V_i$ = 10 μV Δf = 75 KHz | 1 % |
| | $V_i$ = 100 μV Δf = 75 KHz | 1 % |
| $\lvert\frac{S+N}{N}\rvert$ | $V_i$ = 10 μV Δf = 22.5 KHz | 60 dB |
| | $V_i$ = 100 μV Δf = 22.5 KHz | 70 dB |
| | $V_i$ = 1 mV Δf = 22.5 KHz | 70 dB |
| Input limiting voltage | -3 dB | 1 μV |

(*) The performance remains substantially the same over LW, MW and SW bands.




100 KHz/div.

Fig. 13 - FM-SECTION
S curve response




5 KHz/div.

Fig. 14 - AM-SECTION
Band pass IF filter response at AGC starting point.

# LINEAR INTEGRATED CIRCUITS

**TDA1220B**

**PRELIMINARY DATA**

## AM-FM QUALITY RADIO

The TDA 1220B is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed as an improved version of the TDA 1220A.
It is intended for quality receivers produced in large quantities.
The functions incorporated are:

**AM SECTION**
- Preamplifier and double balanced mixer (1)
- One pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

**FM SECTION**
- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier

The TDA 1220B is suitable up to 30 MHz (*) AM and for FM bands (including 450 KHz narrow band) and features:

- Very constant characteristics (3V to 16V)
- High sensitivity and low noise
- Very low tweet
- Very high signal handling (1V)
- Sensitivity regulation facility (**)
- High recovered audio signal suited for stereo decoders and radio recorders
- Very simple DC switching of AM-FM
- Low current drain
- AFC facility

(1) Patent pending.
* Up to 50 MHz with external cristal oscillator.
** Maximum AM sensitivity can be reduced by mean of a resistor (5 to 12 KΩ) between pin 4 and ground.

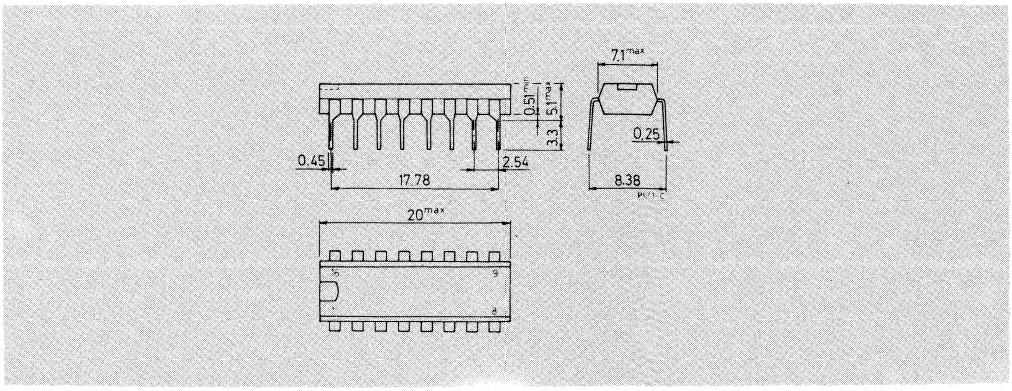
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 16 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb} < 110°C$ | 400 | mW |
| $T_{op}$ | Operating temperature | −20 to 85 | °C |
| $T_{stg}$, $T_j$ | Storage and junction temperature | −55 to 150 | °C |

**ORDERING NUMBER:** TDA 1220BK

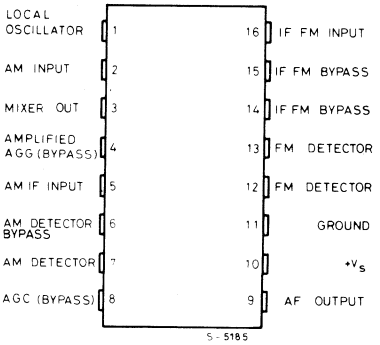
## MECHANICAL DATA

Dimensions in mm

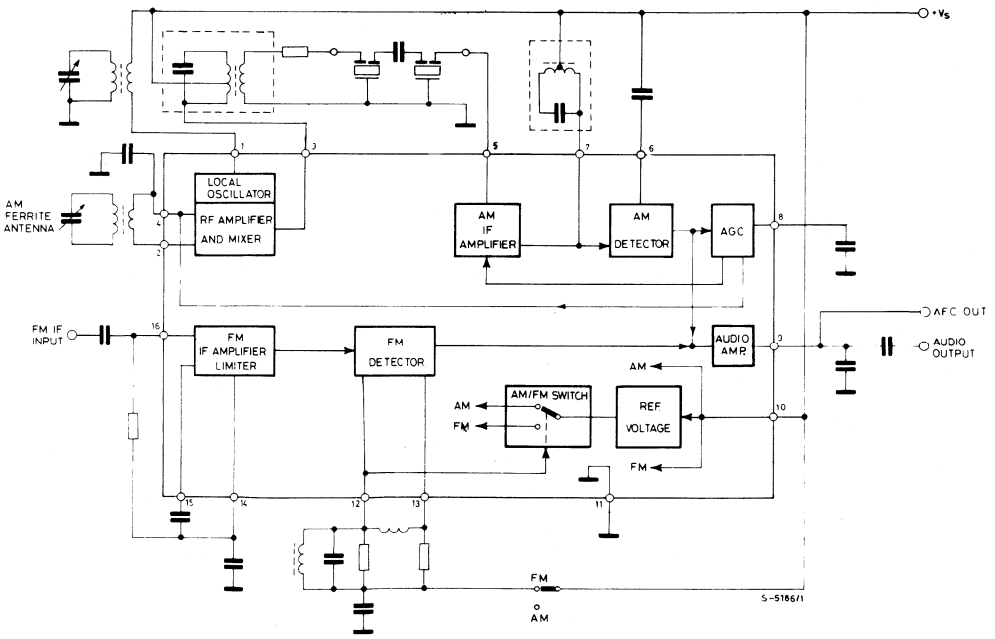


# TDA1220B

## CONNECTION DIAGRAM




## BLOCK DIAGRAM



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $V_s$ = 9V unless otherwise specified, refer to test circuit)

| Parameter | | Test conditions | | Min. | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | 3 | | 16 | V |
| $I_d$ | Drain current | | | | 10 | 15 | mA |
| **AM SECTION** ($f_o$ = 1 MHz; $f_m$ = KHz) | | | | | | | |
| $V_i$ | Input sensitivity | S/N = 26 dB | m = 0.3 | | 12 | 25 | μV |
| S/N | | $V_i$ = 10 mV | m = 0.3 | 45 | 52 | | dB |
| $V_i$ | AGC range | $\Delta V_{out}$ = 10 dB | m = 0.8 | 94 | 100 | | dB |
| $V_o$ | Recovered audio signal (pin 9) | $V_i$ = 1 mV | m = 0.3 | 80 | 130 | 190 | mV |
| d | Distortion | $V_i$ = 1 mV | m = 0.3 | | 0.4 | 1 | % |
| | | | m = 0.8 | | 1.2 | | % |
| $V_H$ | Max input signal handling capability | m = 0.8 | d < 10% | 1 | | | V |
| $R_i$ | Input resistance between pins 2 and 4 | m = 0 | | | 7.5 | | KΩ |
| $C_i$ | Input capacitance between pins 2 and 4 | m = 0 | | | 18 | | pF |
| $R_o$ | Output resistance (pin 9) | | | 4.5 | 7 | 9.5 | KΩ |
| | Tweet 2 IF | m = 0.3 | $V_i$ = 1 mV | | 40 | | dB |
| | Tweet 3 IF | | | | 55 | | dB |
| **FM SECTION** ($f_o$ = 10.7 MHz; $f_m$ = 1 KHz) | | | | | | | |
| $V_i$ | Input limiting voltage | -3 dB limiting point | | | 22 | 36 | μV |
| AMR | Amplitude modulation rejection | $\Delta f = \pm 22.5$ KHz<br>$V_i$ = 3 mV | m = 0.3 | 40 | 50 | | dB |
| S/N | Ultimate quieting | $\Delta f = \pm 22.5$ KHz | $V_i$ = 1 mV | 55 | 65 | | dB |
| d | Distortion | $\Delta f = \pm 75$ KHz | $V_i$ = 1 mV | | 0.7 | 1.5 | % |
| d | Distortion | $\Delta f = \pm 22.5$ KHz | $V_i$ = 1 mV | | 0.25 | 0.5 | % |
| d | Distortion (double tuned) | | | | 0.1 | | % |
| $V_o$ | Recovered audio signal (pin 9) | $\Delta f = \pm 22.5$ KHz | $V_i$ = 1 mV | 80 | 110 | 140 | mV |
| $R_i$ | Input resistance between pin 16 and ground | | | | 6.5 | | KΩ |
| $C_i$ | Input capacitance between pin 16 and ground | | | | 14 | | pF |
| $R_o$ | Output resistance (pin 9) | | | 4.5 | 7 | 9.5 | KΩ |

Fig. 1 - Test circuit

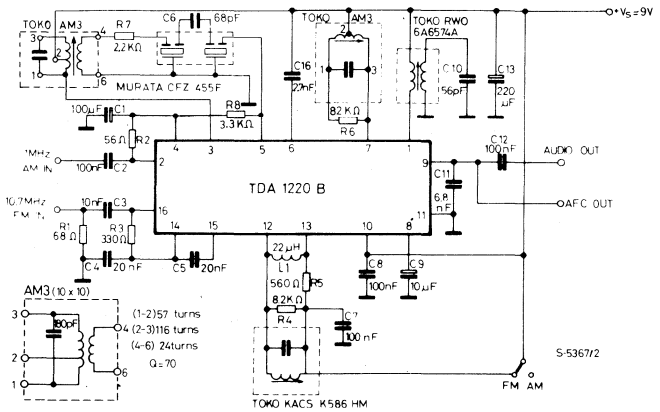



Fig. 2 - PC board and component layout (1:1 scale) of the test circuit.

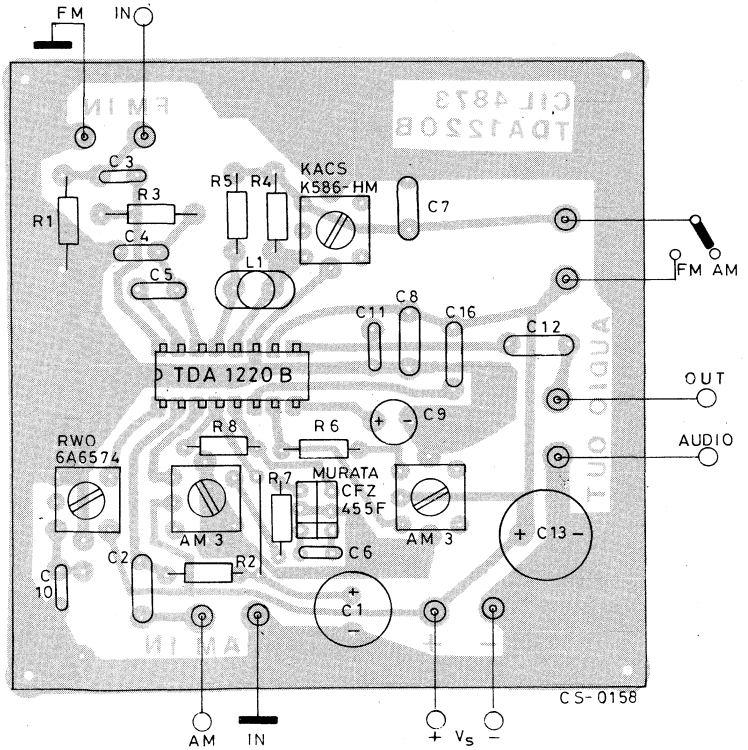


Fig. 3 - Audio output, noise and tweet levels vs. input signal (AM section)

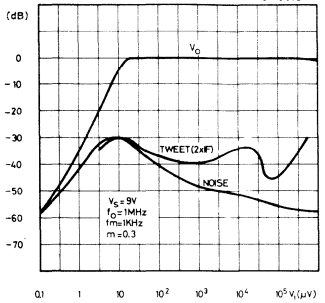



Fig. 4 - Distortion vs input signal and modulation index (AM section)

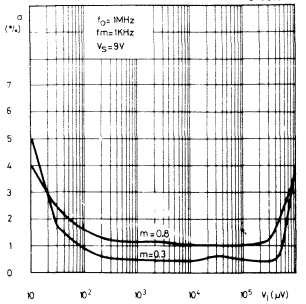



Fig. 5 - Audio output vs. supply voltage (AM section)

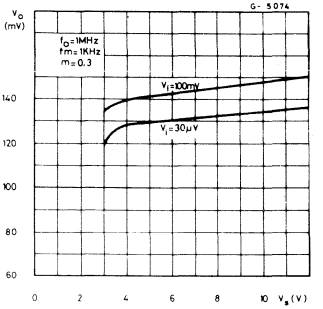



Fig. 6 - Audio output and noise level vs. input signal (FM section)

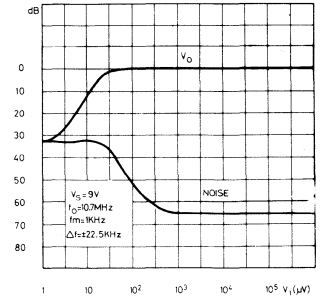



Fig. 7 - Distortion vs. input signal (FM section)

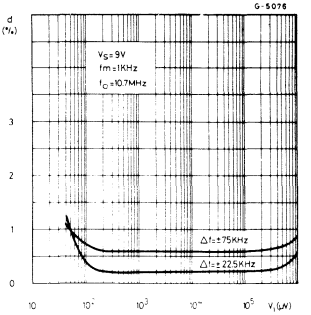



Fig. 8 - Audio output vs. supply voltage (FM section)

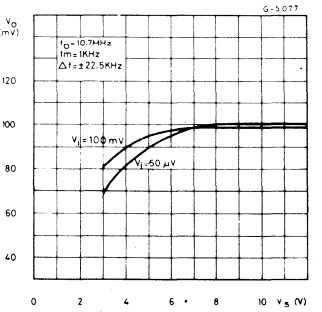



Fig. 9 - Amplitude modulation rejection vs. input signal (FM section)

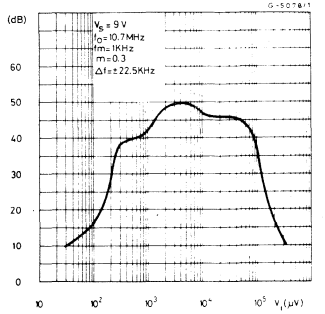



Fig. 10 - ΔDC output voltage (pin. 9) vs. frequency shift (FM section)

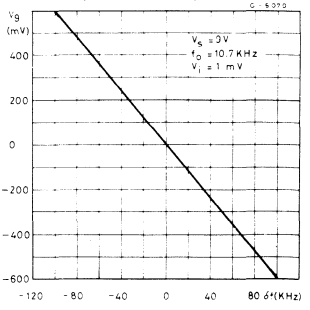
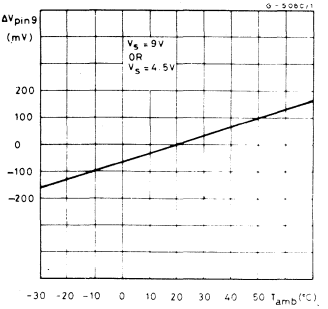



Fig. 11 - ΔDC output voltage (pin 9) vs. ambient tempetature (FM section)



## APPLICATION INFORMATION

### AM Section

#### RF Amplifier and mixer stages

The RF amplifier stage (pin 2) is connected directly to the secondary winding of the ferrite rod antenna or input tuned circuit. Bias is provided at pin 4 which must be adequately decoupled. The RF amplifier provides stable performance extending beyond 30 MHz.
The Mixer employed is a double - balanced multiplier and the IF output at pin 3 is connected directly to the IF filter coil.

#### Local oscillator

The local oscillator is a cross coupled differential stage which oscillates at the frequency determined by the load on pin 1.
The oscillator resonant circuit is transformer coupled to pin 1 to improve the **Q** factor and frequency stability.
The oscillator level at pin 1 is about 100 mV rms and the performance extends beyond 30 MHz, however to enhance the stability and reduce to a minimum pulling effects of the AGC operation or supply voltage variations, a high C/L ratio should be used above 10 MHz.
An external oscillator can be injected at pin 1. The level should be 50 mV rms and pin 1 should be connected to the supply via a 100Ω resistor.

#### IF Amplifier Detector

The IF amplifier is a wide band amplifier with a tuned output stage.
The IF filters can be either LC or mixed LC/ceramic.
AM detection occurs at pin 7. A detection capacitor is connected to pin 6 to reduce the radiation of spurious detector products.
The Audio output is at pin 9 (for either AM or FM); the IF frequency is filtered by an external capacitor which is also used as the FM mono de-enphasis network. The audio output impedance is about 7 KΩ and a high impedance load (~ 50KΩ) must be used.

#### AGC

Automatic gain control operates in two ways.
With weak signals it acts on the IF gain, maintaining the maximum S/N. For strong signals a second circuit intervenes which controls the entire chain and allows signal handling in excess of one volt (m = 0.8).
At pin 8 there is a carrier envelope signal which is filtered by an external capacitor to remove the Audio and RF content and obtain a mean DC signal to drive the AGC circuit.

## APPLICATION INFORMATION (continued)

### FM Section

#### IF Amplifier and limiter

The 10.7 MHz IF signal from the ceramic filter is amplified and limited by a chain of four differential stages.
Pin 16 is the amplifier input and has a typical input impedance of 6.5 KΩ in parallel with 14 pF at 10.7 MHz.
Bias for the first stage is available at pin 14 and provides 100% DC feedback for stable operating conditions. Pin 15 is the second input to the amplifier and is decoupled to pin 14, which is grounded by a 20 nF capacitor.
An RLC network is connected to the amplifier output and gives a 90° phase shift (at the IF centre frequency) between pins 13 and 12. The signal level at pin 13 is about 150 mV rms.

#### FM Detector

The circuit uses a quadrature detector and the choise of component values is determined by the acceptable level of distortion at a given recovered audio level.
With a double tuned network the linearity improves (distortion is reduced) and the phase shift can be optimized; however this leads to a reduction in the level of the recovered audio. A satisfactory compromise for most FM receiver applications is shown in the test circuit.

Care should be taken with the physical layout.
The main recommandations are:

- Locate the phase shift coil as near as possible to pin 13.
- Shunt pins 14 and 16 with a low value resistor (between 56Ω and 330Ω).
- Ground the decoupling capacitor of pin 14 and the 10.7 MHz input filter at the same point.

### AM-FM Switching

AM-FM switching is achieved by applying a DC voltage at pin 13, to switch the internal reference.

**Typical DC voltages (refer to the test circuit)**

| Pins | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AM | 9 | 1.4 | 9 | 1.4 | 1.4 | 8.4 | 9 | 0.7 | 1.9 | 9 | 0 | 0.1 | 0.1 | 8.5 | 8.5 | 8.5 | V |
| FM | 9 | 0.02 | 9 | 0.02 | 0.02 | 8.5 | 9 | 0 | 1.7 | 9 | 0 | 9 | 9 | 8 | 8 | 8 | V |

## APPLICATION SUGGESTION

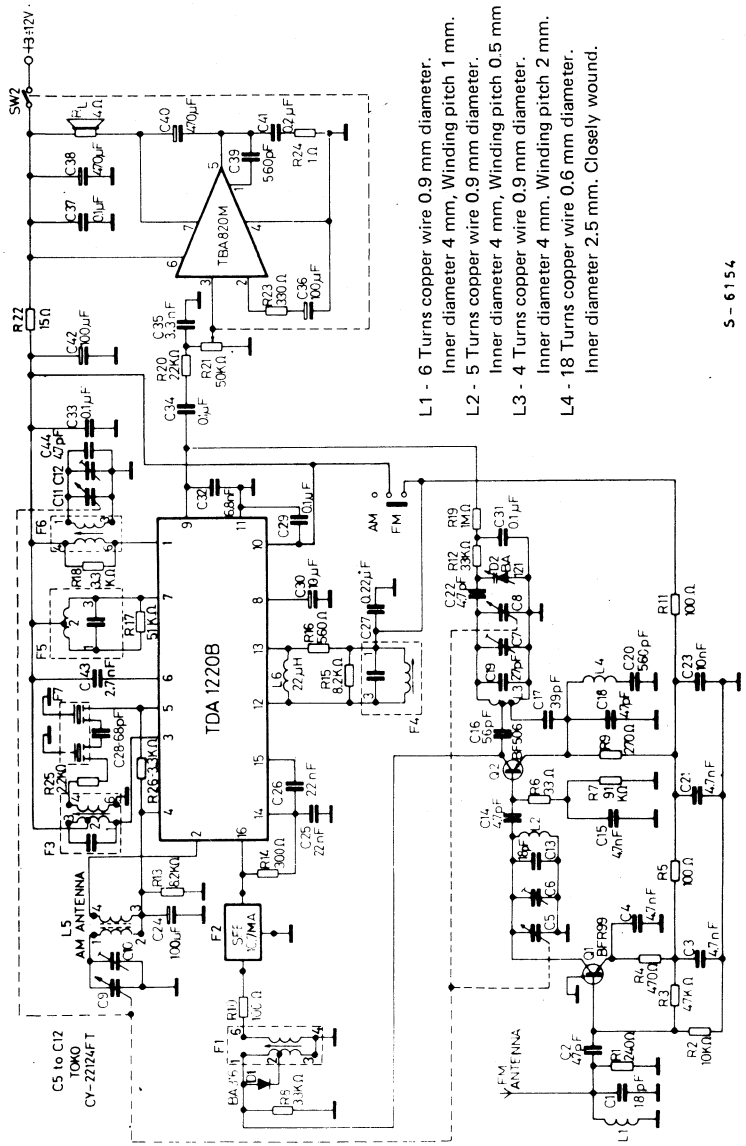
Reccomended values are referred to the test circuit of Fig. 2

| Part number | Recommended value | Purpose | Smaller than recommended value | Larger than recommended value |
|---|---|---|---|---|
| C1 | 100 μF | AGC bypass | Increase of the distortion at low audio frequency | Increase of the AGC time constant |
| C2 (*) | 100 nF | AM input DC cut | | |
| C3 (*) | 10 nF | FM input DC cut | | |
| C4<br>C5 | 20 nF<br>20 nF | FM amplifier bypass | Reduction of sensitivity | – Bandwidth increase<br>– Higher noise |
| C6 | 68 pF | Ceramic filter coupling | IF bandwidth reduction | IF bandwidth increase |
| C7 | 100 nF | FM detector decoupling | Danger of RF irradiation | |
| C8 | 100 nF | Power supply bypass | Noise increase of the audio output | |
| C9 | 10 μF | AGC bypass | Increase of the distortion at low audio frequency | Increase of the AGC time constant |
| C10 (*) | 56 pF | Tuning of the AM oscillator at 1455 KHz | | |
| C11 | 6.8 nF | 50 μs FM de-enphasis | | |
| C12 | 100 nF | Output DC decoupling | Low audio frequency cut | |
| C13 | 220 μF | Power supply decoupling | Increase of the distortion at low frequency | |
| C16 | 2.7 nF | AM detector capacitor | Low suppression of the IF frequency and harmonics | Increase of the audio distortion |
| R1 (*) | 68 ohm | FM input matching | | |
| R2 (*) | 56 ohm | AM input matching | | |
| R3 | 330 ohm | Ceramic filter matching | | |
| R4 | 8.2 Kohm | FM detector coil Q setting | Audio output decrease and lower distortion | Audio output increase and higher distortion |
| R5 | 560 ohm | FM detector load resistor | Audio output decrease and higher AMR | |
| R6 | 82 Kohm | AM detector coil Q setting | Lower IF gain and Lower AGC range | Higher IF gain and lower AGC range |
| R7 | 2.2 Kohm | 455 KHz IF filter matching | | |
| R8 | 3.3 Kohm | 455 KHz IF filter matching | | |

(*) Only for test circuit

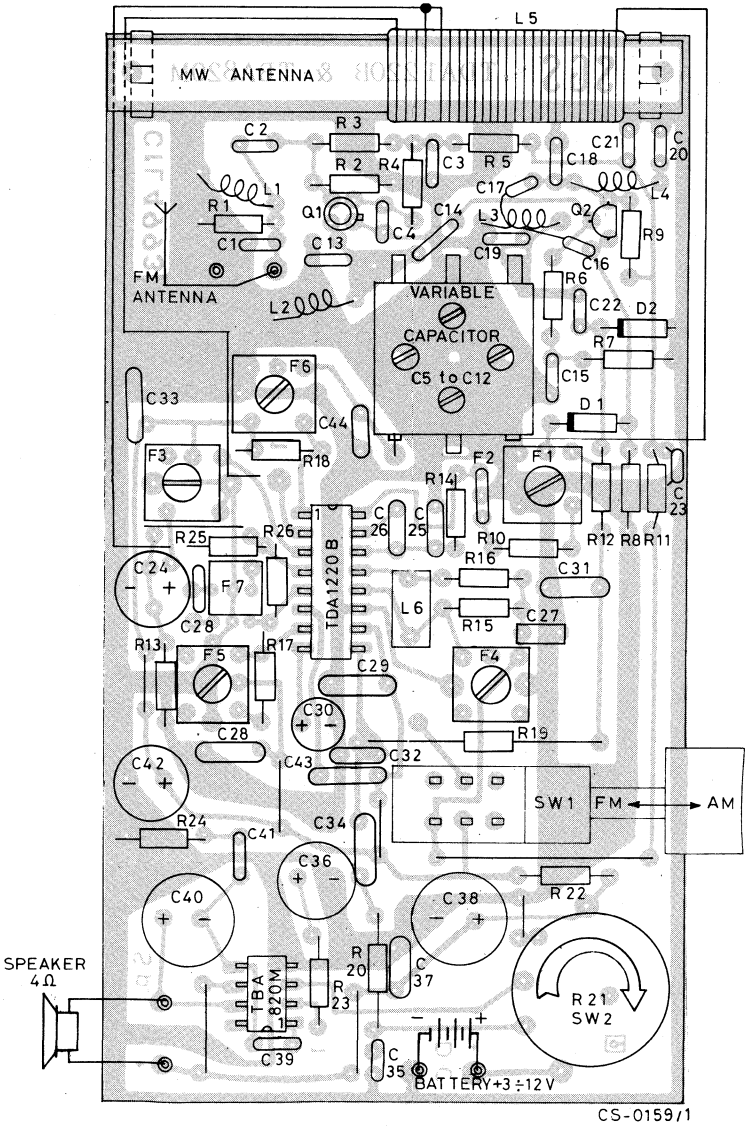
## APPLICATION INFORMATION (continued)

Fig. 12 - Portable AM/FM radio



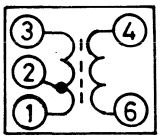
## APPLICATION INFORMATION (continued)

Fig. 13 - PC board and component layout of the fig. 12 1:1 scale



## APPLICATION INFORMATION (continued)

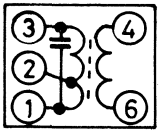
### F1 – 10.7 MHz IF Coil




| $C_o$ (pF) | f (MHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| – | | 1-3 | 1-2 | 2-3 | 4-6 |
| – | 10.7 | 110 | 6 | 8 | 2 |

TOKO - FM1 - 10x10 mm.
154 AN - 7A5965R

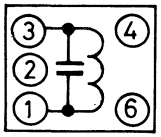
### F3 and F5 - 455 KHz IF Coil




| $C_o$ (pF) | f (kHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| 1-3 | | 1-3 | 1-2 | 2-3 | 4-6 |
| 180 | 455 | 70 | 57 | 116 | 24 |

TOKO - AM3 - 10x10 mm.
RLC - 4A7525N

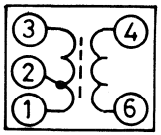
### F4 – FM Detector Coil




| $C_o$ (pF) | f (MHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| 1-3 | | 1-3 | 1-3 | – | – |
| 82 | 10.7 | 100 | 12 | – | – |

TOKO - 10x10 mm.
KACS - K586 HM

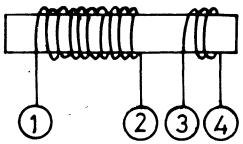
### F6 – AM Oscillator Coil




| f (kHz) | L (μH) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| | 1-3 | 1-3 | 1-2 | 2-3 | 4-6 |
| 796 | 220 | 80 | 2 | 75 | 8 |

TOKO -10x10 mm
RWO + 6A6574N

### L5 – Antenna Coil




S-6161

| f (KHz) | L (μH) | $Q_o$ | TURNS | |
|---|---|---|---|---|
| | 1-2 | 1-2 | 1-2 | 3-4 |
| 796 | | | 105 | 7 |

WIRE: LITZ - 15x0.05 mm.
CORE: 10x80 mm.

## APPLICATION INFORMATION (continued)

Typical performance of the radio receiver of fig.12 ($V_s$ = 9V)

| Parameter | | Test Conditions | | Value |
|---|---|---|---|---|
| WAVEBANDS | FM | | | 87.5 to 108 MHz |
| | AM | | | 510 to 1620 KHz |
| SENSITIVITY | FM | S/N = 26dB | $\Delta f$ = 22.5KHz | 1 $\mu$V |
| | AM | S/N = 6dB | m = 0.3 | 1 $\mu$V |
| | AM | S/N = 26dB | m = 0.3 | 10 $\mu$V |
| DISTORTION (fm = 1KHz) | FM | $P_o$ = 0.5W | $\Delta f$ = 22.5KHz | 0.25% |
| | | | $\Delta f$ = 75KHz | 0,7% |
| | AM | $V_i$ = 100 $\mu$V | m = 0.3 | 0.4% |
| | | | m = 0,8 | 0,8% |
| SIGNAL TO NOISE (fm = 1KHz) | FM | $P_o$ = 0.5W<br>$V_i$ = 100 $\mu$V | $\Delta f$ = 22.5KHz | 64 dB |
| | AM | $P_o$ = 0.5W<br>$V_i$ = 1 mV | m = 0.3 | 50dB |
| AMPLITUDE MODULATION REJECTION | FM | $V_i$ = 100 $\mu$V | $\Delta f$ = 22.5KHz m = 0.3 | 50dB |
| TWEET | 2nd H. | f = 911 KHz | | 0.3% |
| | 3rd H. | f = 1370 KHz | | 0.07% |
| QUIESCENT CURRENT | | | | 20mA |
| SUPPLY VOLTAGE RANGE | | | | 3 to 12V |

## APPLICATION INFORMATION (continued)

Fig. 14 - Low cost 27 MHz receiver

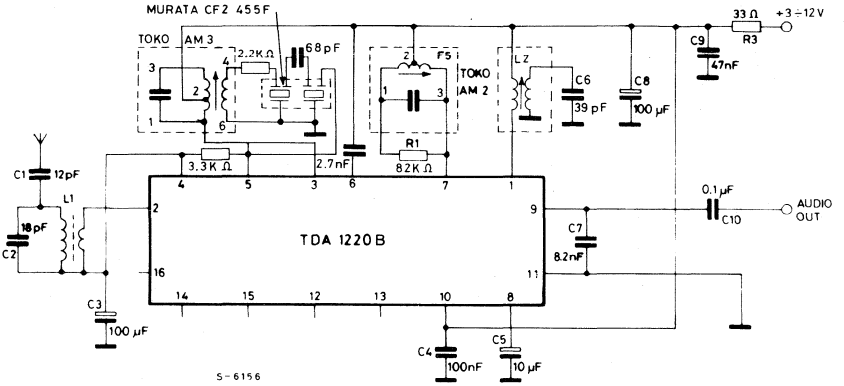
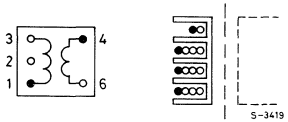
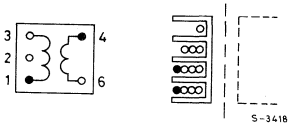



Fig. 15 - L2 Oscillator coil



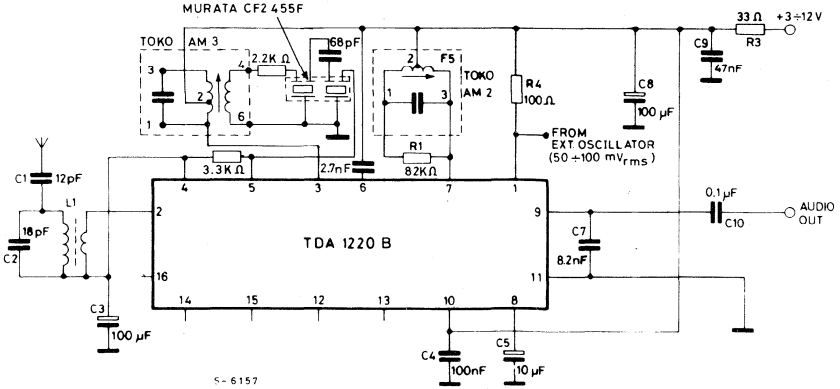

Coil support: Toko 10K
Primary winding: 10 Turns of enamelled copper wire 0.16 mm diameter (pins 3-1).
Secondary winding: 4 Turns copper wire 0.16 mm diameter (pins 6-4)

Fig. 16 - L1 Antenna Coil




Coil support: Toko 10K.
Primary winding: as L2 (pins 3-1)
Secondary winding: 2 Turns copper wire 0.16 mm diameter (pins 6-4)

Fig. 17 - Low cost 27 MHz receiver with external xtal oscillator



## APPLICATION INFORMATION (continued)

Fig. 18 - 455 KHz FM narrow band IF

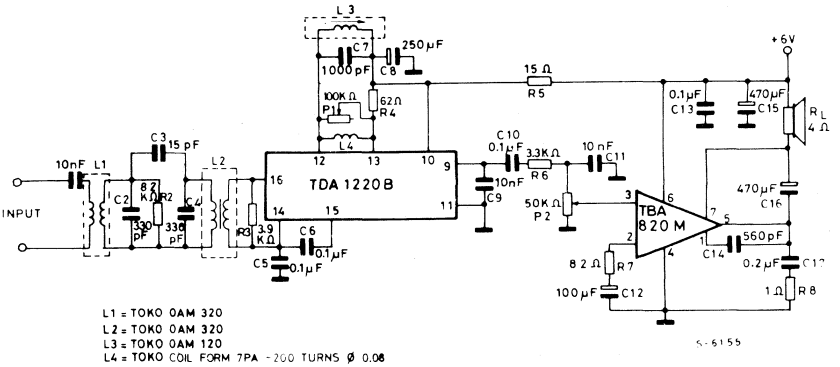
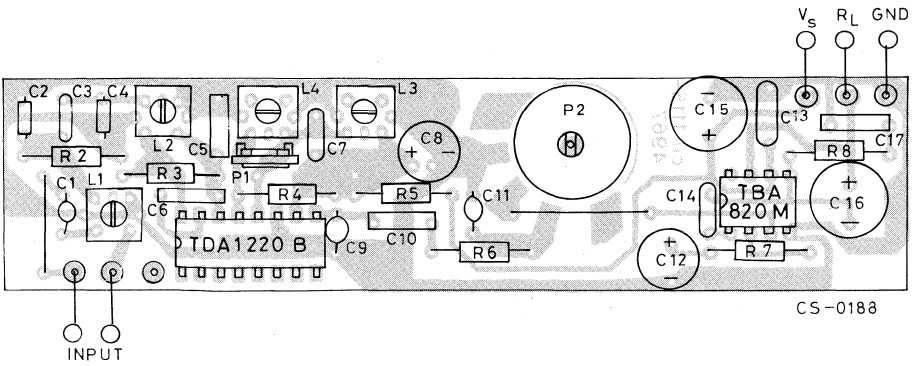



Fig. 19 - P.C. board and component layout of the circuit of fig. 18



## APPLICATION INFORMATION (continued)

Fig. 20 - Discriminator "S" curve response (circuit of fig. 18)

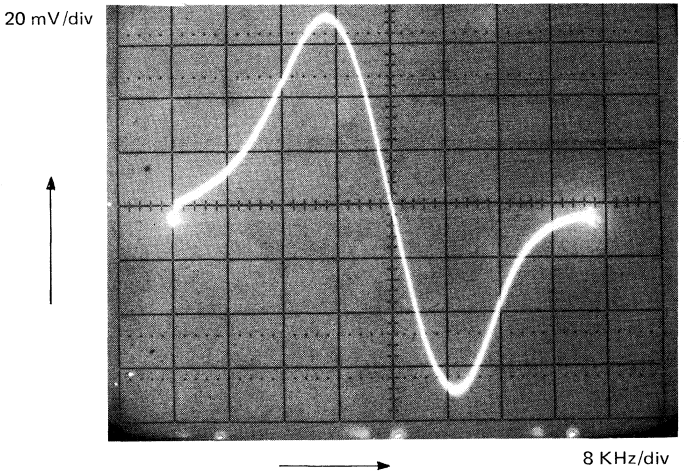
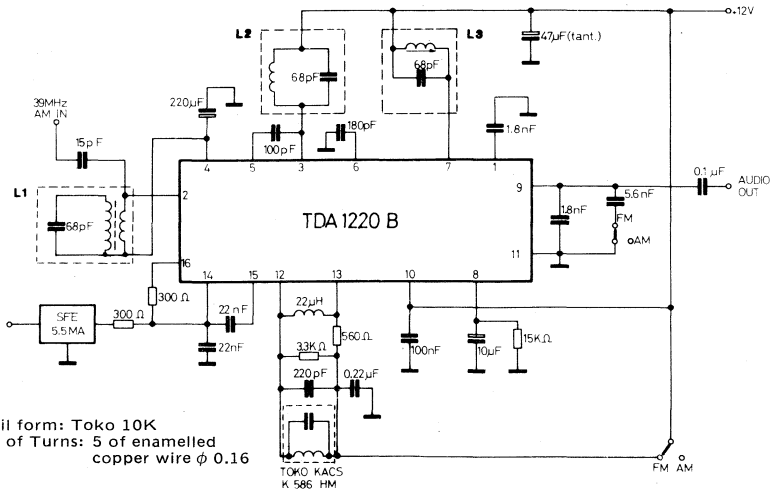



Fig. 21 - Application in sound channel of multistandard TV or in parallel AM modulated sound channel (AM section only).




**L2, L3** Coil form: Toko 10K
N° of Turns: 5 of enamelled copper wire $\phi$ 0.16

**L1** Coil form: Toko 10K
N° of Turns: 5+2 of enamelled copper wire $\phi$ 0.16

## ELECTRICAL CHARACTERISTICS ($V_s$ = 12V)

AM Section ($f_o$ = 39MHz; $f_m$ = 15KHz)

| Parameter | Typ | Unit |
|---|---|---|
| Audio out (m = 0.3) | 60 | mV |
| S/N ($V_i$ = 100 $\mu$V; m = 0.3) | 37 | dB |
| S/N ($V_i$ = 1mV; m = 0.3) | 55 | dB |
| S/N ($V_i$ = 10mV; m = 0.3) | 56 | dB |
| AGC range (m = 0.8, $\Delta$Vout = 3dB) | 65 | dB |
| Max input signal handling (m = 0.8; d = 5%) | 150 | mV |
| −3dB bandwidth | 600 | KHz |
| Distortion ($V_i$ = 100 $\mu$V; m = 0.3) | 2 | % |
| ($V_i$ = 1mV; m = 0.3) | 1 | % |
| ($V_i$ = 10mV; m = 0.3) | 0.8 | % |
| ($V_i$ = 100 $\mu$V; m = 0.8) | 7 | % |
| ($V_i$ = 1mV; m = 0.8) | 5 | % |
| ($V_i$ = 10mV; m = 0.8) | 3 | % |

FM Section ($f_o$ = 5.5MHz; $f_m$ = 1KHz)

| Parameter | Typ | Unit |
|---|---|---|
| −3dB input limiting voltage ($\Delta$f = 25KHz) | 3 | $\mu$V |
| AMR ($\Delta$f = +25KHz; m = 0.3; $V_i$ = 100 $\mu$V) | 40 | dB |
| ($\Delta$f = +25KHz; m = 0.3; $V_i$ = 1mV) | 58 | dB |
| ($\Delta$f = +25KHz; m = 0.3; $V_i$ = 10mV) | 54 | dB |
| S/N ($\Delta$f = ±25KHz; $V_i$ = 100 $\mu$V) | 51 | dB |
| S/N ($\Delta$f = ±25KHz; $V_i$ = 1mV) | 70 | dB |
| S/N ($\Delta$f = ±25KHz; $V_i$ = 10mV) | 70 | dB |
| Distortion ($\Delta$f = ±25KHz; $V_i$ = 100 $\mu$V) | 0.5 | % |
| ($\Delta$f = ±25KHz; $V_i$ = 1mV) | 0.6 | % |
| ($\Delta$f = ±25KHz; $V_i$ = 10mV) | 0.6 | % |
| ($\Delta$f = ±50KHz; $V_i$ = 100 $\mu$V) | 1 | % |
| ($\Delta$f = ±50KHz $V_i$ = 1mV) | 1 | % |
| ($\Delta$f = ±50KHz; $V_i$ = 10mV) | 1 | % |
| Recovered audio ($\Delta$f = ±15KHz; $V_i$ = 1mV) (Recovered audio can be varied by variation of 3.3K ohm resistor in parallel with the discriminator coil) | 70 | mV |
| Max input signal handling | 1 | V |

Note: AM performance at 39MHz can be improved by mean of a selective preamplifier stage.

# LINEAR INTEGRATED CIRCUITS

**TDA1220L**

**PRELIMINARY DATA**

## LOW VOLTAGE AM-FM RADIO

The TDA 1220L is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed for use in 4.5V-6V portable AM-FM radio receivers.
The functions incorporated are:

**AM SECTION**

- Preamplifier and double balanced mixer
- One pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

**FM SECTION**

- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier

The TDA 1220L is suitable up to 30 MHz AM and for FM bands and features:

- High sensitivity and low noise
- Very low tweet
- High signal handling
- Low battery drain
- AM sensitivity regulation facility
- Operating supply voltage: 2.5V to 9V
- Very simple DC switching of AM-FM

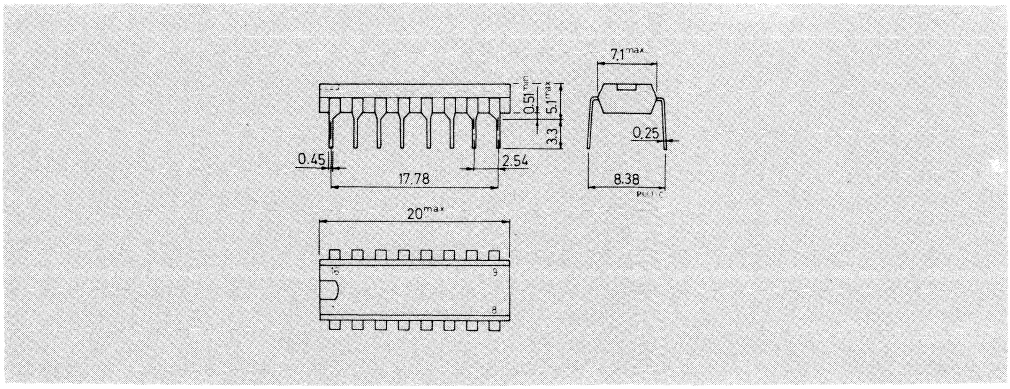
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 12 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb} < 110°C$ | 400 | mW |
| $T_{op}$ | Operating temperature | -20 to 85 | °C |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -55 to 150 | °C |

**ORDERING NUMBER:** TDA 1220LK

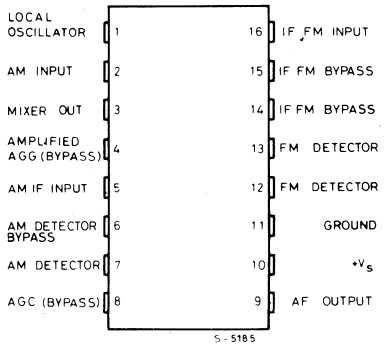
## MECHANICAL DATA

Dimensions in mm

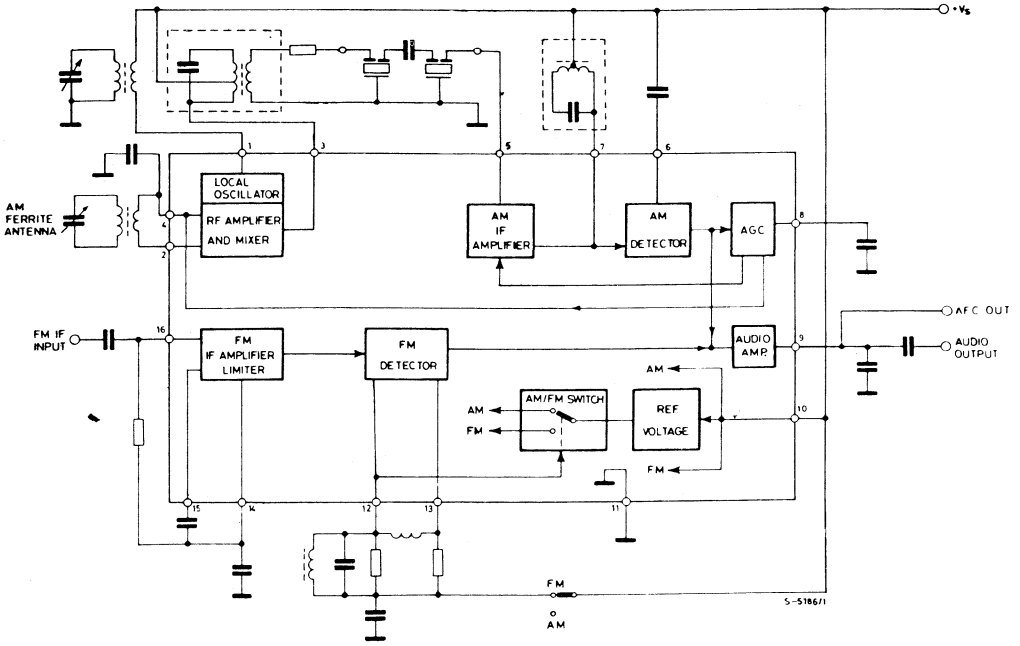


# TDA1220L

## CONNECTION DIAGRAM




## BLOCK DIAGRAM




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$= 25°C, $V_s$= 4.5V unless otherwise specified, refer to test circuit)

| | Parameter | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_d$ | Drain current | AM section | | | 10 | 15 | mA |
| | | FM section | | | 7 | 11 | mA |

### AM SECTION ($f_o$ = 1 MHz; $f_m$= 1 KHz)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_i$ | Input sensitivity | S/N = 26 dB | m = 0.3 | | 15 | 25 | μV |
| S/N | | $V_i$ = 10 mV | m = 0.3 | 45 | 50 | | dB |
| $V_i$ | AGC range | $\Delta V_{out}$= 10 dB | m = 0.8 | 94 | 100 | | dB |
| $V_o$ | Recovered audio signal (pin 9) | $V_i$ = 1 mV | m = 0.3 | 70 | 90 | 120 | mV |
| d | Distortion | | | | 0.4 | 1 | % |
| $V_H$ | Max input signal handling capability | m = 0.8 | d < 10% | 1 | | | V |
| $R_i$ | Input resistance between pins 2 and 4 | m = 0 | | | 7.5 | | KΩ |
| $C_i$ | Input capacitance between pins 2 and 4 | m = 0 | | | 18 | | pF |
| $R_o$ | Output resistance (pin 9) | | | 3.5 | 5 | 6.5 | KΩ |
| | Tweet 2 IF | m = 0,3 | $V_i$ = 1 mV | | 40 | | dB |
| | Tweet 3 IF | | | | 55 | | dB |

### FM SECTION ($f_o$ = 10.7 MHz; $f_m$= 1 KHz)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_i$ | Input limiting voltage | -3 dB limiting point | | | 26 | 36 | μV |
| AMR | Amplitude modulation rejection | $\Delta f$ = ± 22.5 KHz<br>$V_i$ = 3 mV | m = 0.3 | 35 | 46 | | dB |
| S/N | Ultimate quieting | $\Delta f$ = ± 22.5 KHz | $V_i$ = 1 mV | 55 | 64 | | dB |
| d | Distortion | $\Delta f$ = ± 22.5 KHz | $V_i$ = 1 mV | | 0.3 | 0.6 | % |
| $V_o$ | Recovered audio signal (pin 9) | $\Delta f$ = ± 22.5 KHz | $V_i$ = 1 mV | 55 | 80 | 100 | mV |
| $R_i$ | Input resistance between pin 16 and ground | | | | 6.5 | | KΩ |
| $C_i$ | Input capacitance between pin 16 and ground | | | | 14 | | pF |
| $R_o$ | Output resistance (pin 9) | | | 3.5 | 5 | 6.5 | KΩ |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $V_s$ = 3V unless otherwise specified, refer to test circuit)

| | Parameter | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_d$ | Drain current | AM section | | | 9 | 14 | mA |
| | | FM section | | | 6 | 10 | mA |
| **AM SECTION** ($f_o$ = 1 MHz; $f_m$ = 1 KHz) | | | | | | | |
| $V_i$ | Input sensitivity | S/N = 26 dB | m = 0.3 | | 15 | 25 | μV |
| S/N | | $V_i$ = 10 mV | m = 0.3 | 45 | 50 | | dB |
| $V_i$ | AGC range | $\Delta V_{out}$ = 10 dB | m = 0.8 | 94 | 100 | | dB |
| $V_o$ | Recovered audio signal (pin 9) | $V_i$ = 1 mV | m = 0.3 | 70 | 95 | 120 | mV |
| d | Distortion | | | | 0.4 | 1 | % |
| $V_H$ | Max input signal handling capability | m = 0.8 | d < 10% | 1 | | | V |
| $R_i$ | Input resistance between pins 2 and 4 | m = 0 | | | 7.5 | | KΩ |
| $C_i$ | Input capacitance between pins 2 and 4 | m = 0 | | | 18 | | pF |
| $R_o$ | Output resistance (pin 9) | | | 3.5 | 5 | 6.5 | KΩ |
| | Tweet 2 IF | m = 0,3 | $V_i$ = 1 mV | | 40 | | dB |
| | Tweet 3 IF | | | | 55 | | dB |
| **FM SECTION** ($f_o$ = 10.7 MHz; $f_m$ = 1 KHz) | | | | | | | |
| $V_i$ | Input limiting voltage | -3 dB limiting point | | | 40 | 75 | μV |
| AMR | Amplitude modulation rejection | Δf = ± 22.5 KHz<br>$V_i$ = 3 mV | m = 0.3 | 35 | 42 | | dB |
| S/N | Ultimate quieting | Δf = ± 22.5 KHz | $V_i$ = 1 mV | 55 | 64 | | dB |
| d | Distortion | Δf = ± 22.5 KHz | $V_i$ = 1 mV | | 0.3 | 0.7 | % |
| | | Δf = 75 KHz | | | 0.9 | | % |
| $V_o$ | Recovered audio signal (pin 9) | Δf = ± 22.5 KHz | $V_i$ = 1 mV | 55 | 80 | 100 | mV |
| $R_i$ | Input resistance between pin 16 and ground | | | | 6.5 | | KΩ |
| $C_i$ | Input capacitance between pin 16 and ground | | | | 14 | | pF |
| $R_o$ | Output resistance (pin 9) | | | 3.5 | 5 | 6.5 | KΩ |

Fig. 1 - Test circuit

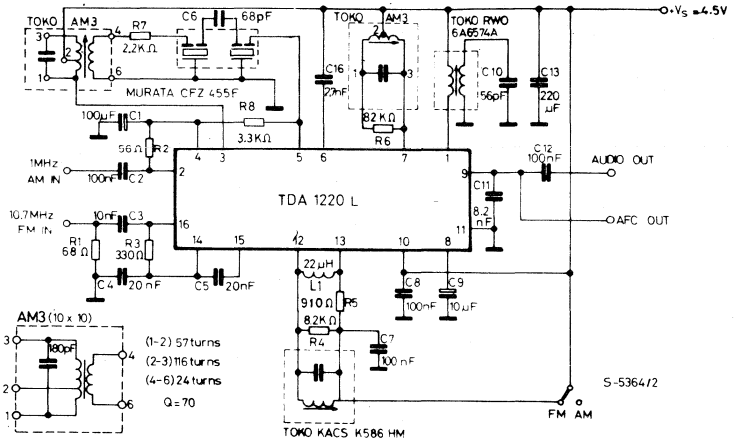
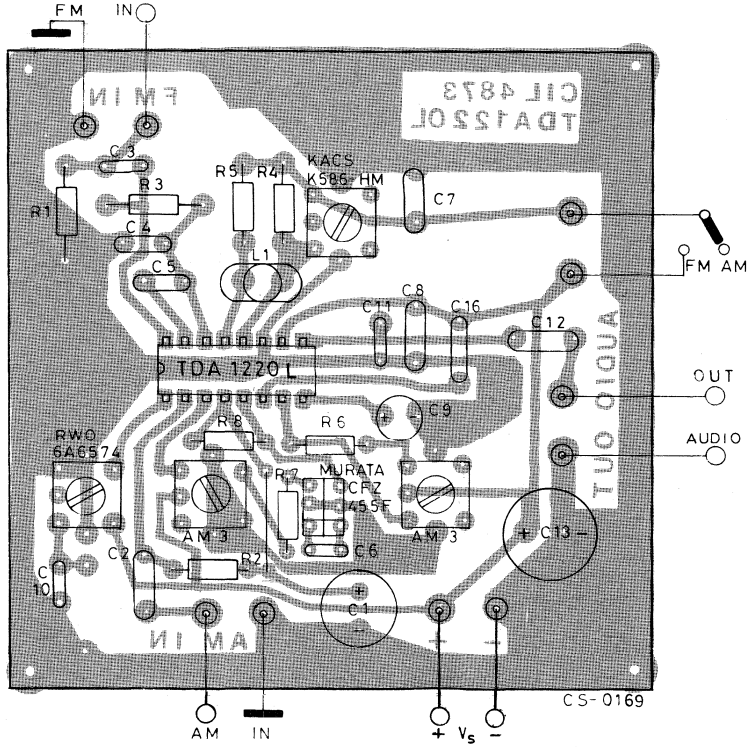



Fig. 2 - PC board and component layout (1:1 scale) of the test circuit.



## APPLICATION INFORMATION

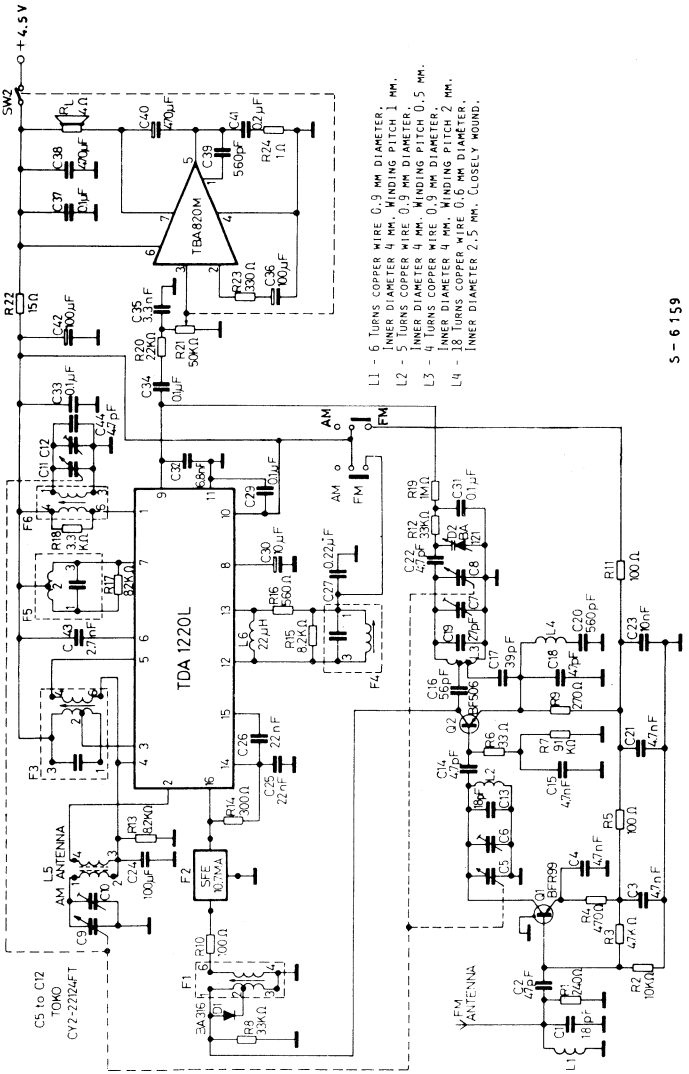
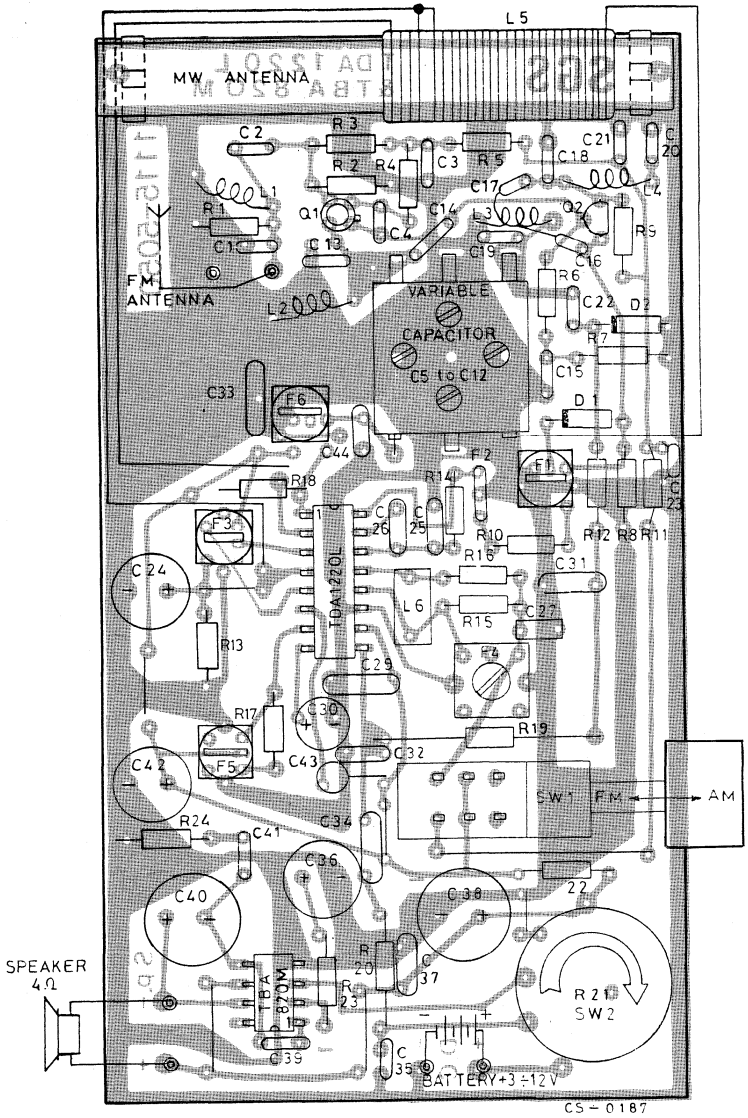



Fig. 3 - Portable AM/FM radio

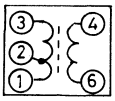
## APPLICATION INFORMATION

Fig. 4 - PC board and component layout of the circuit of fig. 3. (1:1 scale)



## APPLICATION INFORMATION (continued)

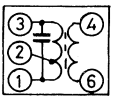
### F1 - 10.7 MHz IF Coil



| $C_o$ (pF) | f (MHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| | | 1-3 | 1-2 | 2-3 | 4-6 |
| – | 10.7 | 1.05 | 6 | 8 | 2 |

TOKO - FM1 - 7x7 mm.
119 AN - A5066R

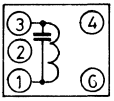
### F3 - 455 KHz IF Coil



| $C_o$ (pF) | f (KHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| 1-3 | | 1-3 | 1-2 | 2-3 | 4-6 |
| 180 | 455 | 70 | 63 | 81 | 7 |

TOKO - AM1 - 7x7 mm.
7LC - A5070EK

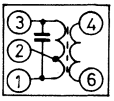
### F4 - FM Detector Coil



| $C_o$ (pF) | f (MHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| 1-3 | | 1-3 | 1-3 | – | – |
| 82 | 10.7 | 100 | 12 | – | – |

TOKO - 10x10 mm.
KACS - K586 HM

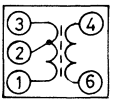
### F5 - 455 KHz IF Coil



| $C_o$ (pF) | f (KHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| 1-3 | | 1-3 | 1-2 | 2-3 | 4-6 |
| 180 | 455 | 70 | 41 | 103 | 20 |

TOKO - AM3 - 7x7 mm.
7LC - A5073 EK

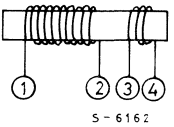
### F6 - AM Oscillator Coil



| f (KHz) | L (μH) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| | 1-3 | 1-3 | 1-2 | 2-3 | 4-6 |
| 796 | 320 | 80 | 90 | 3 | 9 |

TOKO - OAM320 - 7x7 mm.
7BO - A5071 DC

### L5 - Antenna Coil




| f (KHz) | L (μH) | $Q_o$ | TURNS | |
|---|---|---|---|---|
| | 1-2 | 1-2 | 1-2 | 3-4 |
| 796 | | | 105 | 7 |

WIRE: LITZ - 10x0.05 mm.
CORE: 10x80 mm.

## APPLICATION INFORMATION (continued)

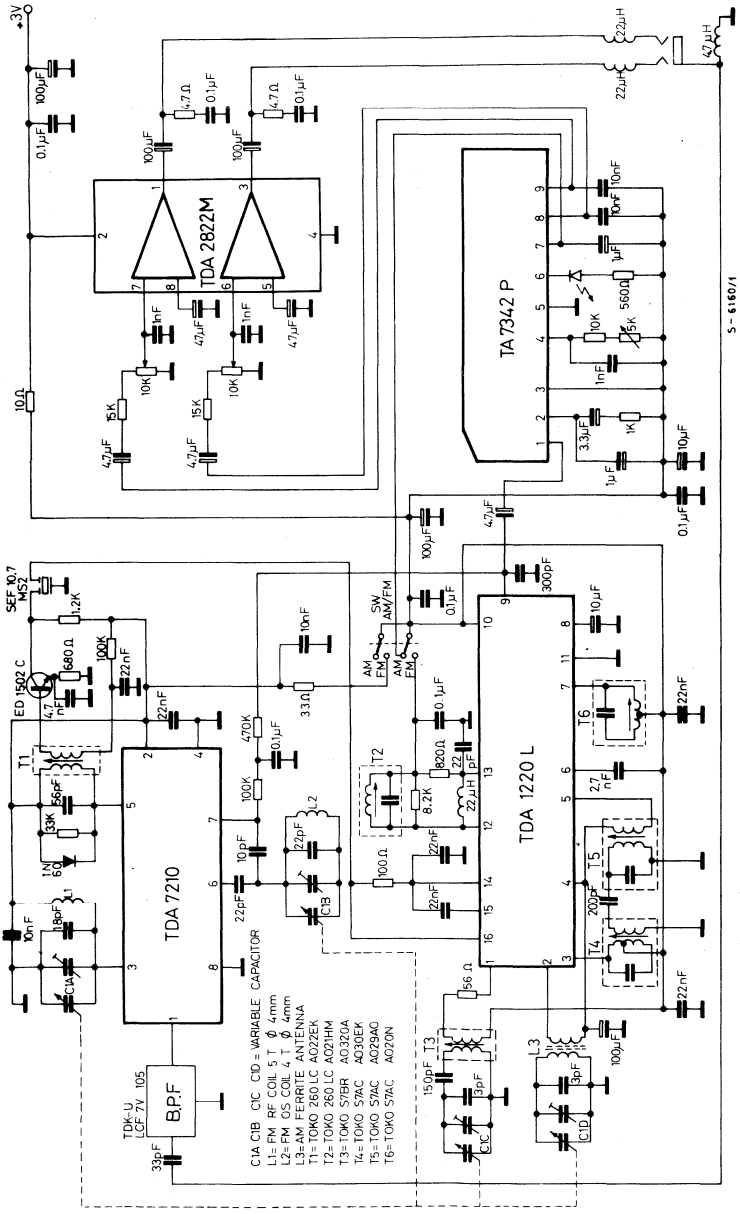



Fig. 5 - 3V AM/FM Stereo application

# TDA1670A

# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## VERTICAL DEFLECTION CIRCUIT

The TDA 1670A is a monolithic integrated circuit in 15-lead Multiwatt® package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke of 110° colour TV picture tubes. It offers a wide range of applications also in portable CTVs, BW TVs, monitors and displays. The functions incorporated are.

- Synchronization circuit
- Precision oscillator and ramp generator
- Power output amplifier with high current capability
- Flyback generator
- Voltage regulator
- Precision blanking pulse generator
- Thermal shut down protection
- CRT screen protection circuit which blanks the beam current in the event of loss of vertical deflection current.

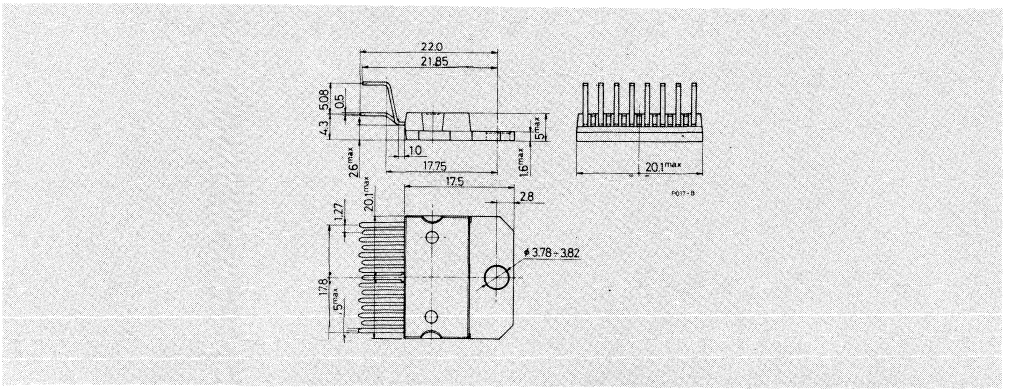
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage at pin 14 | 35 | V |
| $V_1$, $V_2$ | Flyback peak voltage | 60 | V |
| $V_5$ | Sync. input voltage | 20 | V |
| $V_{11}$,$V_{12}$ | Power amplifier input voltage | $\begin{cases} V_s \\ -10 \end{cases}$ | V |
| $V_{13}$ | Voltage at pin 13 | $V_s$ | |
| $I_o$ | Output current (non repetitive) at t = 2 msec | 3 | A |
| $I_o$ | Output peak current at f = 50 Hz t > 10 $\mu$sec | 2 | A |
| $I_o$ | Output peak current at f = 50 Hz t ⩽ 10 $\mu$sec | 3.5 | A |
| $I_{15}$ | Pin 15 peak to peak flyback current at f = 50 Hz, $t_{fly}$ ⩽ 1.5 msec | 3 | A |
| $I_{15}$ | Pin 15 DC current at $V_1 < V_{14}$ | 100 | mA |
| $P_{tot}$ | Maximum power dissipation at $T_{case}$ ⩽ 60°C | 30 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

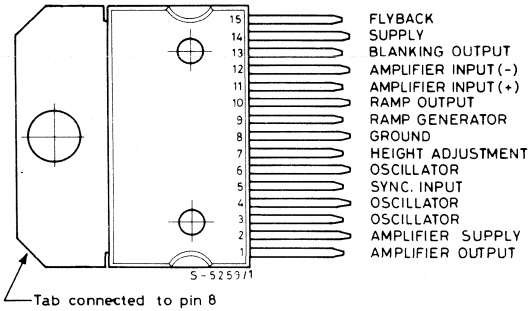
**ORDERING NUMBER:** TDA 1670A

## MECHANICAL DATA

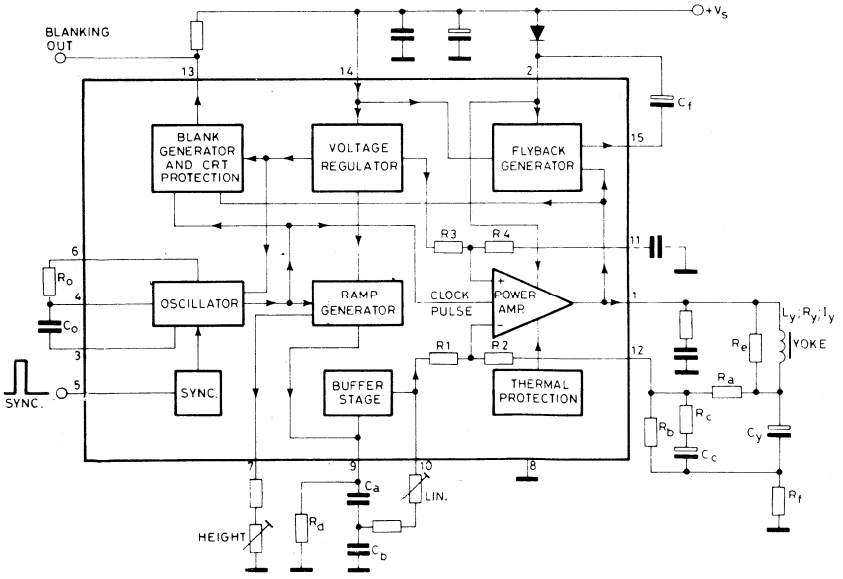
Dimensions in mm



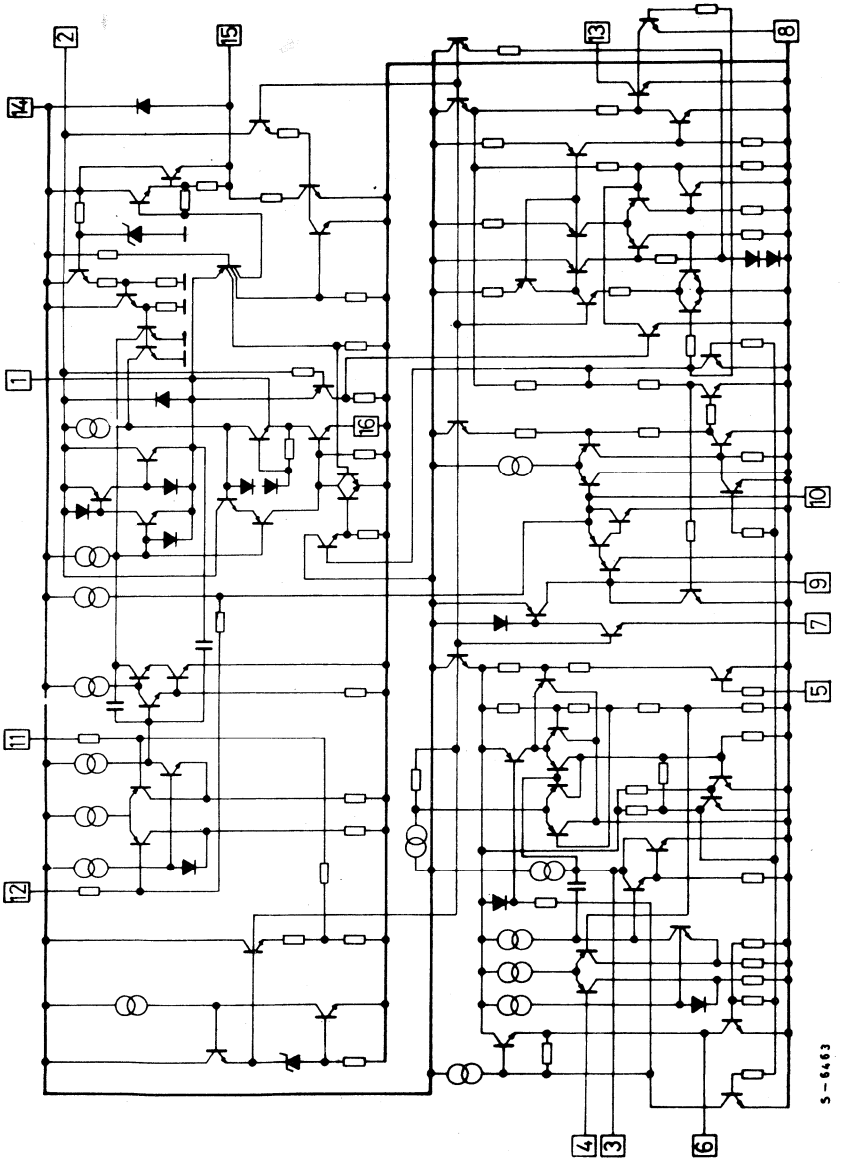
## CONNECTION DIAGRAM
(top view)




## BLOCK DIAGRAM



## SCHEMATIC DIAGRAM



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 40 | °C/W |

## ELECTRICAL CHARACTERISTICS ($V_s$= 35V, $T_{amb}$= 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | |
| $I_2$ | Pin 2 quiescent current | $I_1$= 0 | | 16 | 36 | mA | 1b |
| $-I_9$ | Ramp generator bias current | $V_9$= 0 | | 0.02 | 1 | μA | 1b |
| $-I_9$ | Ramp generator current | $V_9$= 0; $-I_7$= 20 μA | 18.5 | 20 | 21.5 | μA | 1b |
| $\left\lvert\frac{\Delta I_9}{I_9}\right\rvert$ | Ramp generator non linearity | $\Delta V_9$= 0 to 15V<br>$-I_7$= 20 μA | | 0.2 | 1 | % | 1b |
| $I_{14}$ | Pin 14 quiescent current | | | 25 | 45 | mA | 1b |
| $V_1$ | Quiescent output voltage | $V_s$= 35V; $R_a$= 2.2 KΩ<br>$R_b$= 1 KΩ | 16.4 | 17.8 | 19.5 | V | 1a |
| | | $V_s$= 15V; $R_a$= 390Ω<br>$R_b$= 1 KΩ | 6.9 | 7.5 | 8.1 | V | |
| $V_{1L}$ | Output saturation voltage to ground | $I_1$= 1.2A | | 1 | 1.4 | V | 1c |
| $V_{1H}$ | Output saturation voltage to supply | $-I_1$= 1.2A | | 1.6 | 2.2 | V | 1d |
| $V_4$ | Oscillator virtual ground | | | 0.45 | | V | 1b |
| $V_7$ | Regulated voltage at pin 7 | $-I_7$= 20 μA | 6.3 | 6.6 | 7 | V | 1b |
| $\frac{\Delta V_7}{\Delta V_s}$ | Regulated voltage drift with supply voltage | $\Delta V_s$= 15 to 35V | | 1 | 2 | $\frac{mV}{V}$ | 1b |
| $V_{11}$ | Amplifier input (+) reference voltage | | 4.1 | 4.4 | 4.7 | V | 1b |
| $V_{13}$ | Blanking output saturation voltage | $I_{13}$= 10 mA | | 0.35 | 0.5 | V | 1a |
| $V_{15}$ | Pin 15 saturation voltage to ground | $I_{15}$= 20 mA | | 1 | 1.5 | V | 1a |

Fig. 1 - DC test circuit

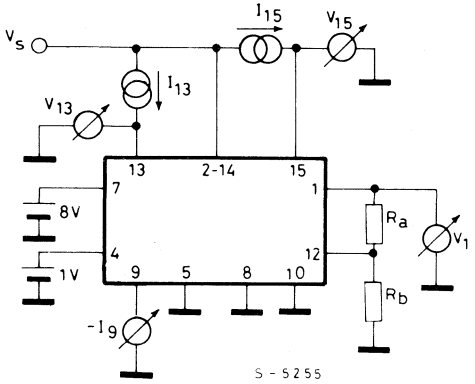



Fig. 1a

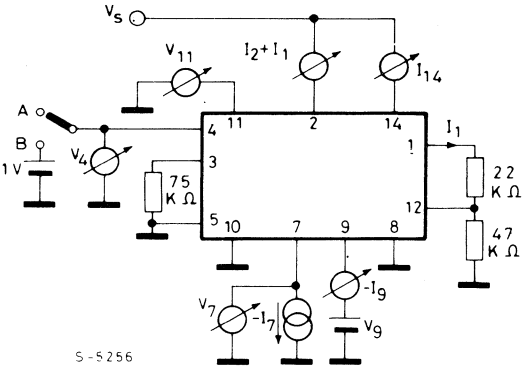



Fig. 1b

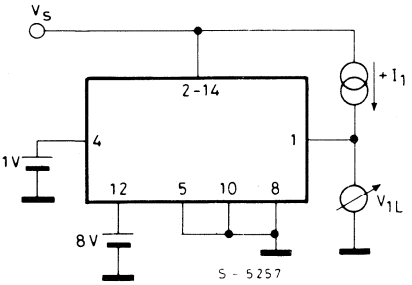



Fig. 1c

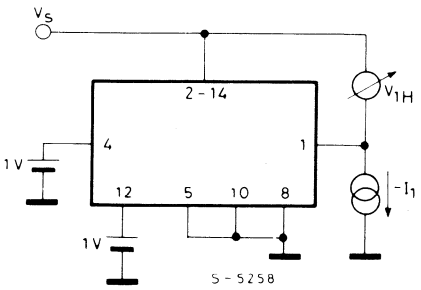



Fig. 1d

**ELECTRICAL CHARACTERISTICS** (Refer to the A.C. test circuit of fig. 2, $T_{amb}$ = 25°C, $V_s$ = 24V, f = 50 Hz, unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | | | |
| $I_s$ | Supply current | $I_y$ = 2 App | | | 295 | | mA |
| $I_5$ | Sync input current required to sync. | | | 100 | | | μA |
| $v_1$ | Flyback voltage | $I_y$ = 2 App | | | 50 | | V |
| $v_3$ | Peak to peak oscillator sawtooth voltage | $I_5$ = 0 | | | 3.6 | | V |
| | | $I_5$ = 100 μA | | | 3.4 | | V |
| $V_{10thL}$ | Start scan level of the input ramp | | | | 1.85 | | V |
| $t_{fly}$ | Flyback time | $I_y$ = 2 App | | | 0.6 | | ms |
| $t_{blank}$ | Blanking pulse duration | $f_o$ = 50 Hz | $T_j$ = 75°C | 1.33 | 1.4 | 1.47 | ms |
| | | $f_o$ = 60 Hz | $T_j$ = 75°C | | 1.17 | | ms |
| $f_o$ | Free running frequency | $R_o$ = 7.5 KΩ $C_o$ = 330 nF | $T_j$ = 75°C | 42 | 43.5 | 45 | Hz |
| | | $R_o$ = 6.2 KΩ $C_o$ = 330 nF | $T_j$ = 75°C | | 52.5 | | Hz |
| Δf | Synchronization range | $I_5$ = 100 μA | $T_j$ = 75°C | 14 | 16 | | Hz |
| $T_j$ | Junction temperature for thermal shut-down | | | | 145 | | °C |

Fig. 2 - AC test circuit

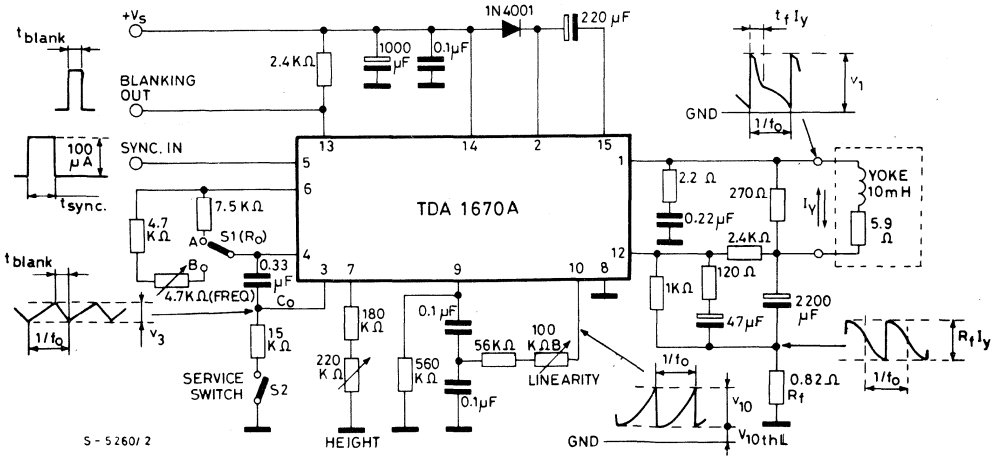
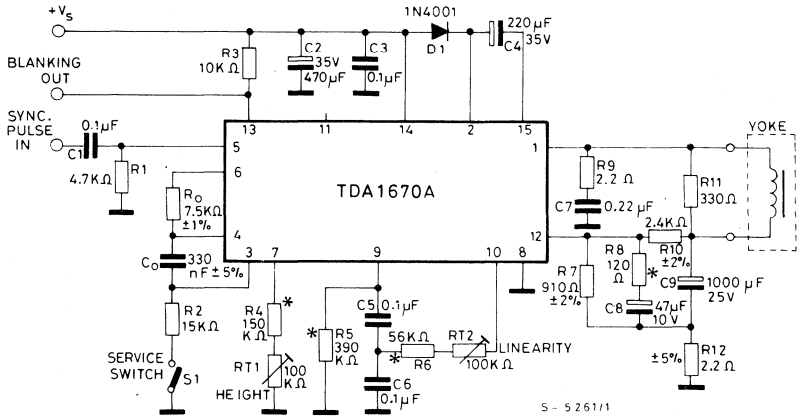


Fig. 3 - Application circuit for small screen 90° TVC set (Ry= 15Ω ; Ly= 30 mH, Iy= 0.82 App)



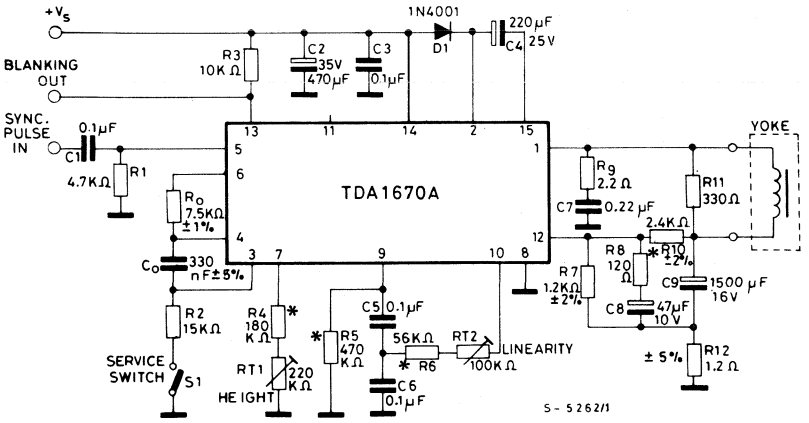

* The value depends on the characteristics of the CRT. The value shown is indicative only.

## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Minimum supply voltage | 25 | V |
| $I_s$ | Supply current | 140 | mA |
| $t_{fly}$ | Flyback time | 0.7 | msec |
| $t_{blkg}$ | Blanking time | 1.4 | msec |
| $f_o$ | Free running frequency | 43.5 | Hz |
| * $P_{tot}$ | Power dissipation | 2.4 | W |
| * $R_{th\ heatsink}$ | Thermal resistance of the heatsink | | |
| | for $T_{amb}$= 60°C and $T_{j\ max}$= 110°C | 13 | °C/W |
| | for $T_{amb}$= 60°C and $T_{j\ max}$= 120°C | 16 | °C/W |

* Worst case condition.

Fig. 4 - Application circuit for 110° TVC set (Ry= 9.6Ω ; Ly= 24.6 mH; Iy = 1.2 App)



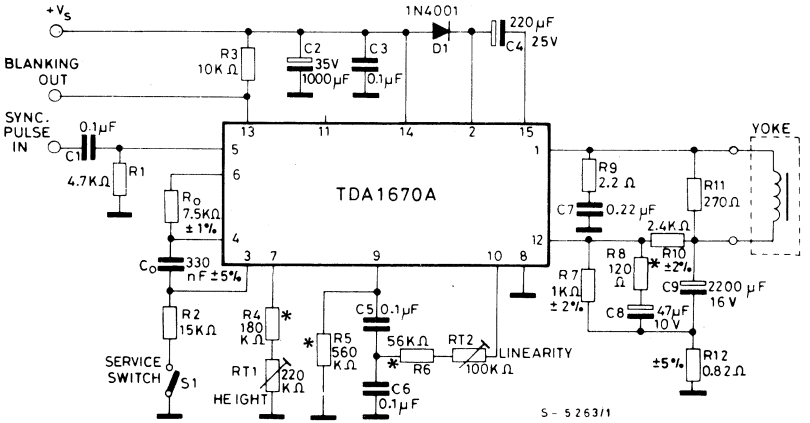

* The value depends on the characteristics of the CRT. The value shown is indicative only.

## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Minimum supply voltage | 22.5 | V |
| $I_s$ | Supply current | 185 | mA |
| $t_{fly}$ | Flyback time | 1 | msec |
| $t_{blkg}$ | Blanking time | 1.4 | msec |
| $f_o$ | Free running frequency | 43.5 | Hz |
| * $P_{tot}$ | Power dissipation | 2.7 | W |
| * $R_{th\ heatsink}$ | Thermal resistance for the heatsink | | |
| | for $T_{amb}$= 60°C and $T_{j\ max}$= 110°C | 11.5 | °C/W |
| | for $T_{amb}$= 60°C and $T_{j\ max}$= 120°C | 14.5 | °C/W |

* Worst case condition.

Fig. 5 - Application circuit for 110° TVC set (Ry= 5.9Ω ; Ly= 10 mH; Iy= 1.95 App)



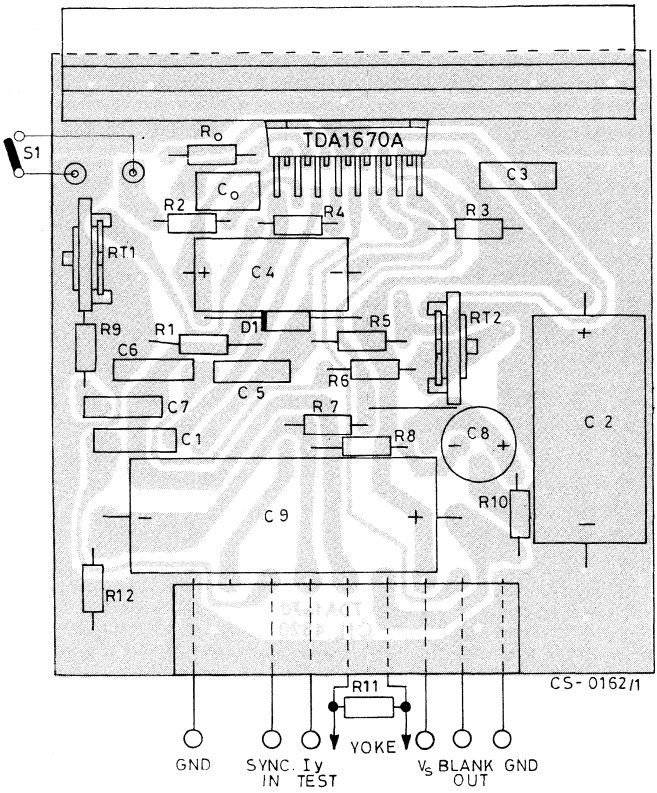

* The value depends on the characteristics of the CRT. The value shown is indicative only.

## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Minimum supply voltage | 24 | V |
| $I_s$ | Supply current | 285 | mA |
| $t_{fly}$ | Flyback time | 0.6 | msec |
| $t_{blkg}$ | Blanking time | 1.4 | msec |
| $f_o$ | Free running frequency | 43.5 | Hz |
| * $P_{tot}$ | Power dissipation | 4.3 | W |
| * $R_{th}$ heatink | Thermal resistance of the heatsink | | |
| | for $T_{amb}$= 60°C and $T_{j\ max}$= 110°C | 6.5 | °C/W |
| | for $T_{amb}$= 60°C and $T_{j\ max}$= 120°C | 8.5 | °C/W |

* Worst case condition.

Fig. 6 - PC board and components layout for the application circuits of fig. 3, 4 and 5 (1 : 1 scale)




## APPLICATION INFORMATION (Refer to the block diagram)

### Oscillator and Sync gate (Clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches $R_o$ high or low so allowing the charge or the discharge of $C_o$ under constant current conditions.
The Sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

**Pin 4** is the inverting input of the amplifier used as integrator.
**Pin 6** is the output of the switch driven by the internal clock pulse generated by the threshold circuits.
**Pin 3** is the output of the amplifier.
**Pin 5** is the input for sync pulses (positive)

## Ramp generator and buffer stage

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.
The internal clock pulse stops the increasing ramp by a very fast discharge of the capacitor; a new voltage ramp is immediately allowed.
The required value of the capacitance is obtained by means of the series of two capacitors, Ca and Cb, which allow the linearity control by applying a feedback between the output of the buffer and the tapping from Ca and Cb.

**Pin 7** The resistance between pin 7 and ground defines the current mirror current and than the height of the scanning.

**Pin 9** is the output of the current mirror that charges the series of Ca and Cb. This pin is also the input of the buffer stage.

**Pin 10** is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R1.

## Power amplifier

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.
The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.
The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

**Pin 12** is the inverting input of the amplifier. An external network, Ra and Rb, defines the DC level across Cy so allowing a correct centering of the output voltage. The series network Rc and Cc, in conjunction with Ra and Rb, applies at the feedback input pin 12 a small part of the parabola, available across Cy, and the AC feedback voltage, taken across Rf. The external components Rc, Ra and Rd, produce the linearity correction on the output scanning current Iy and their values must be optimized for each type of CRT.

**Pin 11** is the non-inverting input and it is not used. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured.
This pin is only used on a quasi-bridge configuration.

**Pin 1** is the output of the power amplifier and it drives the yoke by a negative slope current ramply. Re and the Boucherot cell are used to stabilize the power amplifier.

**Pin 2** The supply voltage of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage $V_s$ by a diode, while during the retrace time this pin is supplied from the flyback generator.

## Flyback generator

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).
The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 14, the flyback pulse front end drives the flyback

generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.
An integrated diode stops the rising of this output increase and the voltage jump is transferred by means of capacitor Cf at the supply voltage pin of the power stage (pin 2).
When the current across the yoke changes its direction, the output of the flyback generator falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.
Later, the increasing flyback current reaches the peak value and then the flyback time is completed: the trace period restarts. The output of the power amplifier (pin 1) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

**Pin 15** is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor Cf transfers the jump to pin 2 (see pin 2).

## Blanking generator and CRT protection

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection. The input is internally driven by the clock pulse that defines the width of the blanking time when a flyback pulse has been generated. If the flyback pulse is absent (short circuit or open circuit of the yoke), the blanking output remains high so allowing the CRT protection.

**Pin 13** is an open collector output where the blanking pulse is available.

## Voltage regulator

The main supply voltage $V_s$ is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

**Pin 14** is the main supply voltage input $V_s$ (positive).
**Pin 8** is the GND pin or the negative input of $V_s$.

Fig. 7 - Output saturation voltage to ground vs. peak output current

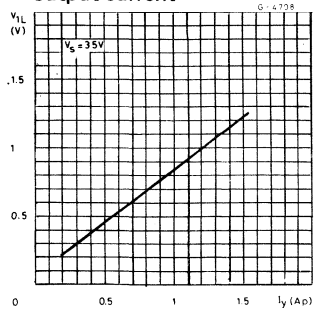



Fig. 8 - Output saturation voltage to supply vs. output peak current

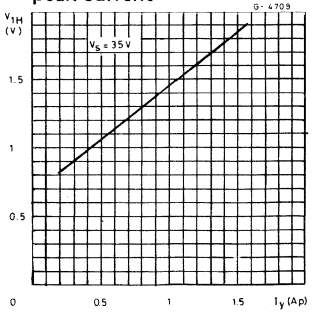
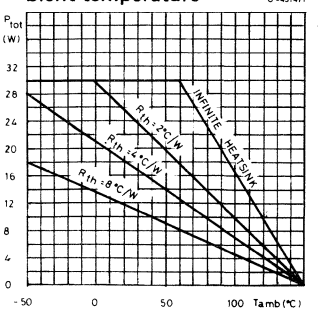


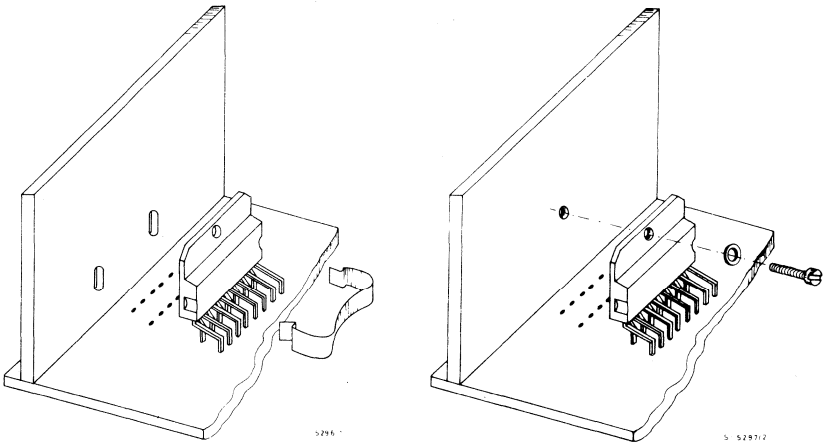

Fig. 9 - Maximum allowable power dissipation vs. ambient temperature



## MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 10 - Mounting example



# LINEAR INTEGRATED CIRCUITS

# TDA1770A

**PRELIMINARY DATA**

## VERTICAL DEFLECTION CIRCUIT

The TDA 1770A is a monolithic integrated circuit in 20-lead plastic package. It is a full performance and very efficient vertical deflection circuit intended for direct drive of the yoke.
It offers a wide range of applications in portable CTVs, BW TVs, monitors and displays. The functions incorporated are:

- synchronization circuit.
- precision oscillator and ramp generator
- power output amplifier
- flyback generator
- voltage regulator
- precision blanking pulse generator
- thermal shut down protection
- CRT screen protection circuit which blanks the beam current in the event of loss of vertical deflection current.

The TDA 1770A is assembled in a new 20-lead plastic package which has 4 centre pins connected together and used for heatsinking.

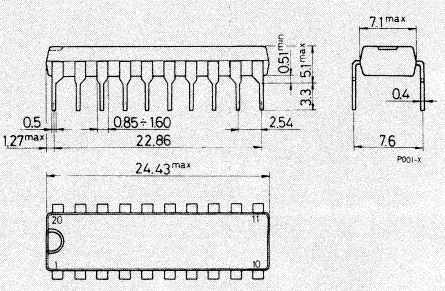
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage at pin 2 | 35 | V |
| $V_7$, $V_8$ | Flyback peak voltage | 60 | V |
| $V_{11}$ | Sync. input voltage | 20 | V |
| $V_{19}$, $V_{20}$ | Power amplifier input voltage | $V_s$ / -10 | V |
| $V_1$ | Voltage at pin 1 | $V_s$ | |
| $I_o$ | Output current (non repetitive) at t = 2 msec | 2 | A |
| $I_o$ | Output peak current at f = 50 Hz t > 10 $\mu$sec | 1.2 | A |
| $I_o$ | Output peak current at f = 50 Hz t ≤ 10 $\mu$sec | 2.2 | A |
| $I_3$ | Pin 3 peak to peak flyback current at f = 50 Hz, $t_{fly} \leq 1.5$ msec | 2 | A |
| $I_3$ | Pin 3 DC current at $V_7 < V_2$ | 50 | mA |
| $P_{tot}$ | Maximum power dissipation: at $T_{pins} \leq 90°C$ | 4.3 | W |
| | at $T_{amb} = 70°C$ | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA 1770A

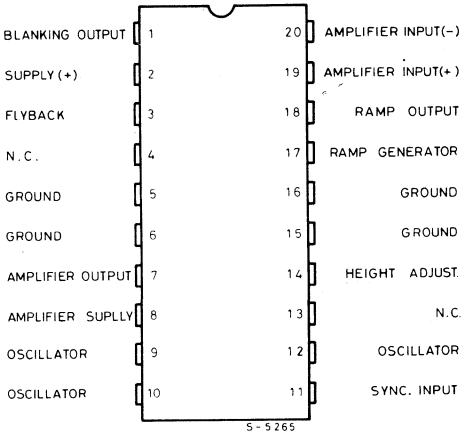
## MECHANICAL DATA

Dimensions in mm

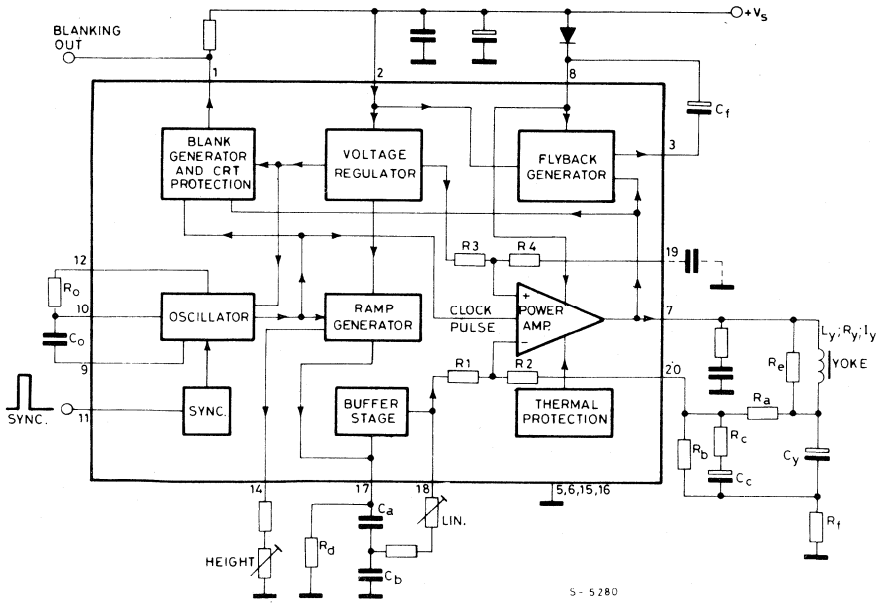


# TDA1770A

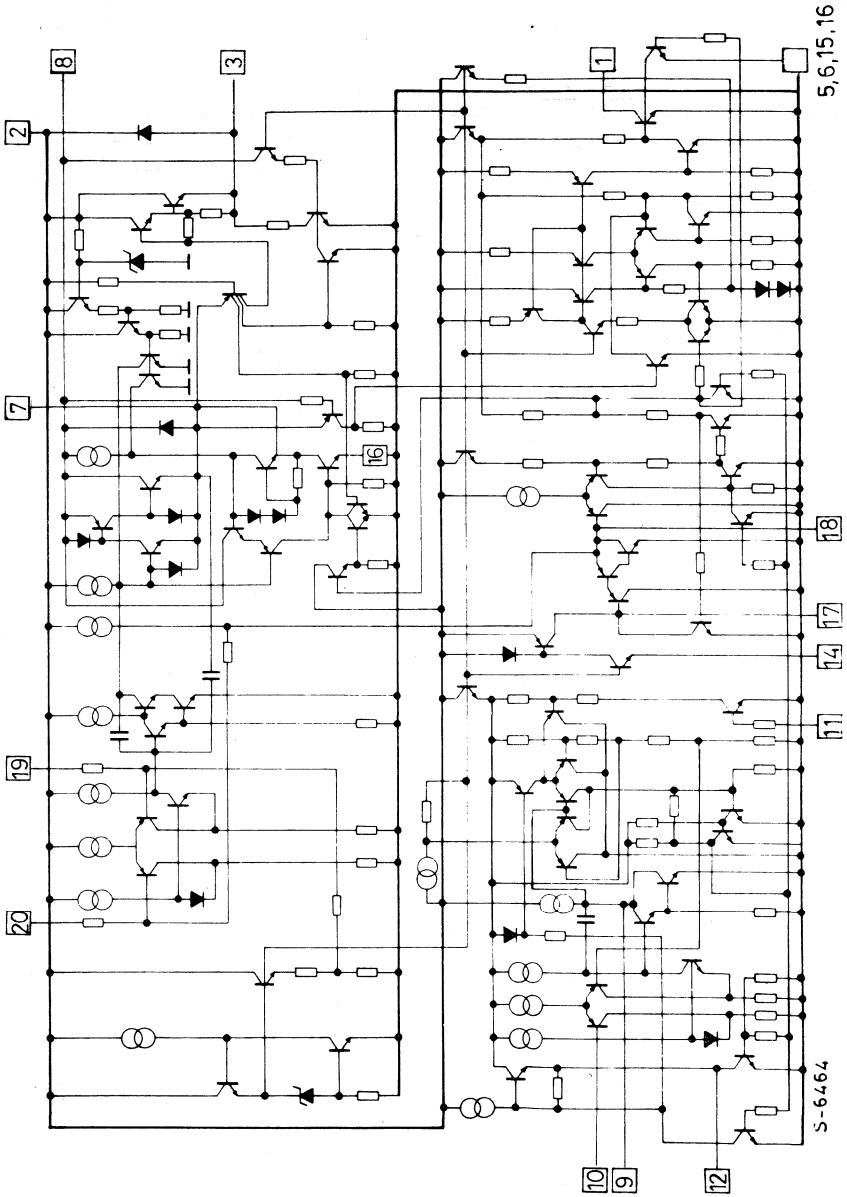
## CONNECTION DIAGRAM
(top view)




## BLOCK DIAGRAM



## SCHEMATIC DIAGRAM



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}pins}$ | Thermal resistance junction-pins | max | 14 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 80 | °C/W |

## ELECTRICAL CHARACTERISTICS ($V_s$= 35V, $T_{amb}$= 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | | |
| $I_2$ | Pin 2 quiescent current | | | 25 | 45 | mA | 1b |
| $I_8$ | Pin 8 quiescent current | $I_7$= 0 | | 16 | 36 | mA | 1b |
| $-I_{17}$ | Ramp generator bias current | $V_{17}$= 0 | | 0.02 | 1 | μA | 1a |
| $-I_{17}$ | Ramp generator current | $V_{17}$= 0; $-I_{14}$= 20 μA | 18.5 | 20 | 21.5 | μA | 1b |
| $\left\lvert\frac{\Delta I_{17}}{I_{17}}\right\rvert$ | Ramp generator non linearity | $\Delta V_{17}$= 0 to 15V<br>$-I_{14}$= 20 μA | | 0.2 | 1 | % | 1b |
| $V_1$ | Blanking output saturation voltage | $I_1$= 10 mA | | 0.35 | 0.5 | V | 1b |
| $V_3$ | Pin 3 saturation voltage to ground | $I_3$= 20 mA | | 1 | 1.5 | V | 1a |
| $V_7$ | Quiescent output voltage | $V_s$= 35V; $R_a$= 2.2 KΩ<br>$R_b$= 1 KΩ | 16.4 | 17.8 | 19.5 | V | 1a |
| | | $V_s$= 15V; $R_a$= 390Ω<br>$R_b$= 1 KΩ | 6.9 | 7.5 | 8.1 | V | |
| $V_{7L}$ | Output saturation voltage to ground | $I_7$= 0.7A | | 0.7 | 1 | V | 1c |
| $V_{7H}$ | Output saturation voltage to supply | $-I_7$= 0.7A | | 1.3 | 1.8 | V | 1d |
| $V_{10}$ | Oscillator virtual ground | | | 0.45 | | V | 1a |
| $V_{14}$ | Regulated voltage at pin 14 | $-I_{14}$= 20 μA | 6.3 | 6.6 | 7 | V | 1b |
| $\frac{\Delta V_{14}}{\Delta V_s}$ | Regulated voltage drift with supply voltage | $\Delta V_s$= 15 to 35V | | 1 | 2 | $\frac{mV}{V}$ | 1b |
| $V_{19}$ | Amplifier input (+) reference voltage | | 4.1 | 4.4 | 4.7 | V | 1b |

Fig. 1 - DC test circuit

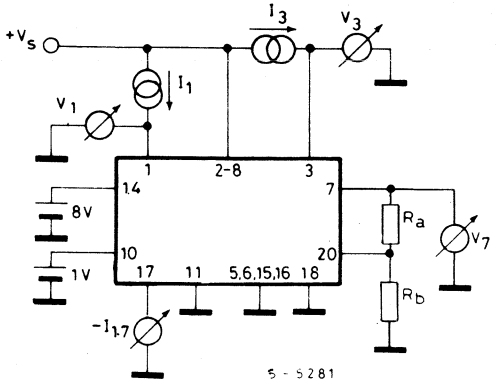



Fig. 1a

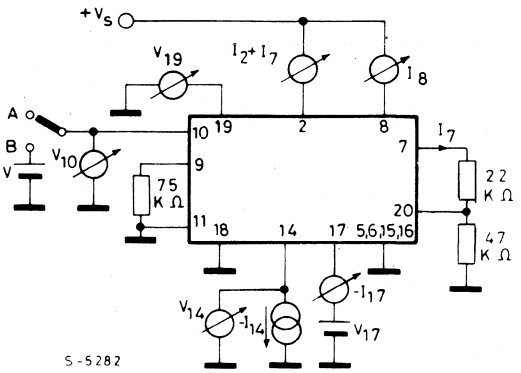



Fig. 1b

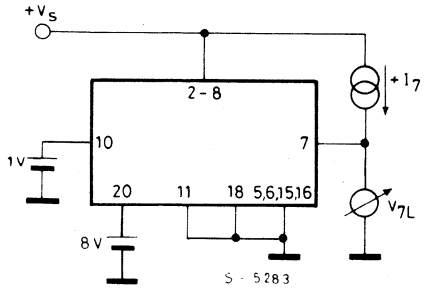



Fig. 1c

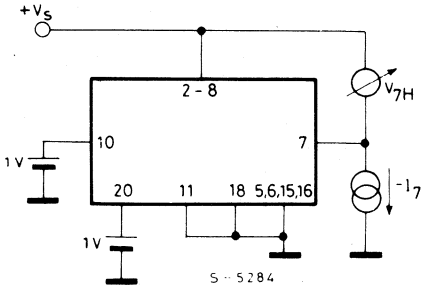



Fig. 1d

## ELECTRICAL CHARACTERISTICS (Refer to the A.C. test circuit of fig. 2, $V_s$= 20V, f= 50 Hz, $T_{amb}$= 25°C, unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | | | |
| $I_s$ | Supply current | $I_y$= 1 App | | | 160 | | mA |
| $I_{11}$ | Sync. input current | | | 100 | | | μA |
| $V_7$ | Flyback voltage | $I_y$= 1 App | | | 42 | | V |
| $V_9$ | Peak to peak oscillator sawtooth voltage | $I_{11}$= 0 | | | 3.6 | | V |
| | | $I_{11}$= 100 μA | | | 3.4 | | V |
| $V_{18thL}$ | Start scan level of the input ramp | | | | 1.85 | | V |
| $t_{fly}$ | Flyback time | $I_y$= 1 App | | | 0.75 | | msec |
| $t_{blank}$ | Blanking pulse duration | $f_o$= 50 Hz | $T_j$ = 75°C | 1.33 | 1.4 | 1.47 | ms |
| | | $f_o$= 60 Hz | $T_j$ = 75°C | | 1.17 | | ms |
| $f_o$ | Free running frequency | $R_o$= 7.5 KΩ $C_o$= 330 nF | $T_j$ = 75°C | 42 | 43.5 | 45 | Hz |
| | | $R_o$= 6.2 KΩ $C_o$= 330 nF | $T_j$ = 75°C | | 52.5 | | Hz |
| Δf | Synchronization range | $I_{11}$= 100 μA | $T_j$ = 75°C | 14 | 16 | | Hz |
| $T_j$ | Junction temperature for thermal shut-down | | | | 145 | | °C |

Fig. 2 - AC test circuit

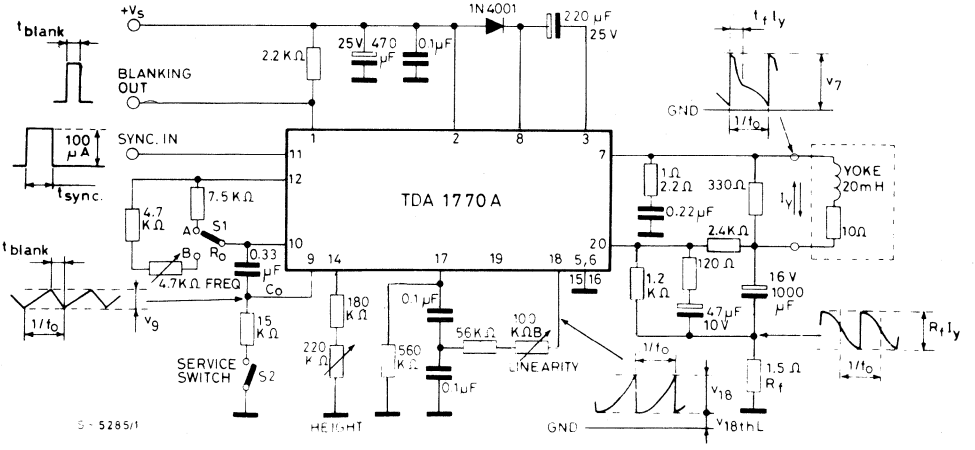
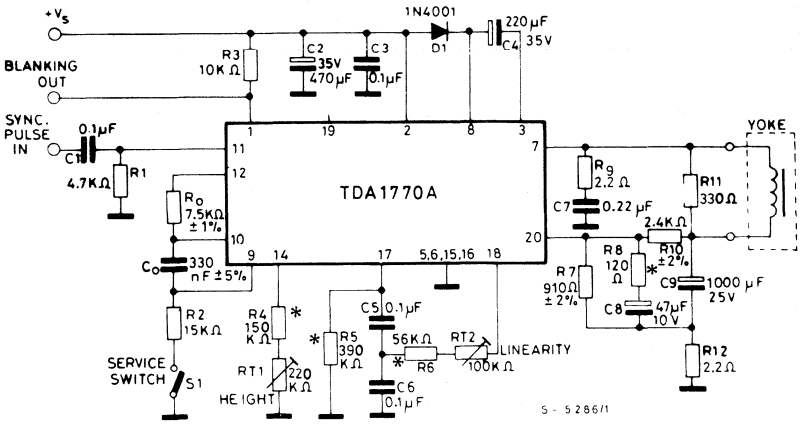


Fig. 3 - Typical application circuit for small screen 90° TVC set (Ry= 15Ω ; Ly= 30 mH; Iy= 0.82 App)



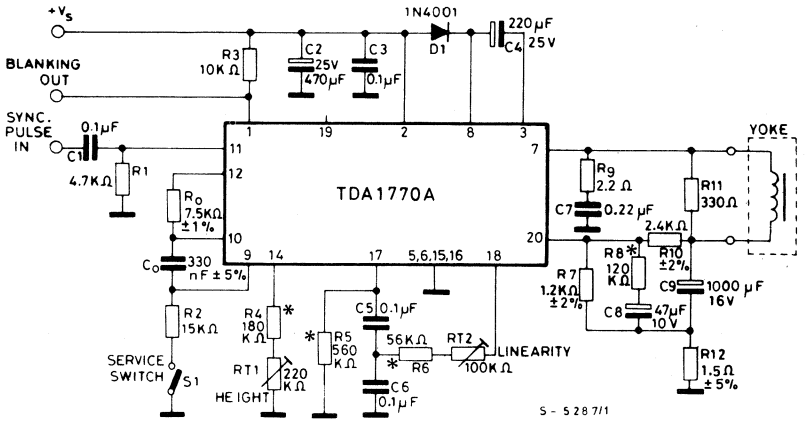

* The value depends on the characteristics of the CRT. The value shown is indicative only.

## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Minimum supply voltage | 25 | V |
| $I_s$ | Supply current | 140 | mA |
| $t_{fly}$ | Flyback time | 0.7 | msec |
| $t_{blkg}$ | Blanking time | 1.4 | msec |
| $f_o$ | Free running frequency | 43.5 | Hz |
| * $P_{tot}$ | Total dissipation | 2.4 | W |
| * $R_{th\ heatsink}$ ** | Thermal resistance of the heatsink for $T_{amb}$= 60°C and $T_{j\ max}$= 130°C | 8 | °C/W |

* Worst case condition. ** See "Thermal considerations".

Fig. 4 - Typical application circuit for B/W TV set (Ry= 10Ω ; Ly= 20 mH; Iy= 1 App)



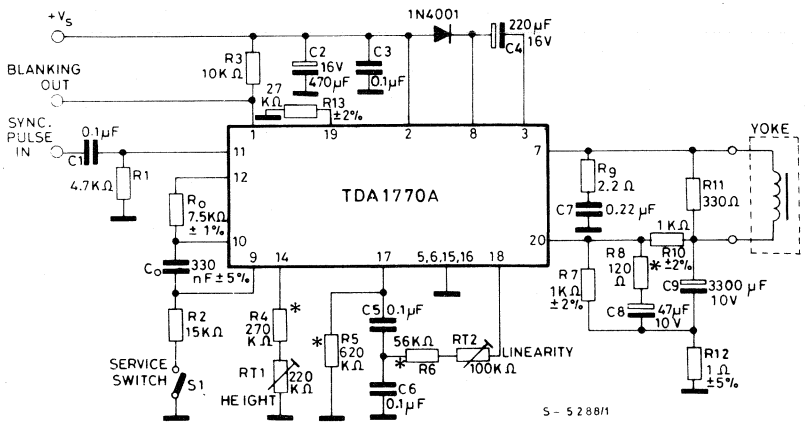

* The value depends on the characteristics of the CRT. The value shown is indicative only.

## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Minimum supply voltage | 20 | V |
| $I_s$ | Supply current | 160 | mA |
| $t_{fly}$ | Flyback time | 0.75 | msec |
| $t_{blkg}$ | Blanking time | 1.4 | msec |
| $f_o$ | Free running frequency | 43.5 | Hz |
| $P_{tot}$ * | Power dissipation | 2.1 | W |
| $R_{th\ heatsink}$ ** | Thermal resistance of the heatsink for $T_{amb}$= 60°C and $T_{j\ max}$= 130°C | 11 | °C/W |

* Worst case condition. ** See "Thermal considerations".

Fig. 5 - Typical application circuit for small screen (Ry= 2.9Ω ; Ly= 6 mH; Iy= 1.1 App)



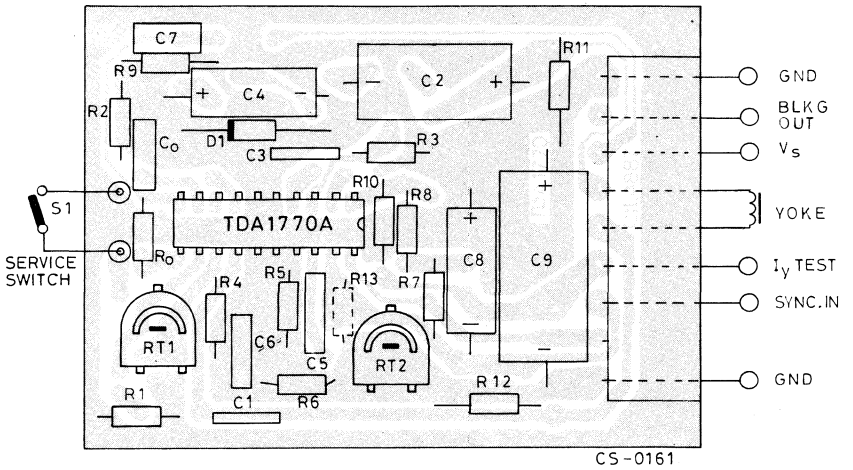

* The value depends on the characteristics of the CRT. The value shown is indicative only.

## Typical performance

| | | | |
|---|---|---|---|
| $V_s$ | Minimum supply voltage | 10.5 | V |
| $I_s$ | Supply current | 170 | mA |
| $t_{fly}$ | Flyback time | 0.45 | msec |
| $t_{blkg}$ | Blanking time | 1.4 | msec |
| $f_o$ | Free running frequency | 43.5 | Hz |
| * $P_{tot}$ | Power dissipation | 1.25 | W |
| * $R_{th\ heatsink}$ ** | Thermal resistance of the heatsink for $T_{amb}$= 60°C and $T_{j\ max}$= 130°C | 28 | °C/W |

* Worst case condition. ** See "Thermal considerations".

Fig. 6 - PC board and components layout for the application circuits of fig. 3, 4 and 5 ( 1:1 scale)




## APPLICATION INFORMATION (Refer to the block diagram)

### Oscillator and Sync gate (Clock generation)

The oscillator is obtained by means of an integrator driven by a two threshold circuit that switches Ro high or low so allowing the charge or the discharge of Co under constant current conditions.
The Sync input pulse at the Sync gate lowers the level of the upper threshold and than it controls the period duration. A clock pulse is generated.

**Pin 10** is the inverting input of the amplifier used as integrator.
**Pin 12** is the output of the switch driven by the internal clock pulse generated by the threshold circuits.
**Pin 9** is the output of the amplifier.
**Pin 11** is the input for sync pulses (positive).

### Ramp generator and buffer stage

A current mirror, the current intensity of which can be externally adjusted, charges one capacitor producing a linear voltage ramp.
The internal clock pulse stops the increasing ramp by a very fast discharge of the capacitor, a new voltage ramp is immediately allowed.
The required value of the capacitance is obtained by means of the series of two capacitors, Ca and Cb, which allow the linearity control by applying a feedback between the output of the buffer and the tapping from Ca and Cb.

**Pin 14** The resistance between pin 14 and ground defines the current mirror current and than the height of the scanning.
**Pin 17** is the output of the current mirror that charges the series of Ca and Cb. This pin is also the input of the buffer stage.
**Pin 18** is the output of the buffer stage and it is internally coupled to the inverting input of the power amplifier through R1.

## APPLICATION INFORMATION (continued)

### Power amplifier

This amplifier is a voltage-to-current power converter, the transconductance of which is externally defined by means of a negative current feedback.
The output stage of the power amplifier is supplied by the main supply during the trace period, and by the flyback generator circuit during the most of the duration of the flyback time. The internal clock turns off the lower power output stage to start the flyback.
The power output stage is thermally protected by sensing the junction temperature and then by putting off the current sources of the power stage.

**Pin 20** is the inverting input of the amplifier. An external network, Ra and Rb, defines the DC level across Cy so allowing a correct centering of the output voltage. The series network Rc and Cc, in conjunction with Ra and Rb, applies at the feedback input pin 20 a small part of the parabola, available across Cy, and the AC feedback voltage, taken across Rf. The external components Rc, Ra and Rd, produce the linearity correction on the output scanning current Iy and their values must be optimized for each type of CRT.

**Pin 19** is the non-inverting input. At this pin the non-inverting input reference voltage supplied by the voltage regulator can be measured.
This pin is used on a quasi-bridge configuration or on portable TVS.

**Pin 7** is the output of the power amplifier and it drives the yoke by a negative slope current ramp Iy. Re and the Boucherot cell are used to stabilize the power amplifier.

**Pin 8** the supply voltage of the power output stage is forced at this pin. During the trace time the supply voltage is obtained from the main supply voltage $V_s$ by a diode, while during the retrace time this pin is supplied from the flyback generator.

### Flyback generator

This circuit supplies both the power amplifier output stage and the yoke during the most of the duration of the flyback time (retrace).
The internal clock opens the loop of the amplifier and lets pin 1 floating so allowing the rising of the flyback. Crossing the main supply voltage at pin 2, the flyback pulse front end drives the flyback generator in such a way allowing its output to reach and overcome the main supply voltage, starting from a low condition forced during the trace period.
An integrated diode stops the rising of this output increase and voltage jump is transferred by means of capacitor Cf at the supply voltage pin of the power stage (pin 8).
When the current across the yoke changes its direction, the output of the flyback generation falls down to the main supply voltage and it is stopped by means of the saturated output darlington at a high level. At this time the flyback generator starts to supply the power amplifier output stage by a diode inside the device. The flyback generator supplies the yoke too.
Later, the increasing flyback current reaches the peak value and then the flyback time is completed: the trace period restarts. The output of the power amplifier (pin 7) falls under the main supply voltage and the output of the flyback generator is driven for a low state so allowing the flyback capacitor Cf to restore the energy lost during the retrace.

**Pin 3** is the output of the flyback generator that, when driven, jumps from low to high condition. An external capacitor Cf transfers the jump to pin 8 (see pin 8).

### Blanking generator and CRT protection

This circuit is a pulse shaper and its output goes high during the blanking period or for CRT protection.

## APPLICATION INFORMATION (continued)

The input is internally driven by the clock pulse that defines the width of the blanking time when a flyback pulse has been generated. If the flyback pulse is absent (short circuit or open circuit of the yoke), the blanking output remains high so allowing the CRT protection.

**Pin 1** is an open collector output where the blanking pulse is available.

### Voltage regulator

The main supply voltage $V_s$ is lowered and regulated internally to allow the required reference voltages for all the above described blocks.

**Pin 2** is the main supply voltage input $V_s$ (positive).
**Pin 5, 6, 15, 16** are the GND pins or the negative input of $V_s$.

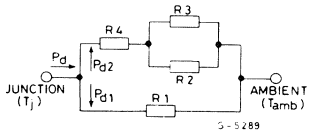
## THERMAL CONSIDERATIONS (a note referred to Fig. 3, 4 and 5)

The shown value of case to ambient thermal resistance is the equivalent to three thermal resistances that are:

R1 – Thermal resistance junction to ambient of the device.
R2 – Thermal resistance of the p.c. copper side.
R3 – Thermal resistance of the auxiliary heatsink.

The circuit that contains these thermal resistances is shown on fig. 7 where R3 is the thermal resistance junction to pins of the device and Pd is the maximum dissipated power.

Fig. 7 - Semiconductor heatsink thermal circuit.




Since the thermal resistance R3 of the heatsink is defined from its physical and mechanical characteristics, it is necessary to define the required copper side on the p.c. board for the necessary R2 value. For instance, let's consider the application for the 90° yoke.
It is known:

$T_{j\ max} = 130°C$; $T_{amb\ max} = 60°C$; $R_{th\ c\text{-}amb} = 8°C/W$; $R_{th\ j\text{-}pins}$ (or R4) $= 14°C/W$; $R_{th\ j\text{-}amb} = 80°C/W$.

It can be calculated:

$$P_d = \frac{T_{j\ max} - T_{amb\ max}}{R_{th\ c\text{-}amb} + R_{th\ j\text{-}pins}} = \frac{130 - 60}{8 + 14} = 3.18W$$

Using an auxiliary heatsink of a thermal resistance R3= 20°C/W (including some losses), it can be easily calculated (see fig. 7): R2 = 94°C/W.
From fig. 9, it can be found: $\ell \geqslant 21$ mm.

## MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the TDA 1770 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 8) or to an external heatsink.
The diagram of figure 9 shows the $R_{th}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 8 - Example of P.C. board copper area which is used as heatsink.

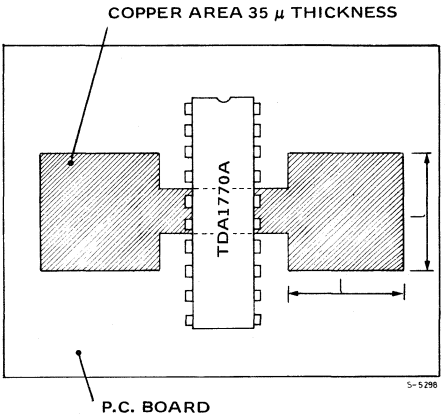



Fig. 9 - Thermal resistance of the P.C. copper side vs. side "ℓ"

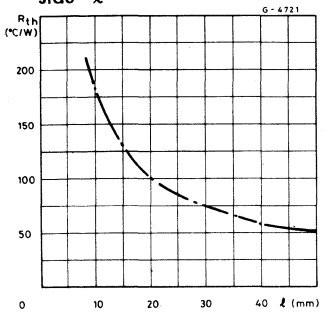
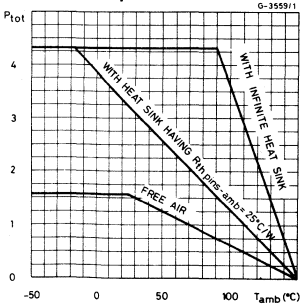



Fig. 10 - Maximum allowable power dissipation vs. ambient temperature



# TDA1904

# LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

## 4W AUDIO AMPLIFIER

- HIGH OUTPUT CURRENT CAPABILITY (UP TO 2A)
- PROTECTION AGAINST CHIP OVERTEMPERATURE
- LOW NOISE
- HIGH SUPPLY VOLTAGE REJECTION
- SUPPLY VOLTAGE RANGE: 4V TO 20V

The TDA 1904 is a monolithic integrated circuit in POWERDIP package intended for use as low-frequency power amplifier in a wide range of applications in portable radio and TV sets.

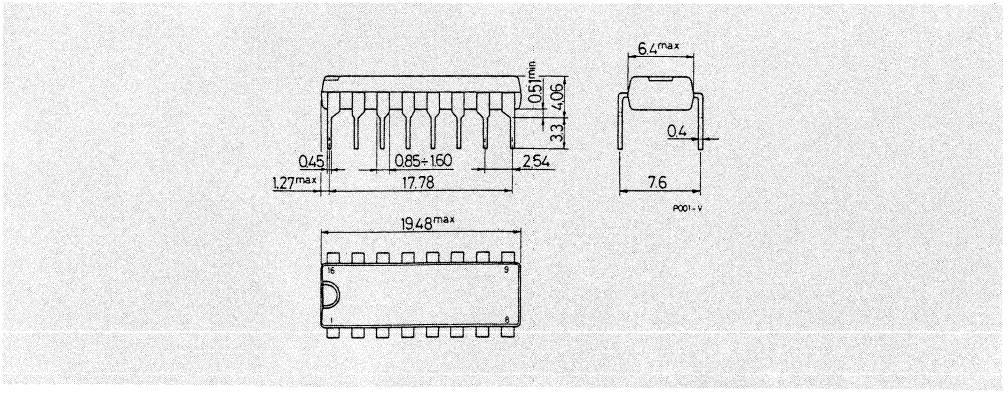
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 20 | V |
| $I_o$ | Peak output current (non repetitive) | 2.5 | A |
| $I_o$ | Peak output current (repetitive) | 2 | A |
| $P_{tot}$ | Total power dissipation at $T_{amb} = 80°C$ | 1 | W |
| | $T_{case} = 60°C$ | 6 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

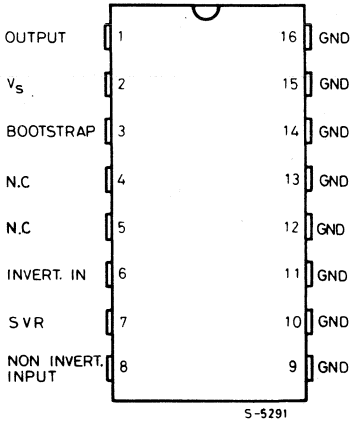
**ORDERING NUMBER:** TDA 1904

## MECHANICAL DATA

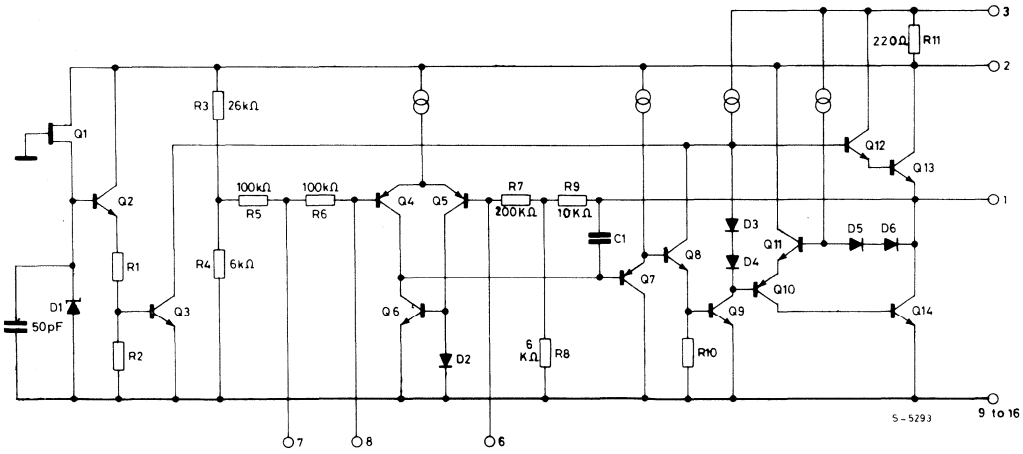
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## SCHEMATIC DIAGRAM




## THERMAL DATA

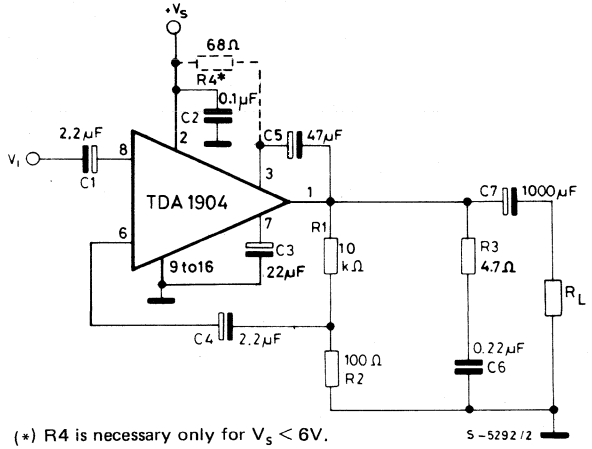
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-pins | max | 15 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb}$= 25°C, $R_{th}$ (heatsink) = 20°C/W, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 4 | | 20 | V |
| $V_o$ | Quiescent output voltage | $V_s$ = 4V<br>$V_s$ = 14V | | 2.1<br>7.2 | | V |
| $I_d$ | Quiescent drain current | $V_s$ = 9V<br>$V_s$ = 14V | | 8<br>10 | 18<br>20 | mA |
| $P_o$ | Output power | d = 10% f = 1 KHz<br>$V_s$ = 9V $R_L$ = 4Ω<br>$V_s$ = 14V<br>$V_s$ = 12V<br>$V_s$ = 6V | 1.8<br>4<br>3.1<br>0.7 | 2<br>4.5 | | W |
| d | Harmonic distortion | f = 1 KHz<br>$V_s$ = 9V $R_L$ = 4Ω<br>$P_o$ = 50 mW to 1.2W | | 0.1 | 0.3 | % |
| $V_i$ | Input saturation voltage (rms) | $V_s$ = 9V<br>$V_s$ = 14V | 0.8<br>1.3 | | | V |
| $R_i$ | Input resistance (pin 8) | f = 1 KHz | 55 | 150 | | KΩ |
| $\eta$ | Efficiency | f = 1 KHz<br>$V_s$ = 9V $R_L$ = 4Ω $P_o$ = 2W<br>$V_s$ = 14V $R_L$ = 4Ω $P_o$ = 4.5W | | 70<br>65 | | % |
| BW | Small signal bandwidth (-3 dB) | $V_s$ = 14V $R_L$ = 4Ω | 40 to 40,000 | | | Hz |
| $G_v$ | Voltage gain (open loop) | $V_s$ = 14V<br>f = 1 KHz | | 75 | | dB |
| $G_v$ | Voltage gain (closed loop) | $V_s$ = 14V $R_L$ = 4Ω<br>f = 1 KHz $P_o$ = 1W | 39.5 | 40 | 40.5 | dB |
| $e_N$ | Total input noise | $R_g$ = 50Ω<br>$R_g$ = 10 KΩ (°) | | 1.2<br>2 | 4 | μV |
| | | $R_g$ = 50Ω<br>$R_g$ = 10 KΩ (°°) | | 2<br>3 | | μV |
| SVR | Supply voltage rejection | $V_s$ = 12V<br>$f_{ripple}$= 100 Hz $R_g$ = 10 KΩ<br>$V_{ripple}$= 0.5Vrms | 40 | 50 | | dB |
| $T_{sd}$ | Thermal shut-down case temperature | $P_{tot}$= 2W | | 120 | | °C |

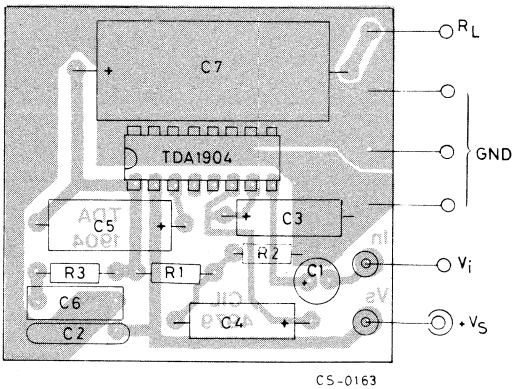
**Note:** (°) Weighting filter = curve A.
(°°) Filter with noise bendwidth: 22 Hz to 22 KHz.

Fig. 1 - Test and application circuit




(*) R4 is necessary only for $V_S < 6V$.

Fig. 2 - P.C. board and components layout of fig. 1 (1:1 scale)



## APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 1. When the supply voltage $V_s$ is less than 6V, a 68Ω resistor must be connected between pin 2 and pin 3 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

| Components | Recomm. value | Purpose | Larger than recommended value | Smaller than recommended value | Allowed range | |
|---|---|---|---|---|---|---|
| | | | | | Min. | Max. |
| R1 | 10 KΩ | Feedback resistors | Increase of gain. | Decrease of gain. Increase quiescent current. | 9 R3 | |
| R2 | 100 Ω | | Decrease of gain. | Increase of gain. | | 1 KΩ |
| R3 | 4.7 Ω | Frequency stability | Danger of oscillation at high frequencies with inductive loads. | | | |
| R4 | 68 Ω | Increase of the output swing with low supply voltage. | | | 39 Ω | 220 Ω |
| C1 | 2.2 μF | Input DC decoupling. | Higher cost lower noise. | Higher low frequency cutoff. Higher noise. | | |
| C2 | 0.1 μF | Supply voltage bypass. | | Danger of oscillations. | | |
| C3 | 22 μF | Ripple rejection | Increase of SVR increase of the switch-on time. | Degradation of SVR. | 2.2 μF | 100μF |
| C4 | 2.2 μF | Inverting input DC decoupling. | Increase of the switch-on noise | Higher low frequency cutoff. | 0.1 μF | |
| C5 | 47 μF | Bootstrap. | | Increase of the distortion at low frequency. | 10 μF | 100μF |
| C6 | 0.22 μF | Frequency stability. | | Danger of oscillation. | | |
| C7 | 1000 μF | Output DC decoupling. | | Higher low frequency cutoff. | | |

## THERMAL SHUT-DOWN

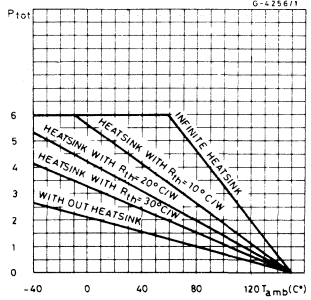
The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the $T_j$ cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 3 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 3 - Maximum allowable power dissipation vs. ambient temperature




## MOUNTING INSTRUCTION

The TDA 1904 is assembled in the Powerdip, in which 8 pins (from 9 to 16) are attached to the frame and remove the heat produced by the chip.

Figure 4 and 5 show two ways of heatsinking. In the first case, a PC board copper area is used as a heatsink l = 65 mm. while in the second case, the device is soldered to an external heatsink.
In both examples, the thermal resistance junction-ambient is 35°C/W.

Fig. 4 - Example of heatsink using PC board copper (l = 65 mm)

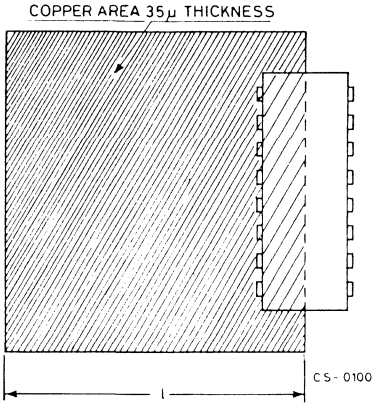
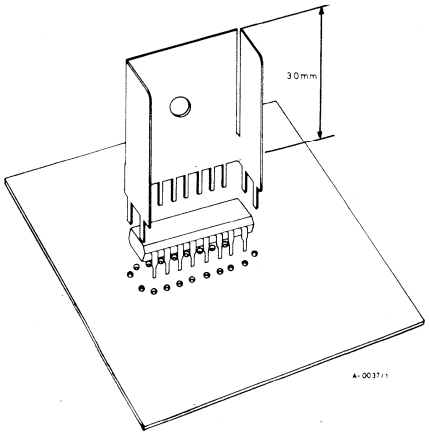



Fig. 5 - Example of an external heatsink.



## 5W AUDIO AMPLIFIER WITH MUTING

The TDA 1905 is a monolithic integrated circuit in POWERDIP package, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets.
Its main features are:

- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise
- voltage range 4V to 30V

The TDA 1905 is assembled in a new plastic package, the POWERDIP, that offers the same assembly ease, space and cost saving of a normal dual in-line package but with a power dissipation of up to 6W and a thermal resistance of 15°C/W (junction to pins).

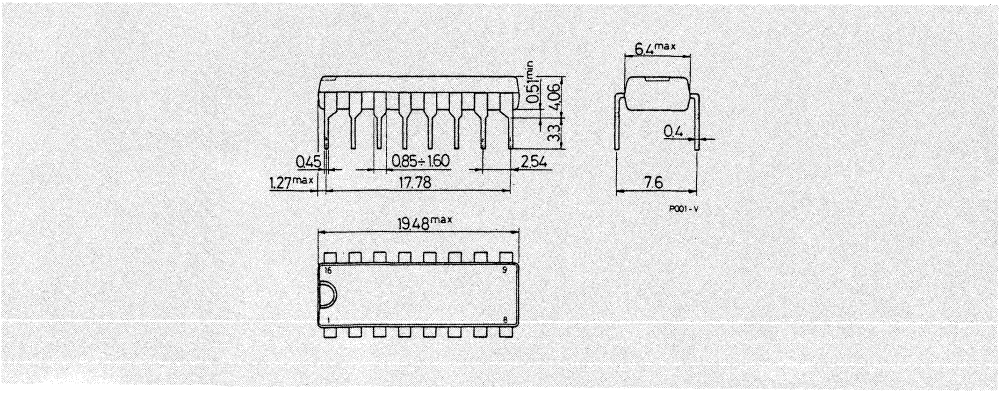
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 30 | V |
| $I_o$ | Output peak current (non repetitive) | 3 | A |
| $I_o$ | Output peak current (repetitive) | 2.5 | A |
| $V_i$ | Input voltage | 0 to + $V_s$ | V |
| $V_i$ | Differential input voltage | ± 7 | V |
| $V_{11}$ | Muting thresold voltage | $V_s$ | V |
| $P_{tot}$ | Power dissipation at $T_{amb}$ = 80°C | 1 | W |
| | $T_{case}$ = 60°C | 6 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA 1905

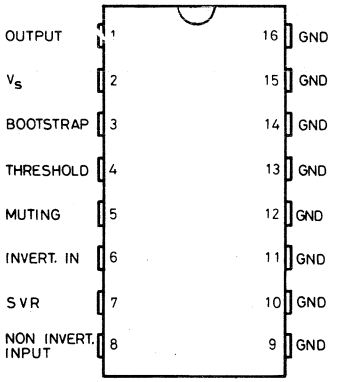
## MECHANICAL DATA

Dimensions in mm

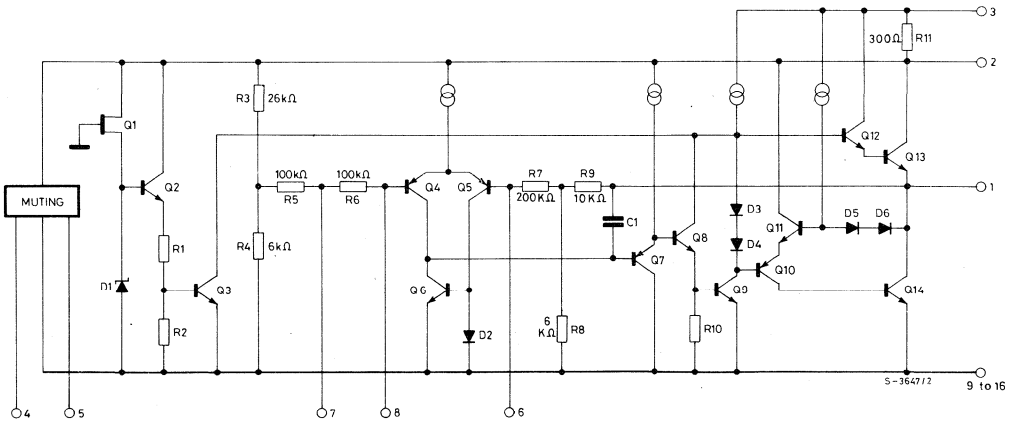


## CONNECTION DIAGRAM

(Top view)



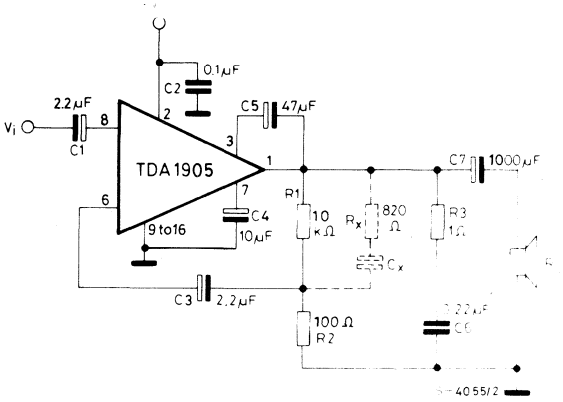

## SCHEMATIC DIAGRAM



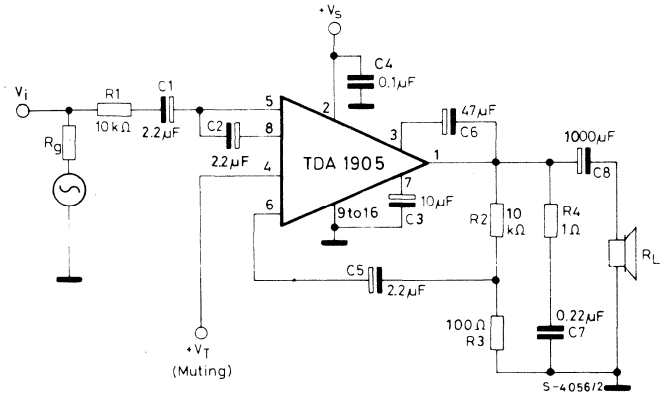

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\,j\text{-}case}$ | Thermal resistance junction-pins | max | 15 | °C/W |
| $R_{th\,j\text{-}amb}$ | Thermal resistance junction-amb | max | 70 | °C/W |

## TEST CIRCUIT




## MUTING CIRCUIT



## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb}$ = 25°C, $R_{th}$ (heatsink) = 20°C/W, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 4 | | 30 | V |
| $V_o$ | Quiescent output voltage | $V_s$ = 4V<br>$V_s$ = 14V<br>$V_s$ = 30V | 1.6<br>6.7<br>14.4 | 2.1<br>7.2<br>15.5 | 2.5<br>7.8<br>16.8 | V |
| $I_d$ | Quiescent drain current | $V_s$ = 4V<br>$V_s$ = 14V<br>$V_s$ = 30V | | 15<br>17<br>21 | <br><br>35 | mA |
| $V_{CE\ sat}$ | Output stage saturation voltage | $I_C$ = 1A<br>$I_C$ = 2A | | 0.5<br>1 | | V |
| $P_o$ | Output power | d = 10% f = 1KHz<br>$V_s$ = 9V $R_L$ = 4Ω (*)<br>$V_s$ = 14V $R_L$ = 4Ω<br>$V_s$ = 18V $R_L$ = 8Ω<br>$V_s$ = 24V $R_L$ = 16Ω | <br>2.2<br>5<br>5<br>4.5 | <br>2.5<br>5.5<br>5.5<br>5.3 | | W |
| d | Harmonic distortion | f = 1KHz<br>$V_s$ = 9V $R_L$ = 4Ω<br>$P_o$ = 50 mW to 1.5W<br>$V_s$ = 14V $R_L$ = 4Ω<br>$P_o$ = 50 mW to 3W<br>$V_s$ = 18V $R_L$ = 8Ω<br>$P_o$ = 50 mW to 3W<br>$V_s$ = 24V $R_L$ = 16Ω<br>$P_o$ = 50 mW to 3W | | <br>0.1<br>0.1<br>0.1<br>0.1 | | % |
| $V_i$ | Input sensitivity | f = 1KHz<br>$V_s$ = 9V $R_L$ = 4Ω $P_o$ = 2.5W<br>$V_s$ = 14V $R_L$ = 4Ω $P_o$ = 5.5W<br>$V_s$ = 18V $R_L$ = 8Ω $P_o$ = 5.5W<br>$V_s$ = 24V $R_L$ = 16Ω $P_o$ = 5.3W | | <br>37<br>49<br>73<br>100 | | mV |
| $V_i$ | Input saturation voltage (rms) | $V_s$ = 9V<br>$V_s$ = 14V<br>$V_s$ = 18V<br>$V_s$ = 24V | 0.8<br>1.3<br>1.8<br>2.4 | | | V |
| $R_i$ | Input resistance (pin 8) | f = 1KHz | 60 | 100 | | KΩ |
| $I_d$ | Drain current | f = 1KHz<br>$V_s$ = 9V $R_L$ = 4Ω $P_o$ = 2.5W<br>$V_s$ = 14V $R_L$ = 4Ω $P_o$ = 5.5W<br>$V_s$ = 18V $R_L$ = 8Ω $P_o$ = 5.5W<br>$V_s$ = 24V $R_L$ = 16Ω $P_o$ = 5.3W | | <br>380<br>550<br>410<br>295 | | mA |
| $\eta$ | Efficiency | f = 1KHz<br>$V_s$ = 9V $R_L$ = 4Ω $P_o$ = 2.5W<br>$V_s$ = 14V $R_L$ = 4Ω $P_o$ = 5.5W<br>$V_s$ = 18V $R_L$ = 8Ω $P_o$ = 5.5W<br>$V_s$ = 24V $R_L$ = 16Ω $P_o$ = 5.3W | | <br>73<br>71<br>74<br>75 | | % |

(*) With an external resistor of 100Ω between pin 3 and $+V_s$.

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| BW | Small signal bandwidth (-3dB) | $V_s$ = 14V $R_L$ = 4Ω $P_o$ = 1W | | | 40 to 40,000 | | Hz |
| $G_v$ | Voltage gain (open loop) | $V_s$ = 14V<br>f = 1KHz | | | 75 | | dB |
| $G_v$ | Voltage gain (closed loop) | $V_s$ = 14V $R_L$ = 4Ω<br>f = 1KHz $P_o$ = 1W | | 39.5 | 40 | 40.5 | dB |
| $e_N$ | Total input noise | | $R_g$ = 50Ω<br>$R_g$ = 1KΩ<br>$R_g$ = 10KΩ (°) | | 1.2<br>1.3<br>1.5 | 4.0 | μV |
| | | | $R_g$ = 50Ω<br>$R_g$ = 1KΩ<br>$R_g$ = 10KΩ (°°) | | 2.0<br>2.0<br>2.2 | 6.0 | μV |
| S/N | Signal to noise ratio | $V_s$ = 14V<br>$P_o$ = 5.5W<br>$R_L$ = 4Ω | $R_g$ = 10KΩ<br>$R_g$ = 0 (°) | | 90<br>92 | | dB |
| | | | $R_g$ = 10KΩ<br>$R_g$ = 0 (°°) | | 87<br>87 | | dB |
| SVR | Supply voltage rejection | $V_s$ = 18V $R_L$ = 8Ω<br>$f_{ripple}$ = 100 Hz $R_g$ = 10KΩ<br>$V_{ripple}$ = 0.5Vrms | | 40 | 50 | | dB |
| $T_{sd}$ | Thermal shut-down (*)<br>case temperature | $P_{tot}$ = 2.5W | | | 115 | | °C |

## MUTING FUNCTION (Refer to Muting circuit)

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{T_{OFF}}$ | Muting-off threshold voltage (pin 4) | | 1.9 | | 4.7 | V |
| $V_{T_{ON}}$ | Muting-on threshold voltage (pin 4) | | 0 | | 1.3 | V |
| | | | 6.2 | | $V_s$ | |
| $R_5$ | Input resistance (pin 5) | Muting off | 80 | 200 | | KΩ |
| | | Muting on | | 10 | 30 | Ω |
| $R_4$ | Input resistance (pin 4) | | 150 | | | KΩ |
| $A_T$ | Muting attenuation | $R_g + R_1$ = 10KΩ | 50 | 60 | | dB |

**Note:**
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 30 and fig. 31

Fig. 1 - Quiescent output voltage vs. supply voltage

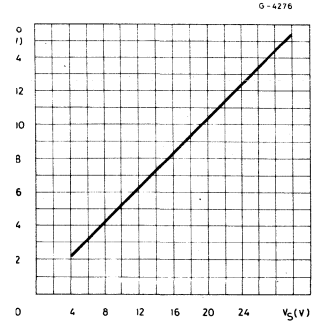



Fig. 2 - Quiescent drain current vs. supply voltage

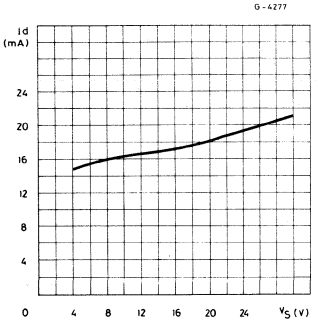



Fig. 3 - Output power vs. supply voltage

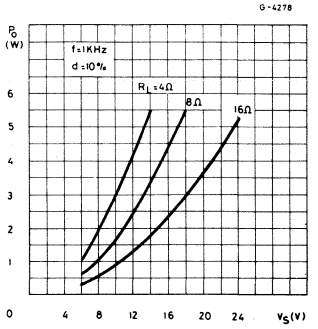



Fig. 4 - Distortion vs. output power ($R_L = 16\Omega$)

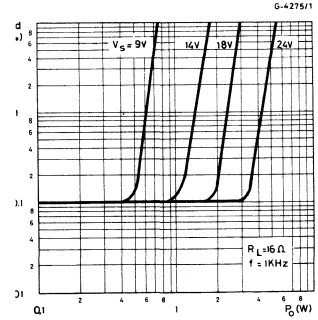



Fig. 5 - Distortion vs. output power ($R_L = 8\Omega$)

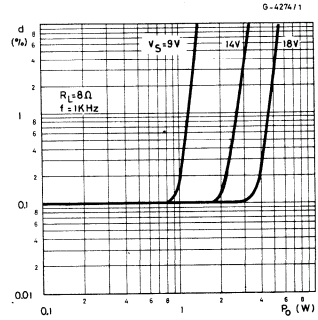



Fig. 6 - Distortion vs. output power ($R_L = 4\Omega$)

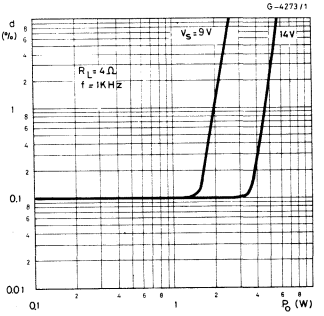



Fig. 7 - Distortion vs. frequency ($R_L = 16\Omega$)

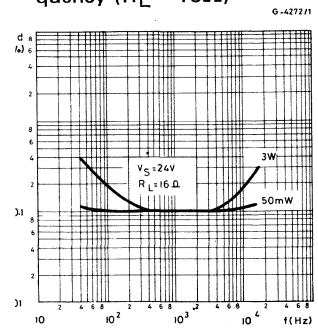



Fig. 8 - Distortion vs. frequency ($R_L = 8\Omega$)

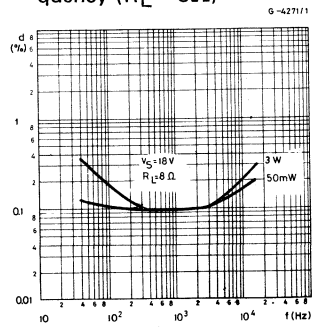



Fig. 9 - Distortion vs. frequency ($R_L = 4\Omega$)

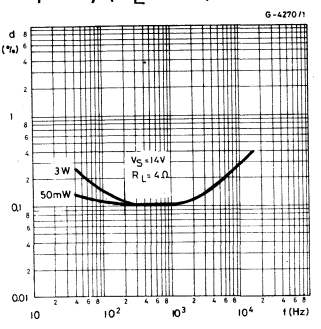


Fig. 10 - Open loop frequency response

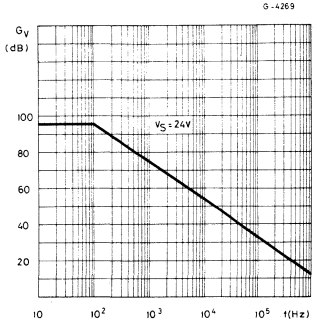



Fig. 11 - Output power vs. input voltage

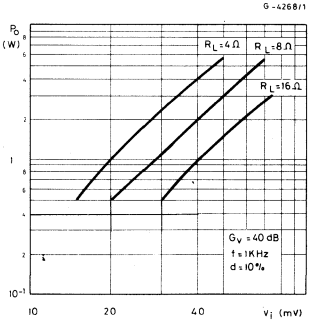



Fig. 12 - Value of capacitor Cx vs. bandwidth (BW) and gain (Gv)

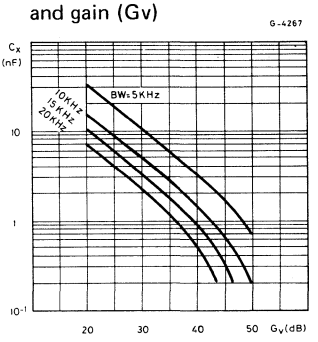



Fig. 13 - Supply voltage rejection vs. voltage gain (ref. to the Muting circuit)

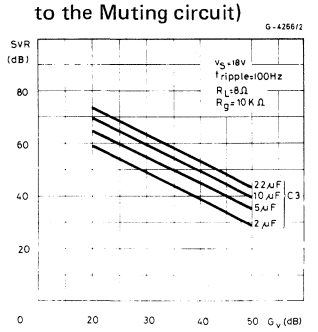



Fig. 14 - Supply voltage rejection vs. source resistance

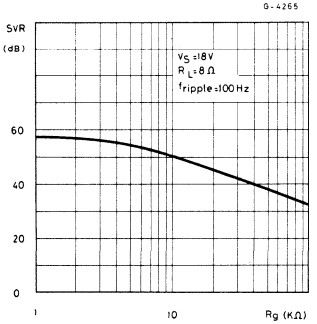



Fig. 15 - Max power dissipation vs. supply voltage (sine wave operation)

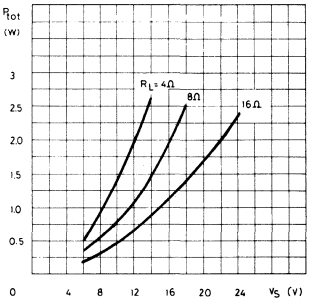



Fig. 16 - Power dissipation and efficiency vs. output power

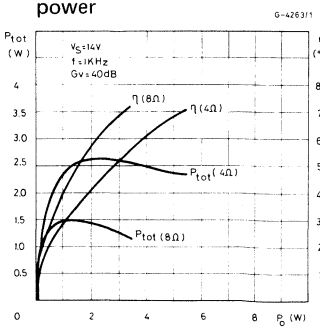



Fig. 17 - Power dissipation and efficiency vs. output power

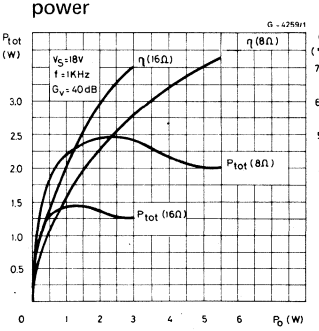
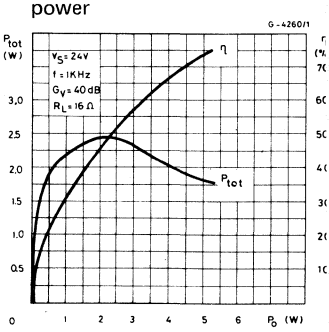
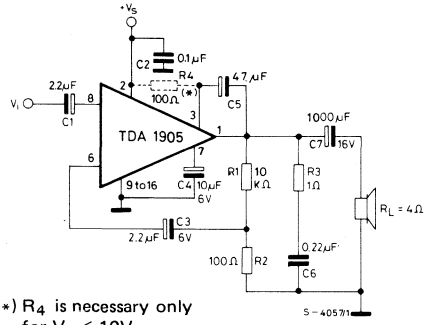



Fig. 18 - Power dissipation and efficiency vs. output power



## APPLICATION INFORMATION

Fig. 19 - Application circuit without muting




(*) $R_4$ is necessary only for $V_s < 10V$.

$P_o = 5.5W$ (d = 10%)
$V_s = 14V$
$I_d = 0.55A$
$G_v = 40$ dB

Fig. 20 - PC board and components lay-out of the circuit of fig. 19 (1:1 scale)

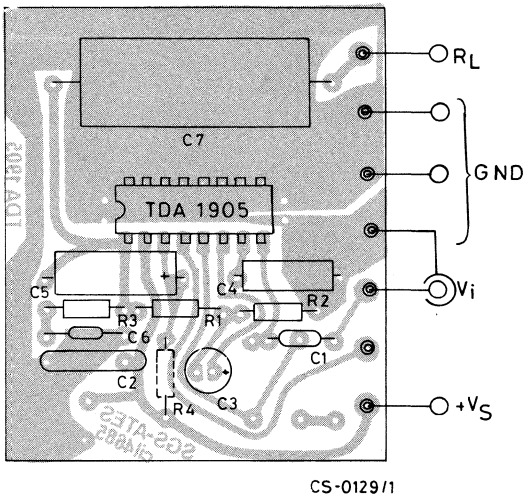



Fig. 21 - Application circuit with muting

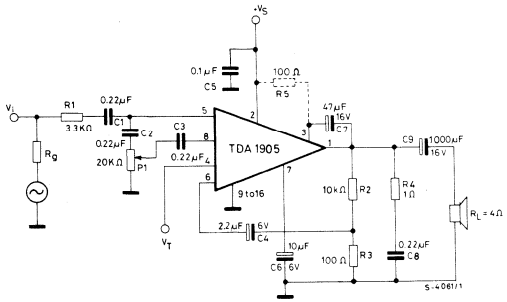
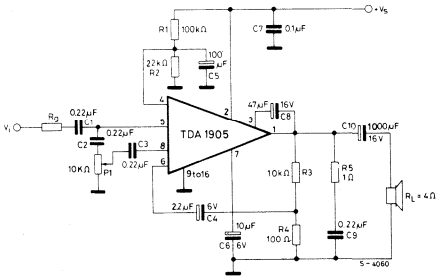



Fig. 22 - Delayed muting circuit



## APPLICATION INFORMATION (continued)

Fig. 23 - Low-cost application circuit without bootstrap.

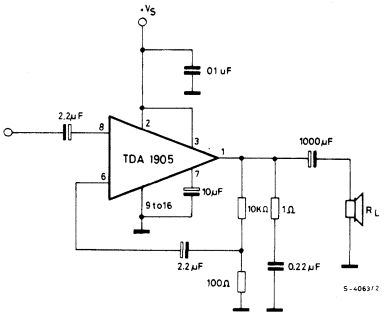



Fig. 24 - Output power vs. supply voltage (circuit of fig. 23)

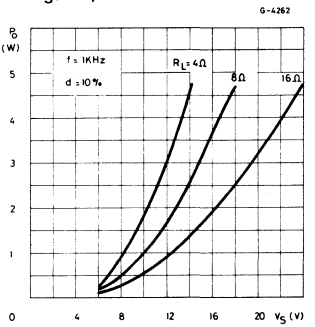



Fig. 25 - Two position DC tone control using change of pin 5 resistance (muting function)

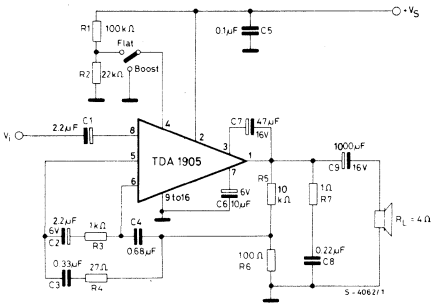



Fig. 26 - Frequency response of the circuit of fig. 25

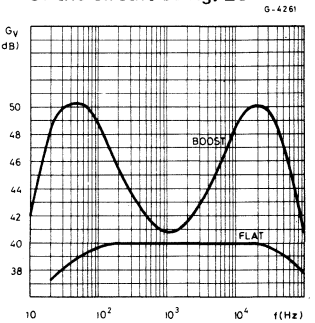



Fig. 27 - Bass Bomb tone control using change of pin 5 resistance (muting function)

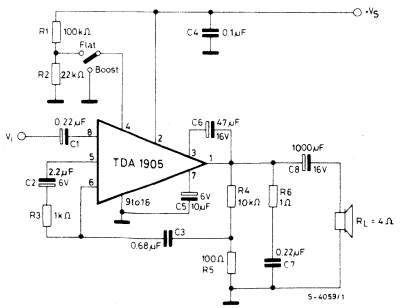
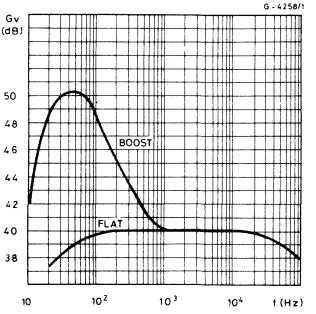


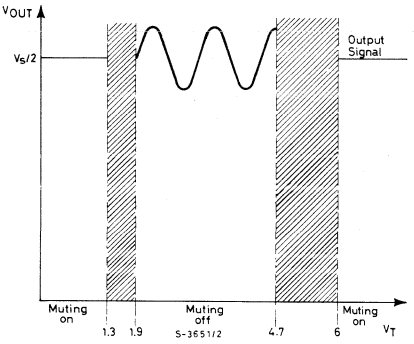

Fig. 28 - Frequency response of the circuit of fig. 27



## MUTING FUNCTION

The output signal can be inhibited applying a DC voltage $V_T$ to pin 4, as shown in fig. 29

Fig. 29

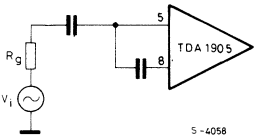



The input resistance at pin 5 depends on the threshold voltage $V_T$ at pin 4 and is typically:

$R_5 = 200\ K\Omega$ @ $1.9V \leqslant V_T \leqslant 4.7V$ muting-off

$R_5 = 10\Omega$ @ $0V \leqslant V_T \leqslant 1.3V$, $6V \leqslant V_T \leqslant V_s$ muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression:




$$A_T = \frac{V_i}{V_8} = \frac{R_g + \left(\frac{R_8 \cdot R_5}{R_8 + 5}\right)}{\left(\frac{R_8 \cdot R_5}{R_8 + R_5}\right)}$$

where $R_8 \cong 100\ K\Omega$

Considering $R_g = 10\ K\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, tipically 1.2 dB.
A very low current is necessary to drive the threshold voltage $V_T$ because the input resistance at pin 4 is greater than 150 $K\Omega$. The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients (see fig. 22)
- during switching at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 5 can be useful in many application and two examples are shown in fig. 25 and 27, where it has been used to change the feedback network, obtaining 2 different frequency response.

## APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 21. When the supply voltage $V_s$ is less than 10V, a 100Ω resistor must be connected between pin 2 and pin 3 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

| Component | Raccom. value | Purpose | Larger than recommended value | Smaller than recommended value | Allowed range Min. | Max. |
|---|---|---|---|---|---|---|
| $R_g + R_1$ | 10KΩ | Input signal imped. for muting operation | Increase of the attenuation in muting-on condition. Decrease of the input sensitivity. | Decrease of the attenuation in muting on condition. | | |
| $R_2$ | 10KΩ | Feedback resistors | Increase of gain. | Decrease of gain. Increase quiescent current. | $9\,R_3$ | |
| $R_3$ | 100Ω | | Decrease of gain. | Increase of gain. | | 1KΩ |
| $R_4$ | 1Ω | Frequency stability | Danger of oscillation at high frequencies with inductive loads. | | | |
| $R_5$ | 100Ω | Increase of the output swing with low supply voltage. | | | 47 | 330 |
| $P_1$ | 20KΩ | Volume potentiometer | Increase of the switch-on noise. | Decrease of the input impedance and of the input level. | 10KΩ | 100KΩ |
| $C_1$ $C_2$ $C_3$ | 0.22 μF | Input DC decoupling. | Higher cost lower noise. | Higher low frequency cutoff. Higher noise | | |
| $C_4$ | 2.2μF | Inverting input DC decoupling. | Increase of the switch-on noise. | Higher low frequency cutoff. | 0.1μF | |
| $C_5$ | 0.1μF | Supply voltage bypass. | | Danger of oscillations. | | |
| $C_6$ | 10 μF | Ripple rejection | Increase of SVR increase of the switch-on time | Degradation of SVR | 2.2 μF | 100 μF |
| $C_7$ | 47μF | Bootstrap. | | Increase of the distortion at low frequency. | 10μF | 100μF |
| $C_8$ | 0.22μF | Frequency stability. | | Danger of oscillation. | | |
| $C_9$ | 1000 μF | Output DC decoupling. | | Higher low frequency cutoff. | | |

## THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily tolerated since the $T_j$ cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 32 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 30 - Output power and drain current vs. case temperature.

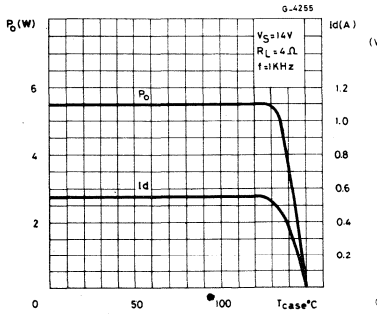



Fig. 31 - Output power and drain current vs. case temperature

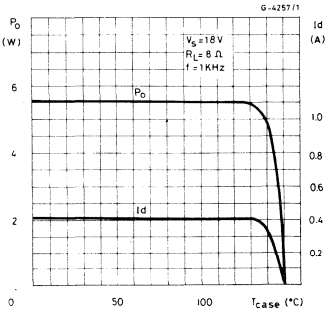
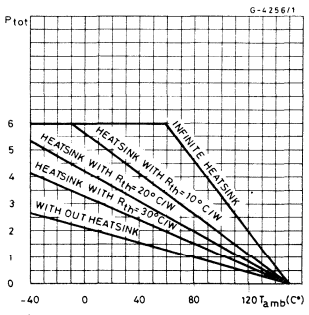



Fig. 32 - Maximum allowable power dissipation vs. ambient temperature.



## MOUNTING INSTRUCTION

The TDA 1905 is assembled in a new plastic package, the Powerdip, in which 8 pins (from 9 to 16) are attached to the frame and remove the heat produced by the chip.

Figure 33 and 34 show two ways of heatsinking. In the first case, a PC board copper area is used as a heatsink l = 65 mm. while in the second case, the device is soldered to an external heatsink.
In both examples, the thermal resistance junction-ambient is 35°C/W.

Fig. 33 - Example of heatsink using PC board copper (l = 65 mm)

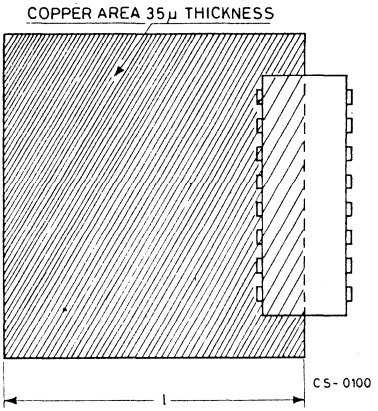
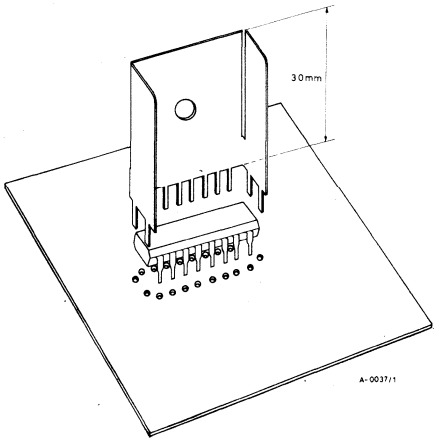



Fig. 34 - Example of an external heatsink



## 8W AUDIO AMPLIFIER

The TDA 1908 is a monolithic integrated circuit in 12 lead quad in-line plastic package intended for low frequency power applications. The mounting is compatible with the old types TBA 800, TBA 810S, TCA 830S and TCA 940N. Its main features are:

- flexibility in use with a max output current of 3A and an operating supply voltage range of 4V to 30V
- protection against chip overtemperature
- soft limiting in saturation conditions
- low "switch-on" noise
- low number of external components
- high supply voltage rejection
- very low noise

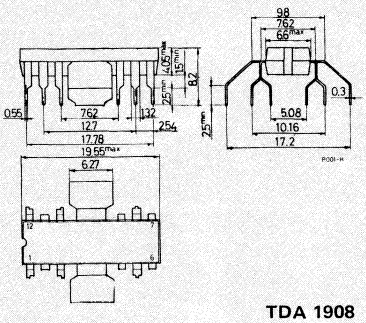
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 30 | V |
| $I_o$ | Output peak current (non repetitive) | 3.5 | A |
| $I_o$ | Output peak current (repetitive) | 3 | A |
| $P_{tot}$ | Power dissipation: at $T_{amb}$= 80°C (TDA 1908) | 1 | W |
| | at $T_{tab}$ = 100°C (TDA 1908A) | 5 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

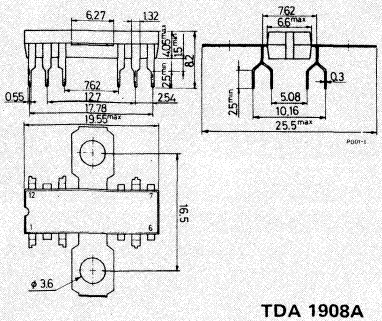
**ORDERING NUMBERS:** TDA 1908, TDA 1908A

## MECHANICAL DATA

Dimensions in mm



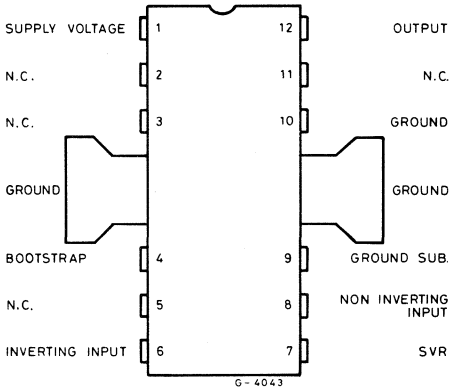

TDA 1908



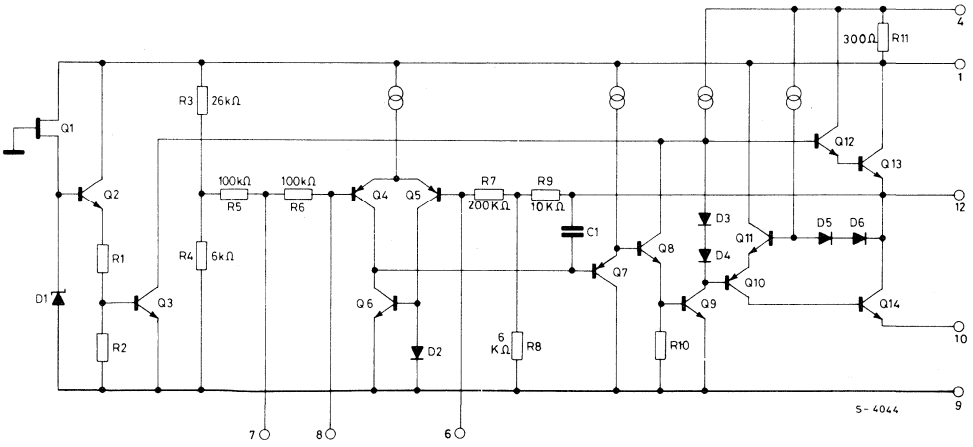

TDA 1908A

# TDA1908

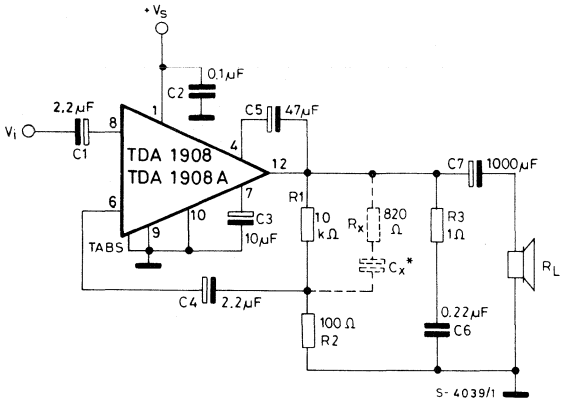
## CONNECTION DIAGRAM
(top view)




## SCHEMATIC DIAGRAM



## TEST CIRCUIT




* See fig. 12.

## THERMAL DATA

| | | | TDA 1908 | TDA 1980A |
|---|---|---|---|---|
| $R_{th\ j\text{-}tab}$ | Thermal resistance junction-tab | max | 12 °C/W | 10 °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-amb | max | (°) 70 °C/W | 80 °C/W |

(°) Obtained with tabs soldered to printed circuit board with min copper area.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb}$= 25°C, $R_{th}$ (heatsink)= 8 °C/W, unless otherwise specified)

| Parameter | | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 4 | | 30 | V |
| $V_o$ | Quiescent output voltage | $V_s$ = 4V<br>$V_s$ = 18V<br>$V_s$ = 30V | 1.6<br>8.2<br>14.4 | 2.1<br>9.2<br>15.5 | 2.5<br>10.2<br>16.8 | V |
| $I_d$ | Quiescent drain current | $V_s$ = 4V<br>$V_s$ = 18V<br>$V_s$ = 30V | | 15<br>17.5<br>21 | <br><br>35 | mA |
| $V_{CEsat}$ | Output stage saturation voltage (each output transistor) | $I_C$= 1A<br>$I_C$= 2.5A | | 0.5<br>1.3 | | V |
| $P_o$ | Output power | d = 10% f = 1 KHz<br>$V_s$ = 9V $R_L$= 4Ω<br>$V_s$ = 14V $R_L$= 4Ω<br>$V_s$ = 18V $R_L$= 4Ω<br>$V_s$ = 22V $R_L$= 8Ω<br>$V_s$ = 24V $R_L$= 16Ω | <br><br><br>7<br>6.5<br>4.5 | <br>2.5<br>5.5<br>9<br>8<br>5.3 | | W |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test condition | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| d | Harmonic distortion | f = 1KHz<br>$V_s$ = 9V $R_L$ = 4Ω<br>$P_o$ = 50 mW to 1.5W<br>$V_s$ = 18V $R_L$ = 4Ω<br>$P_o$ = 50 mW to 4W<br>$V_s$ = 24V $R_L$ = 16Ω<br>$P_o$ = 50 mW to 3W | | 0.1<br>0.1<br>0.1 | | % |
| $V_i$ | Input sensitivity | $V_s$ = 9V $R_L$ = 4Ω $P_o$ = 2.5W<br>$V_s$ = 14V $R_L$ = 4Ω $P_o$ = 5.5W<br>$V_s$ = 18V $R_L$ = 4Ω $P_o$ = 9W<br>$V_s$ = 22V $R_L$ = 8Ω $P_o$ = 8W<br>$V_s$ = 24V $R_L$ = 16Ω $P_o$ = 5.3W | | 37<br>52<br>64<br>90<br>110 | | mV |
| $V_i$ | Input saturation voltage (rms) | $V_s$ = 9V<br>$V_s$ = 14V<br>$V_s$ = 18V<br>$V_s$ = 24V | 0.8<br>1.3<br>1.8<br>2.4 | | | V |
| $R_i$ | Input resistance (pin 8) | f = 1 KHz | 60 | 100 | | KΩ |
| $I_s$ | Drain current | f = 1 KHz<br>$V_s$ = 14V $R_L$ = 4Ω $P_o$ = 5.5W<br>$V_s$ = 18V $R_L$ = 4Ω $P_o$ = 9W<br>$V_s$ = 22V $R_L$ = 8Ω $P_o$ = 8W<br>$V_s$ = 24V $R_L$ = 16Ω $P_o$ = 5.3W | | 570<br>730<br>500<br>310 | | mA |
| η | Efficiency | $V_s$ = 18V f = 1 KHz<br>$R_L$ = 4Ω $P_o$ = 9W | | 72 | | % |
| BW | Small signal bandwidth (-3 dB) | $V_s$ = 18V $R_L$ = 4Ω $P_o$ = 1W | 40 to 40 000 | | | Hz |
| $G_v$ | Voltage gain (open loop) | f = 1 KHz | | 75 | | dB |
| $G_v$ | Voltage gain (closed loop) | $V_s$ = 18V $R_L$ = 4Ω<br>f = 1 KHz $P_o$ = 1W | 39.5 | 40 | 40.5 | dB |
| $e_N$ | Total input noise | (°) $R_g$ = 50Ω<br>$R_g$ = 1KΩ<br>$R_g$ = 10 KΩ | | 1.2<br>1.3<br>1.5 | 4.0 | μV |
| | | (°°) $R_g$ = 50Ω<br>$R_g$ = 1KΩ<br>$R_g$ = 10KΩ | | 2.0<br>2.0<br>2.2 | 6.0 | μV |
| S/N | Signal to noise ratio | $V_s$ = 18V $P_o$ = 9W $R_L$ = 4Ω; $R_g$ = 10KΩ $R_g$ = 0 (°) | | 92<br>94 | | dB |
| | | $V_s$ = 18V $P_o$ = 9W $R_L$ = 4Ω; $R_g$ = 10KΩ $R_g$ = 0 (°°) | | 88<br>90 | | dB |
| SVR | Supply voltage rejection | $V_s$ = 18V $R_L$ = 4Ω<br>$f_{ripple}$ = 100 Hz $R_g$ = 10KΩ | 40 | 50 | | dB |
| $T_{sd}$ | Thermal shut-down case temperature (*) | $P_{tot}$ = 4W | | 110 | | °C |

Note:
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 24 and fig. 25.

Fig. 1 - Quiescent output voltage vs. supply voltage

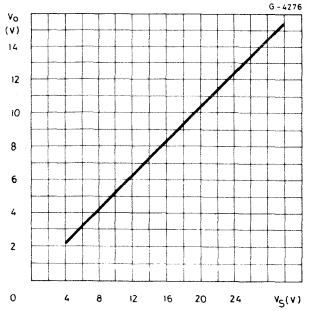



Fig. 2 - Quiescent drain current vs. supply voltage

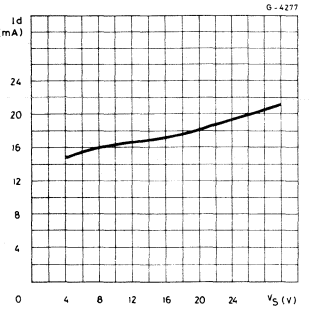



Fig. 3 - Output power vs. supply voltage

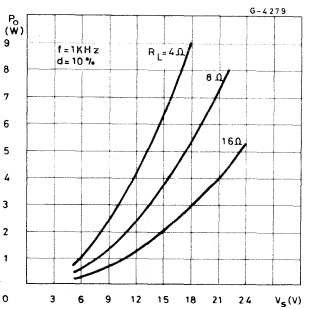



Fig. 4 - Distortion vs. output power ($R_L = 16\Omega$)

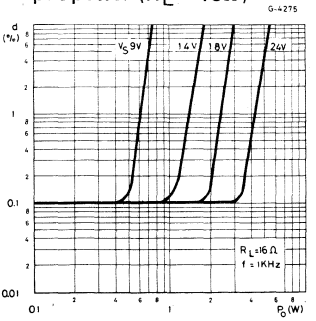



Fig. 5 - Distortion vs. output power ($R_L = 8\Omega$)

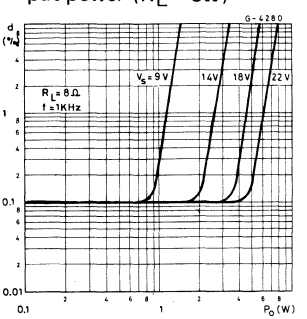



Fig. 6 - Distortion vs. output power ($R_L = 4\Omega$)

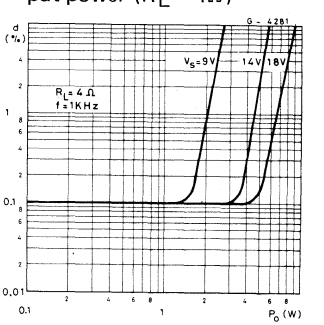



Fig. 7 - Distortion vs. frequency ($R_L = 16\Omega$)

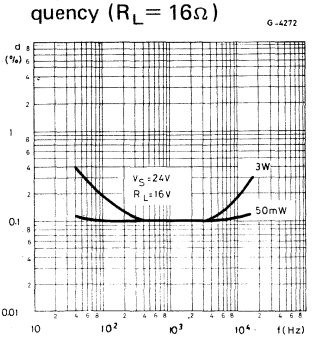



Fig. 8 - Distortion vs. frequency ($R_L = 8\Omega$)

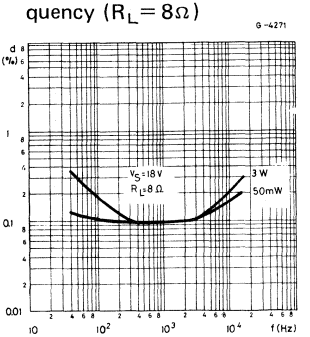



Fig. 9 - Distortion vs. frequency ($R_L = 4\Omega$)

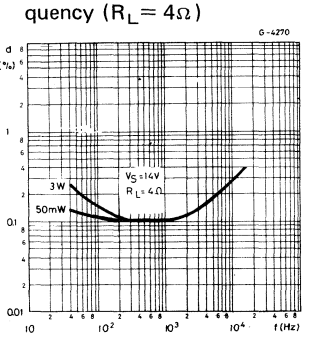


Fig. 10 - Open loop frequency response

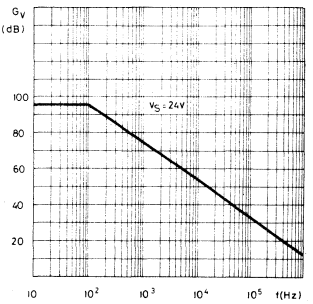



Fig. 11 - Output power vs. input voltage

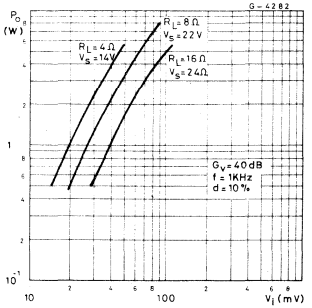



Fig. 12 - Values of capacitor $C_X$ versus gain and $B_W$

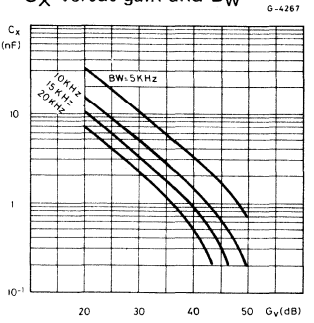



Fig. 13 - Supply voltage rejection vs. voltage gain

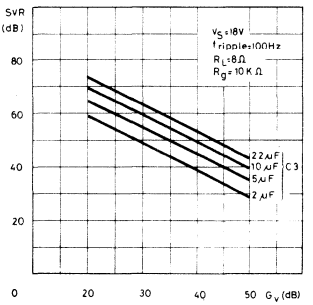



Fig. 14 - Supply voltage rejection vs. source resistance

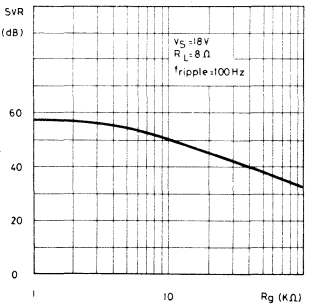



Fig. 15 - Max power dissipation vs. supply voltage

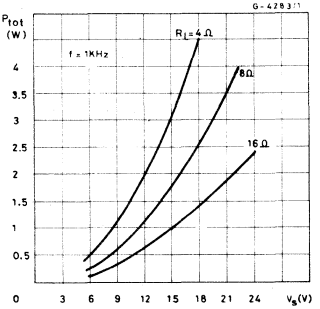



Fig. 16 - Power dissipation and efficiency vs. output power ($V_S$= 14V)

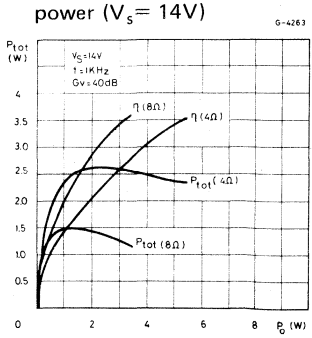



Fig. 17 - Power dissipation and efficiency vs. output power ($V_S$= 18V)

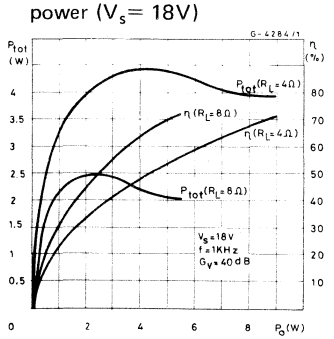
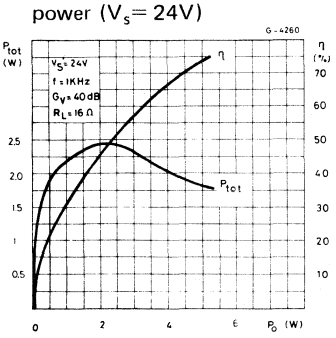
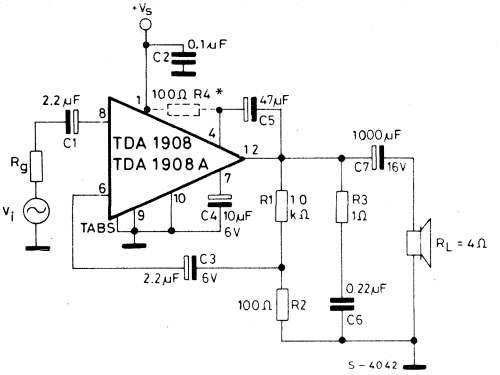



Fig. 18 - Power dissipation and efficiency vs. output power ($V_S$= 24V)



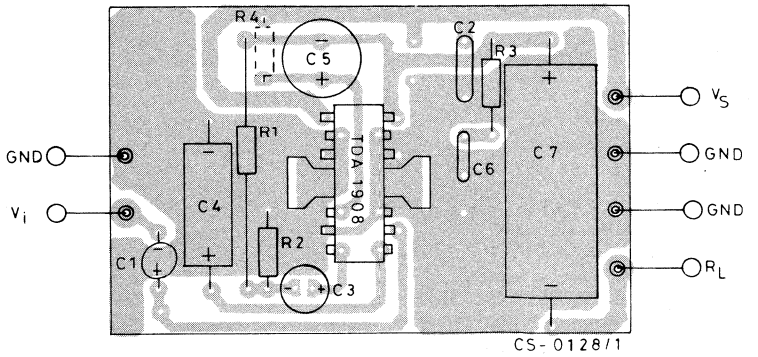
## APPLICATION INFORMATION

Fig. 19 - Application circuit with bootstrap




* R4 is necessary when $V_s$ is less than 10V.

Fig. 20 - P.C. board and component lay-out of the circuit of fig. 19 (1:1 scale)



## APPLICATION INFORMATION (continued)

Fig. 21 - Application circuit without bootstrap

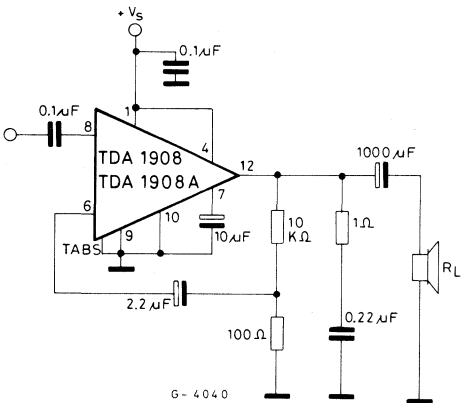



Fig. 22 - Output power vs. supply voltage (circuit of fig. 21)

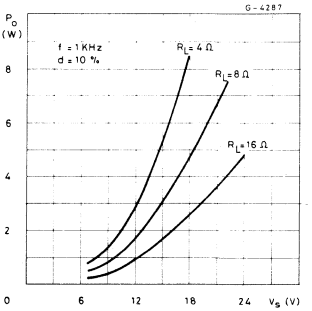
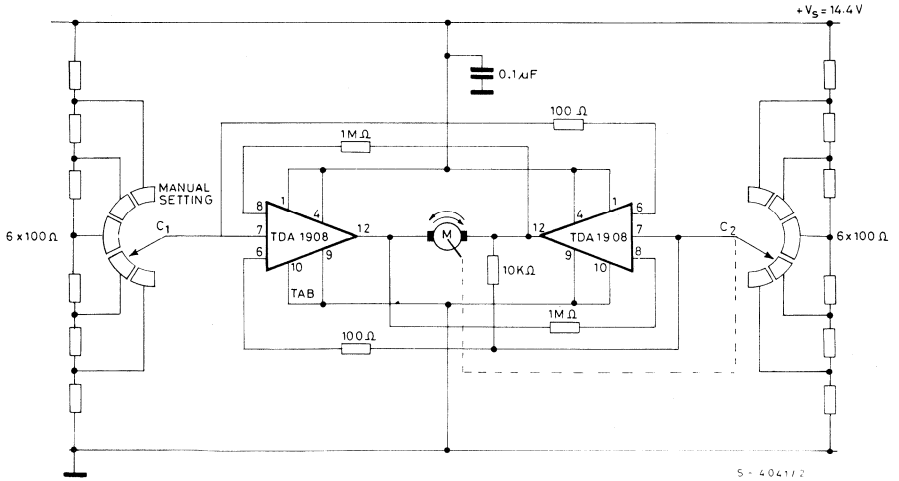



Fig. 23 - Position control for car headlights



## APPLICATION SUGGESTION

The recommended values of the external components are those shown on the application circuit of fig. 19.
When the supply voltage $V_s$ is less than 10V, a 100Ω resistor must be connected between pin 1 and pin 4 in order to obtain the maximum output power.
Different values can be used. The following table can help the designer.

| Component | Raccom. value | Purpose | Larger than raccomanded value | Smaller than raccomanded value | Allowed range | |
|---|---|---|---|---|---|---|
| | | | | | Min. | Max. |
| $R_1$ | 10 KΩ | Close loop gain setting. | Increase of gain. | Decrease of gain. Increase quiescent current. | 9 $R_2$ | |
| $R_2$ | 100 Ω | Close loop gain setting. | Decrease of gain. | Increase of gain. | | $R_1/9$ |
| $R_3$ | 1 Ω | Frequency stability | Danger of oscillation at high frequencies with inductive loads. | | | |
| $R_4$ | 100 Ω | Increasing of output swing with low $V_s$. | | | 47Ω | 330Ω |
| $C_1$ | 2.2 μF | Input DC decoupling. | Lower noise | Higher low frequency cutoff. Higher noise. | 0.1 μF | |
| $C_2$ | 0.1 μF | Supply voltage bypass. | | Danger of oscillations. | | |
| $C_3$ | 2.2 μF | Inverting input DC decoupling. | Increase of the switch-on noise | Higher low frequency cutoff. | 0.1 μF | |
| $C_4$ | 10 μF | Ripple Rejection. | Increase of SVR. Increase of the switch-on time. | Degradation of SVR. | 2.2 μF | 100 μF |
| $C_5$ | 47 μF | Bootstrap | | Increase of the distortion at low frequency | 10 μF | 100 μF |
| $C_6$ | 0.22 μF | Frequency stability. | | Danger of oscillation. | | |
| $C_7$ | 1000 μF | Output DC decoupling. | | Higher low frequency cutoff. | | |

## THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the $T_j$ cannot be higher than 150°C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
   If, for any reason,, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 26 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 24 - Output power and drain current vs. case temperature

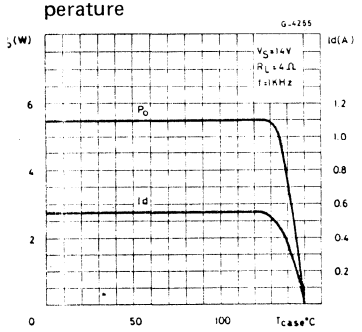



Fig. 25 - Output power and drain current vs. case temperature

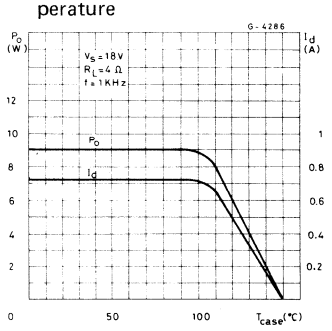
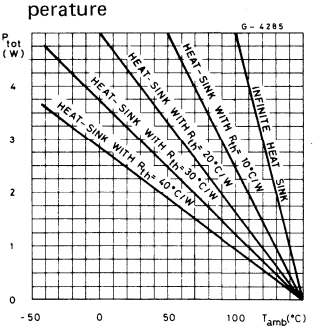


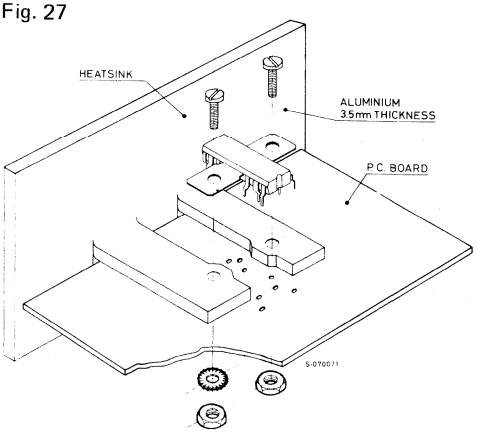

Fig. 26 - Maximum power dissipation vs. ambient temperature




## MOUNTING INSTRUCTIONS

The thermal power dissipated in the circuit may be removed by connecting the tabs to an external heatsink (TDA 1908A see fig. 27), or by soldering them to a copper area on the PC board (TDA 1908 see fig. 28). During soldering, tab temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

Fig. 27



## MOUNTING INSTRUCTIONS (continued)

Fig. 28 - Mounting example (TDA 1908)

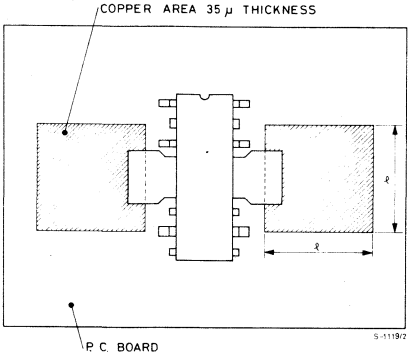
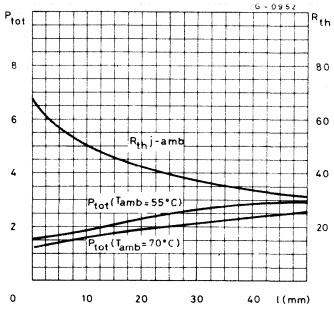



Fig. 29 - Maximum power dissipation and thermal resistance vs. side "ℓ" (TDA 1908)



## 10W AUDIO AMPLIFIER WITH MUTING

The TDA 1910 is a monolithic integrated circuit in MULTIWATT® package, intended for use in Hi-Fi audio power applications, **as high quality TV sets.**
The TDA 1910 meets the DIN 45500 (d = 0.5%) guaranteed output power of 10W when used at 24V/4Ω. At 24V/8Ω the output power is 7W min. Features:

- muting facility
- protection against chip over temperature
- very low noise
- high supply voltage rejection
- low "switch-on" noise.

The TDA 1910 is assembled in MULTIWATT® package that offers:

- easy assembly
- simple heatsink
- space and cost saving
- high reliability.

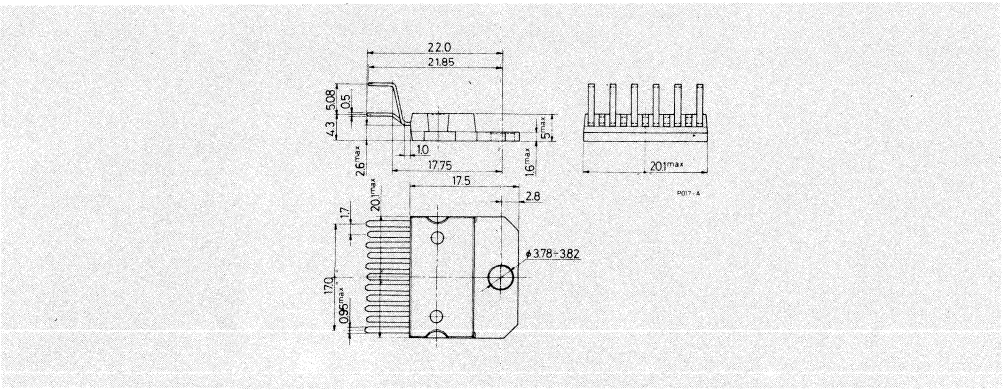
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 30 | V |
| $I_o$ | Output peak current (non repetitive) | 3.5 | A |
| $I_o$ | Output peak current (repetitive) | 3.0 | A |
| $V_i$ | Input voltage | 0 to + $V_s$ | V |
| $V_i$ | Differential input voltage | ± 7 | V |
| $V_{11}$ | Muting thresold voltage | $V_s$ | V |
| $P_{tot}$ | Power dissipation at $T_{case}$ = 90°C | 20 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

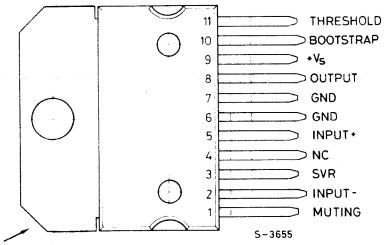
**ORDERING NUMBER:** TDA 1910

## MECHANICAL DATA

Dimensions in mm

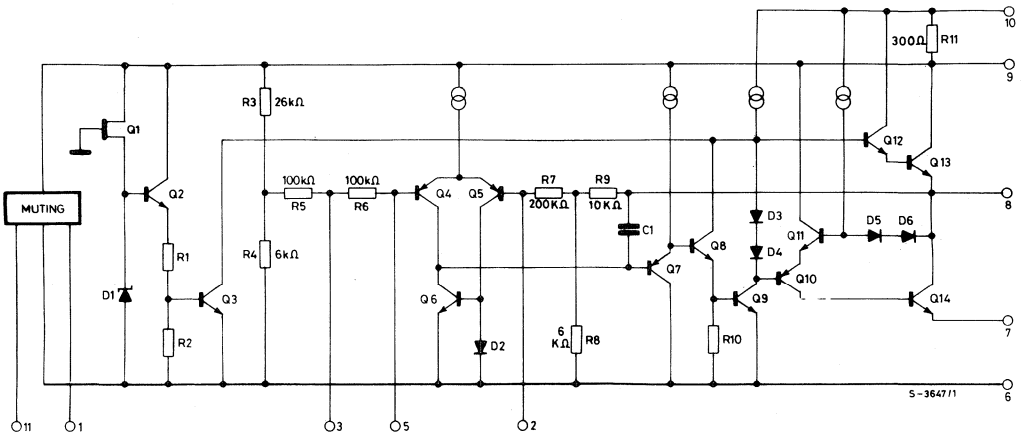


## CONNECTION DIAGRAM (Top view)

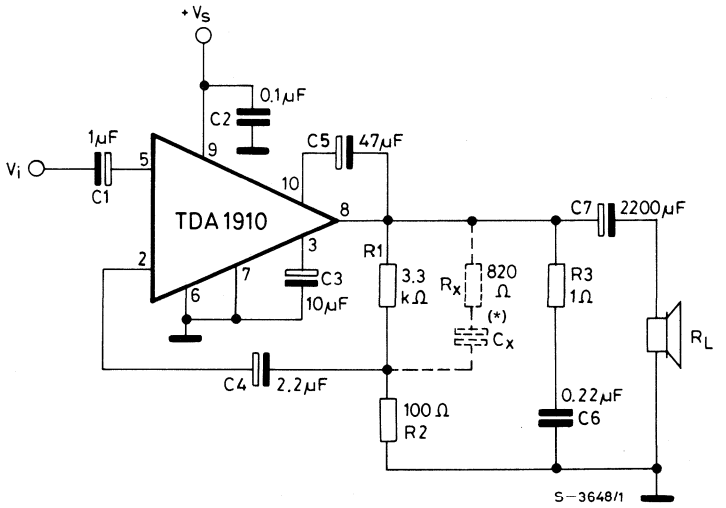



tab connected to pin 6

## SCHEMATIC DIAGRAM

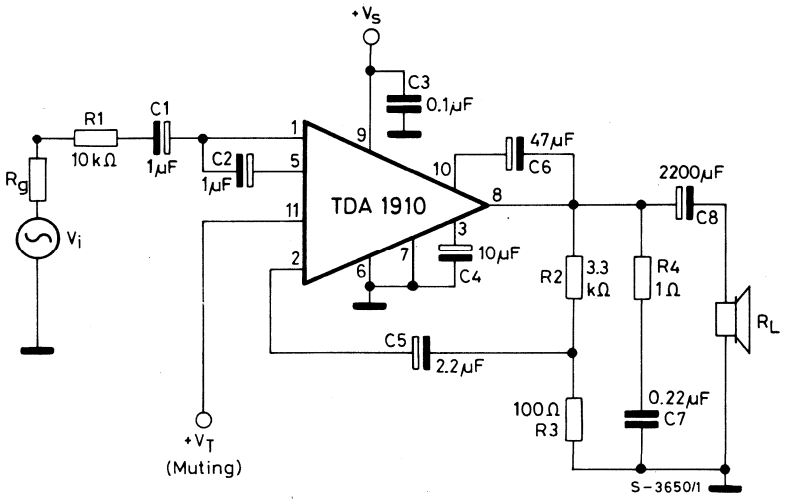


## TEST CIRCUIT




(*) See fig. 13.

## MUTING CIRCUIT



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}c}$ | Thermal resistance junction-case | max | 3 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb}$= 25°C, $R_{th}$ (heatsink) = 4°C/W, unless otherwise specified)

| Parameter | | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 8 | | 30 | V |
| $V_o$ | Quiescent output voltage | $V_s$ = 18V<br>$V_s$ = 24V | 8.3<br>11.5 | 9.2<br>12.4 | 10<br>13.4 | V |
| $I_d$ | Quiescent drain current | $V_s$ = 18V<br>$V_s$ = 24V | | 19<br>21 | 32<br>35 | mA |
| $V_{CE\ sat}$ | Output stage saturation voltage | $I_C$= 2A | | 1 | | V |
| | | $I_C$= 3A | | 1.6 | | |
| $P_o$ | Output power | d = 0.5% f = 40 to 15,000Hz<br>$V_s$ = 18V $R_L$= 4Ω<br>$V_s$ = 24V $R_L$= 4Ω<br>$V_s$ = 24V $R_L$= 8Ω | <br>6.5<br>10<br>7 | <br>7<br>12<br>7.5 | | W |
| | | d = 10% f = 1 KHz<br>$V_s$ = 18V $R_L$= 4Ω<br>$V_s$ = 24V $R_L$= 4Ω<br>$V_s$ = 24V $R_L$= 8Ω | <br>8.5<br>15<br>9 | <br>9.5<br>17<br>10 | | W |
| d | Harmonic distortion | f = 40 to 15,000 Hz<br>$V_s$ = 18V $R_L$= 4Ω<br>$P_o$= 50 mW to 6.5W<br>$V_s$= 24V $R_L$= 4Ω<br>$P_o$= 50 mW to 10W<br>$V_s$ = 24V $R_L$= 8Ω<br>$P_o$= 50 mW to 7W | | <br>0.2<br><br>0.2<br><br>0.2 | <br>0.5<br><br>0.5<br><br>0.5 | % |
| d | Intermodulation distortion | $V_s$ = 24V $R_L$= 4Ω $P_o$= 10W<br>$f_1$= 250 Hz $f_2$= 8 KHz<br>(DIN 45500) | | 0.2 | | % |
| $V_i$ | Input sensitivity | f = 1 KHz<br>$V_s$ = 18V $R_L$= 4Ω $P_o$= 7W<br>$V_s$ = 24V $R_L$= 4Ω $P_o$= 12W<br>$V_s$ = 24V $R_L$= 8Ω $P_o$= 7.5W | | <br>170<br>220<br>245 | | mV |
| $V_i$ | Input saturation voltage (rms) | $V_s$ = 18V<br>$V_s$ = 24V | 1.8<br>2.4 | | | V |
| $R_i$ | Input resistance (pin 5) | f = 1 KHz | 60 | 100 | | KΩ |
| $I_d$ | Drain current | $V_s$ = 24V f = 1 KHz<br>$R_L$= 4Ω $P_o$= 12W<br>$R_L$= 8Ω $P_o$= 7.5W | | 820<br>475 | | mA |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\eta$ | Efficiency | $V_s$ = 24V f = 1 KHz<br>$R_L$= 4Ω $P_o$= 12W<br>$R_L$= 8Ω $P_o$= 7.5W | | | 62<br>65 | | % |
| BW | Small signal bandwidth | $V_s$ = 24V $R_L$= 4Ω $P_o$= 1W | | 10 to 120,000 | | | Hz |
| BW | Power bandwidth | $V_s$ = 24V $R_L$= 4Ω<br>$P_o$ = 12W d ⩽ 0.5% | | 40 to 15,000 | | | Hz |
| $G_v$ | Voltage gain (open loop) | f = 1 KHz | | | 75 | | dB |
| $G_v$ | Voltage gain (closed loop) | $V_s$ = 24V $R_L$= 4Ω<br>f = 1 KHz $P_o$ = 1W | | 29.5 | 30 | 30.5 | dB |
| $e_N$ | Total input noise | | $R_g$ = 50Ω<br>$R_g$ = 1KΩ (°)<br>$R_g$ = 10KΩ | | 1.2<br>1.3<br>1.5 | 3.0<br>3.2<br>4.0 | μV |
| | | | $R_g$ = 50Ω<br>$R_g$ = 1KΩ (°°)<br>$R_g$ = 10KΩ | | 2.0<br>2.0<br>2.2 | 5.0<br>5.2<br>6.0 | μV |
| S/N | Signal to noise ratio | $V_s$ = 24V<br>$P_o$ = 12W<br>$R_L$= 4Ω | $R_g$ = 10KΩ<br>$R_g$ = 0 (°) | 97 | 103<br>105 | | dB |
| | | | $R_g$ = 10KΩ<br>$R_g$ = 0 (°°) | 93 | 100<br>100 | | dB |
| SVR | Supply voltage rejection | $V_s$ = 24V $R_L$= 4Ω<br>$f_{ripple}$= 100 Hz $R_g$= 10KΩ | | 50 | 60 | | dB |
| $T_{sd}$ | Thermal shut-down case temperature (*) | $P_{tot}$= 8W | | 110 | 125 | | °C |

### MUTING FUNCTION (Refer to Muting circuit)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_T$ | Muting-off threshold voltage (pin 11) | | | 1.9 | | 4.7 | V |
| $V_T$ | Muting-on threshold voltage (pin 11) | | | 0 | | 1.3 | V |
| | | | | 6 | | $V_s$ | |
| $R_1$ | Input resistance (pin 1) | Muting off | | 80 | 200 | | KΩ |
| | | Muting on | | | 10 | 30 | Ω |
| $R_{11}$ | Input resistance (pin 11) | | | 150 | | | KΩ |
| $A_T$ | Muting attenuation | $R_g + R_1$= 10 KΩ | | 50 | 60 | | dB |

**Note:**
(°) Weighting filter = curve A.
(°°) Filter with noise bandwidth: 22 Hz to 22 KHz.
(*) See fig. 29 and fig. 30.

Fig. 1 - Quiescent output voltage vs. supply voltage

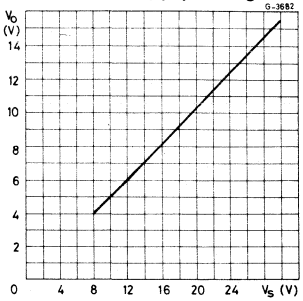



Fig. 2 - Quiescent drain current vs. supply voltage

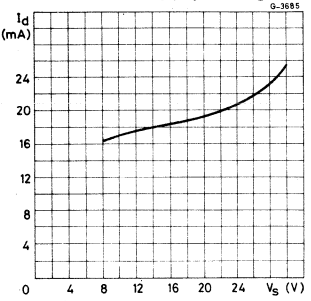



Fig. 3 - Open loop frequency response

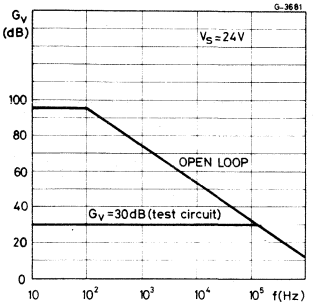



Fig. 4 - Output power vs. supply voltage

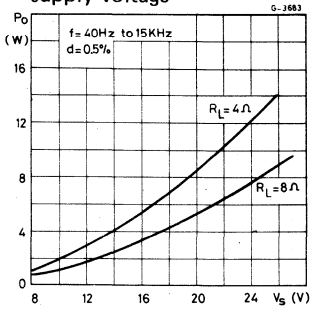



Fig. 5 - Output power vs. supply voltage

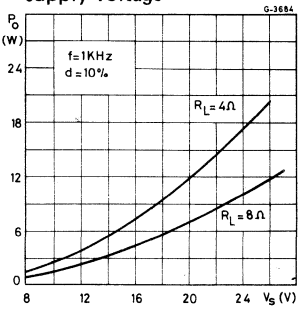



Fig. 6 - Distortion vs. output power

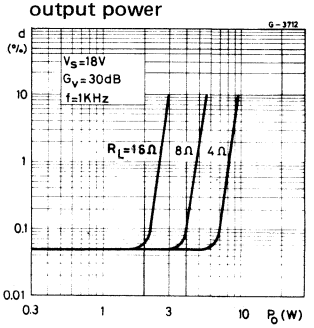



Fig. 7 - Distortion vs. output power

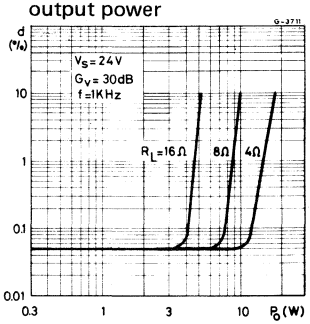



Fig. 8 - Output power vs. frequency

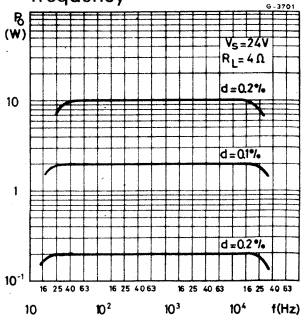



Fig. 9 - Output power vs. frequency

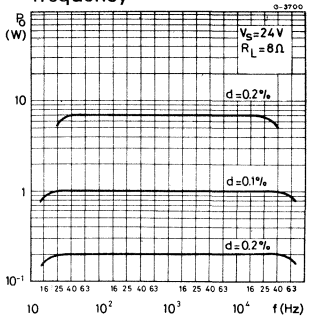


Fig. 10 - Output power vs. input voltage

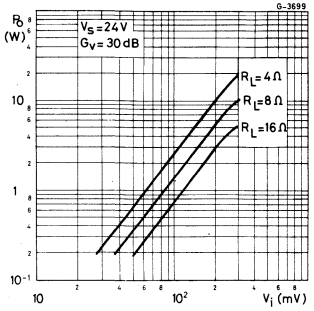



Fig. 11 - Output power vs. input voltage

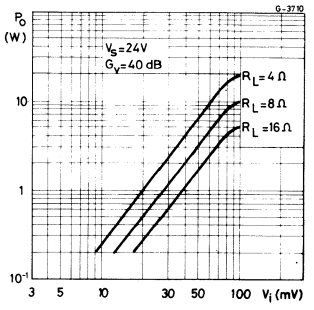



Fig. 12 - Total input noise vs. source resistance

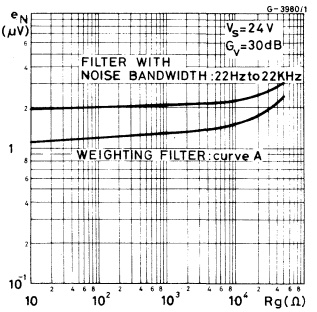



Fig. 13 - Values of capacitor $C_X$ vs. bandwidth (BW) and gain ($G_v$)

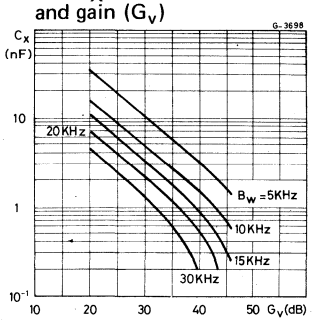



Fig. 14 - Supply voltage rejection vs. voltage gain

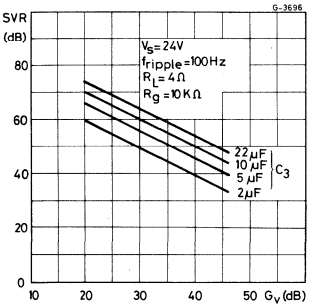



Fig. 15 - Supply voltage rejection vs. source resitance

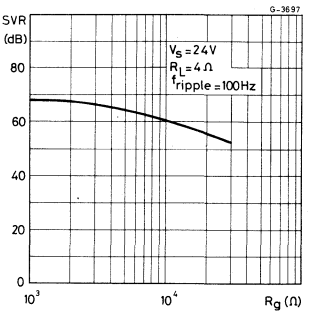



Fig. 16 - Power dissipation and efficiency vs. output power

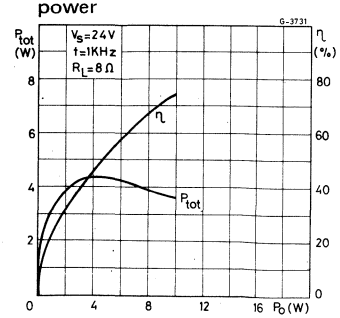



Fig. 17 - Power dissipation and efficiency vs. output power

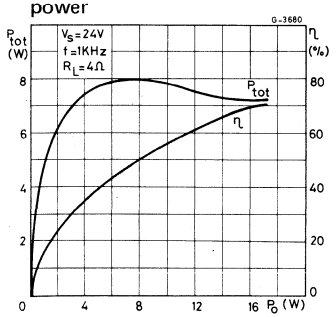
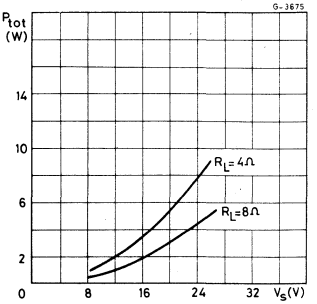



Fig. 18 - Max power dissipation vs. supply voltage



## APPLICATION INFORMATION

Fig. 19 - Application circuit without muting

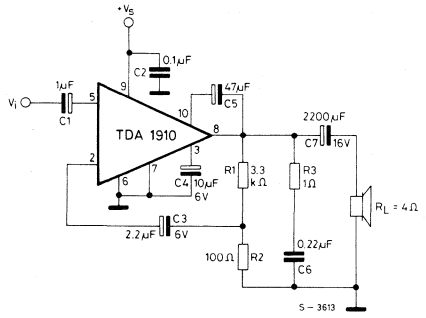



Fig. 20 - PC board and component lay-out of the circuit of fig. 19 (1:1 scale)

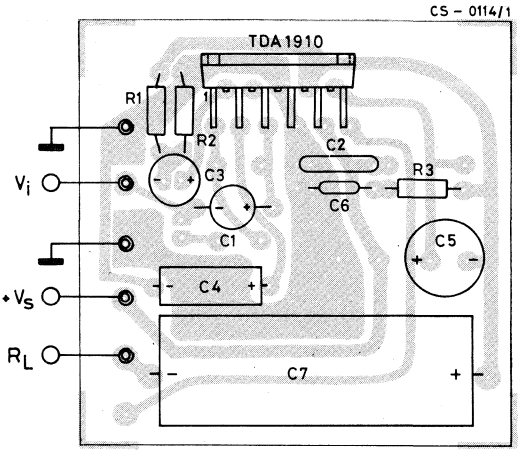
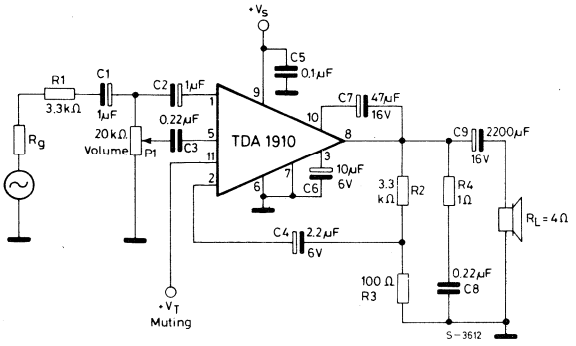



Fig. 21 - Application circuit with muting




Performance (circuits of fig. 19 and 21)

$P_o$ = 12W (40 to 15000 Hz, d ⩽0.5% )
$V_s$ = 24V
$I_d$ = 0.82A
$G_v$ = 30 dB

## APPLICATION INFORMATION (continued)

Fig. 22 - Two position DC tone control (10 dB boost 50 Hz and 20 KHz) using change of pin 1 resistance (muting function)

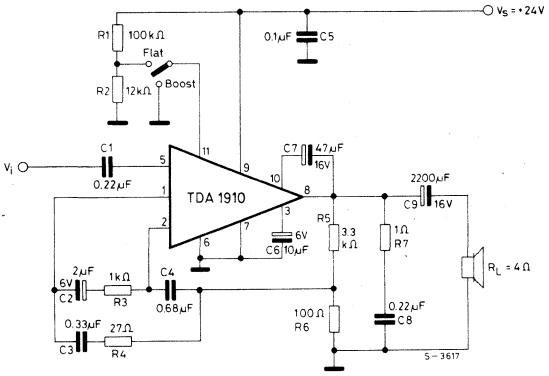



Fig. 23 - Frequency response of the circuit of fig. 22

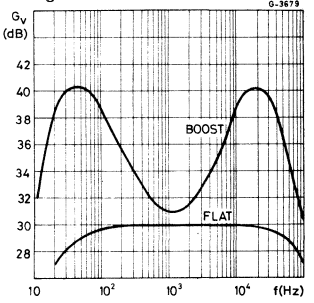



Fig. 24 - 10 dB 50 Hz boost tone control using change of pin 1 resistance (muting function)

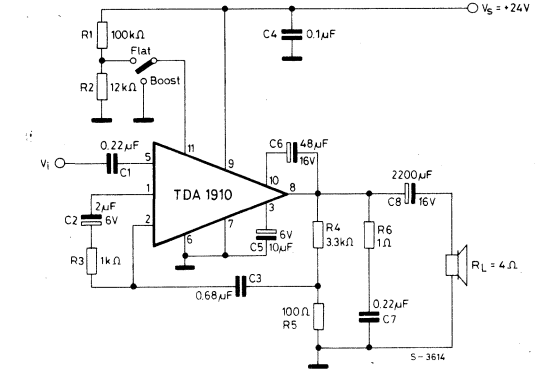



Fig. 25 - Frequency response of the circuit of fig. 24

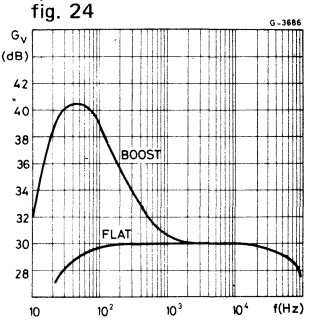



Fig. 26 - Squelch function in TV applications

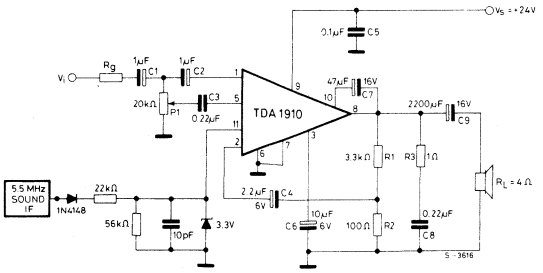
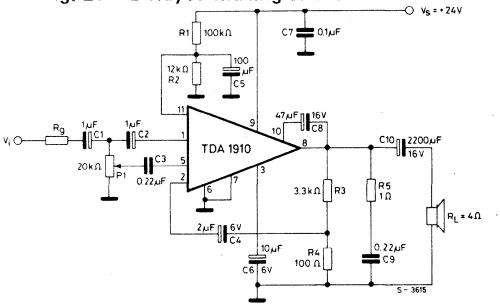


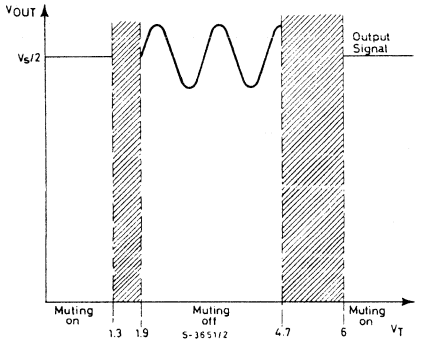

Fig. 27 - Delayed muting circuit



## MUTING FUNCTION

The output signal can be inhibited applying a DC voltage $V_T$ to pin 11, as shown in fig. 28

Fig. 28

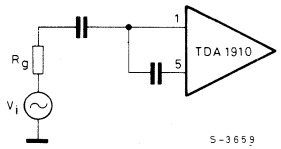



The input resistance at pin 1 depends on the threshold voltage $V_T$ at pin 11 and is typically.

$R_1 = 200\ K\Omega$ @ $1.9V \leqslant V_T \leqslant 4.7V$ muting-off

$R_1 = 10\ \Omega$ @ $0V \leqslant V_T \leqslant 1.3V$ $6V \leqslant V_T \leqslant V_s$ muting-on

Referring to the following input stage, the possible attenuation of the input signal and therefore of the output signal can be found using the following expression.




$$A_T = \frac{V_i}{V_5} = \frac{R_g + R_5//R_1}{R_5//R_1}$$

where $R_5 \cong 100\ K\Omega$

Considering $R_g = 10\ K\Omega$ the attenuation in the muting-on condition is typically $A_T = 60$ dB. In the muting-off condition, the attenuation is very low, typically 1.2 dB.
A very low current is necessary to drive the threshold voltage $V_T$ because the input resistance at pin 11 is greater than 150 KΩ. The muting function can be used in many cases, when a temporary inhibition of the output signal is requested, for example:

- in switch-on condition, to avoid preamplifier power-on transients (see fig. 27)
- during commutations at the input stages.
- during the receiver tuning.

The variable impedance capability at pin 1 can be useful in many applications and we have shown 2 examples in fig. 22 and 24, where it has been used to change the feedback network, obtaining 2 different frequency responses.

## APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 21. Different values can be used.
The following table can help the designer.

| Component | Recomm. value | Purpose | Larger than recommended value | Smaller than recommended value | Allowed range | |
|---|---|---|---|---|---|---|
| | | | | | Min. | Max. |
| $R_g + R_1$ | 10KΩ | Input signal imped. for muting operation | Increase of the attenuation in muting-on condition.Decrease of the input sensitivity. | Decrease of the attenuation in muting on condition. | | |
| $R_2$ | 3.3KΩ | Close loop gain setting. | Increase of gain. | Decrease of gain. Increase quiescent current. | $9\,R_3$ | |
| $R_3$ | 100Ω | Close loop gain setting. | Decrease of gain. | Increase of gain. | | $R_2/9$ |
| $R_4$ | 1Ω | Frequency stability | Danger of oscillation at high frequencies with inductive loads. | | | |
| $P_1$ | 20KΩ | Volume potentiometer. | Increase of the switch-on noise. | Decrease of the input impedance and the input level. | 10KΩ | 100KΩ |
| $C_1$<br>$C_2$<br>$C_3$ | 1 μF<br>1 μF<br>0.22 μF | Input DC decoupling. | | Higher low frequency cutoff. | | |
| $C_4$ | 2.2 μF | Inverting input DC decoupling. | Increase of the switch-on noise. | Higher low frequency cutoff. | 0.1 μF | |
| $C_5$ | 0.1 μF | Supply voltage bypass. | | Danger of oscillations. | | |
| $C_6$ | 10 μF | Ripple Rejection. | Increase of SVR. Increase of the switch-on time. | Degradation of SVR. | 2.2 μF | 100 μF |
| $C_7$ | 47 μF | Bootstrap. | | Increase of the distortion at low frequency. | 10 μF | 100 μF |
| $C_8$ | 0.22 μF | Frequency stability. | | Danger of oscillation. | | |
| $C_9$ | 2200 μF ($R_L = 4\Omega$)<br>1000 μF ($R_L = 8\Omega$) | Output DC decoupling. | | Higher low frequency cutoff. | | |

## THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the $T_j$ cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.
If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 31 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 29 - Output power and drain current vs. case temperature

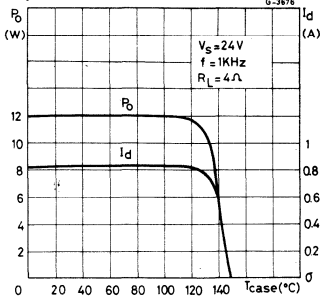



Fig. 30 - Output power and drain current vs. case temperature

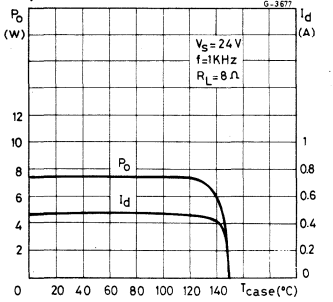
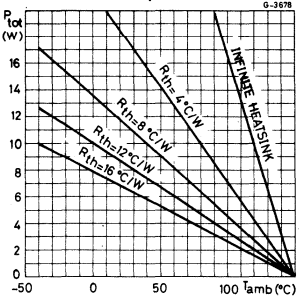


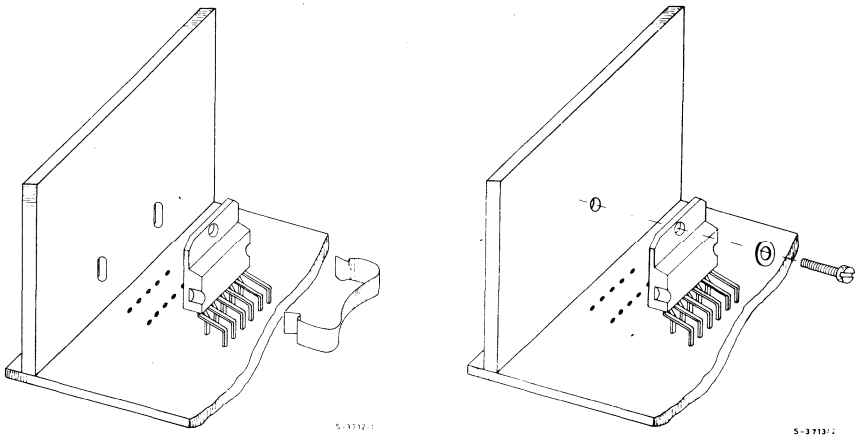

Fig. 31 - Maximum allowable power dissipation vs. ambient temperature



## MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the Multiwatt® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 34 - Mounting examples



# LINEAR INTEGRATED CIRCUITS

## 8W CAR RADIO AUDIO AMPLIFIER

The TDA 2002 is a class B audio power amplifier in Pentawatt® package designed for driving low impedance loads (down to 1.6Ω). The device provides a high output current capability (up to 3.5A), very low harmonic and cross-over distortion. In addition, the device offers the following features:

- very low number of external components
- assembly ease, due to Pentawatt® power package with no electrical insulation requirement
- space and cost saving
- high reliability
- flexibility in use
- complete safety during operation due to protection against:
  a) short circuit; b) thermal over range; c) fortuitous open ground; d) polarity inversion ($V_s$ max= 12V); e) load dump voltage surge.

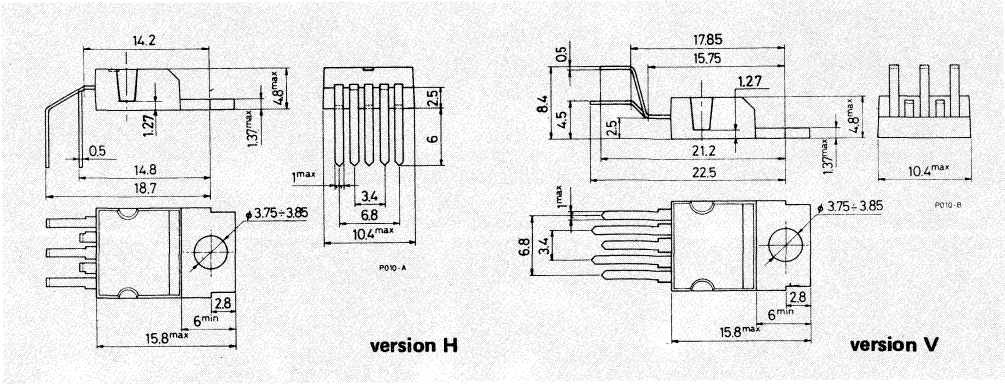
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Peak supply voltage (50 ms) | 40 | V |
| $V_s$ | DC supply voltage | 28 | V |
| $V_s$ | Operating supply voltage | 18 | V |
| $I_o$ | Output peak current (repetitive) | 3.5 | A |
| $I_o$ | Output peak current (non repetitive) | 4.5 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$= 90°C | 15 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBERS:** TDA 2002 H
TDA 2002 V

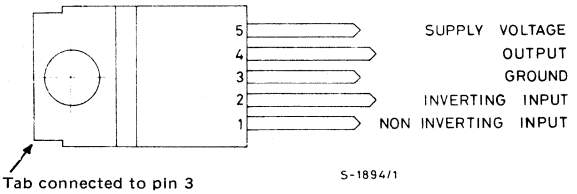
## MECHANICAL DATA

Dimensions in mm

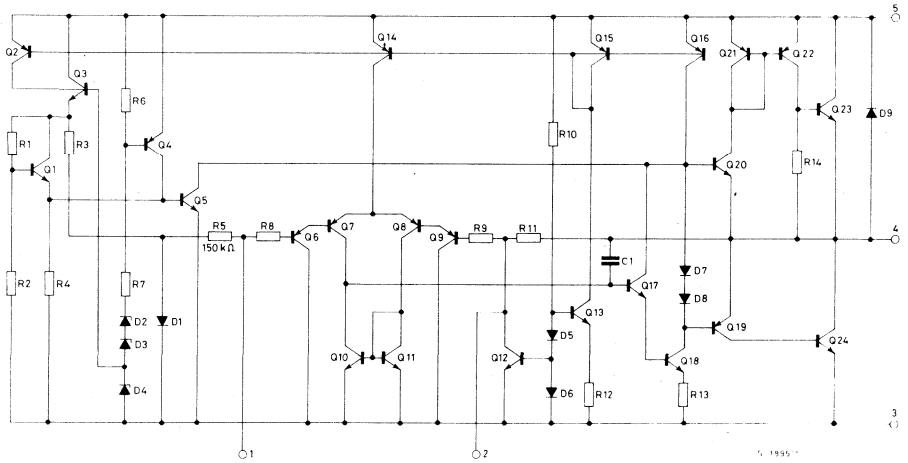


# TDA2002

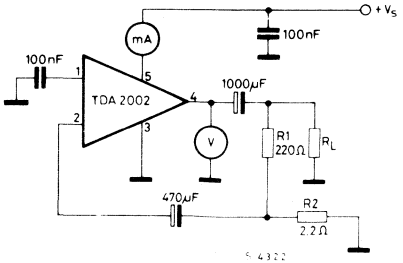
## CONNECTION DIAGRAM
(top view)



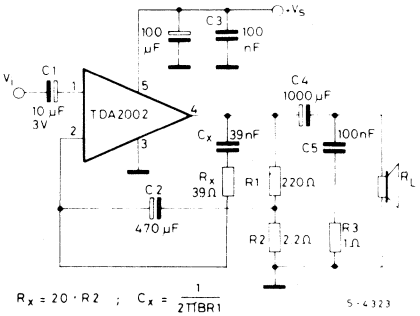

## SCHEMATIC DIAGRAM




## DC TEST CIRCUIT




## AC TEST CIRCUIT



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 4 | °C/W |

## ELECTRICAL CHARACTERISTICS ($V_s$= 14.4V, $T_{amb}$= 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** (Refer to DC test circuit) | | | | | | |
| $V_s$ | Supply voltage | | 8 | | 18 | V |
| $V_o$ | Quiescent output voltage (pin 4) | | 6.4 | 7.2 | 8 | V |
| $I_d$ | Quiescent drain current (pin 5) | | | 45 | 80 | mA |
| **AC CHARACTERISTICS** (Refer to AC test circuit, $G_v$= 40 dB) | | | | | | |
| $P_o$ | Output power | d = 10% f = 1 kHz $R_L$= 4Ω<br>$R_L$= 2Ω<br>$V_s$ = 16V<br>$R_L$= 4Ω<br>$R_L$= 2Ω | 4.8<br>7 | 5.2<br>8<br><br>6.5<br>10 | | W<br>W<br><br>W<br>W |
| $V_{i\,(rms)}$ | Input saturation voltage | | 600 | | | mV |
| $V_i$ | Input sensitivity | f = 1 kHz<br>$P_o$ = 0.5W $R_L$= 4Ω<br>$P_o$ = 0.5W $R_L$= 2Ω<br>$P_o$ = 5.2W $R_L$= 4Ω<br>$P_o$ = 8W $R_L$= 2Ω | | 15<br>11<br>55<br>50 | | mV<br>mV<br>mV<br>mV |
| B | Frequency response (-3 dB) | $R_L$= 4Ω $P_o$= 1W | 40 to 15 000 | | | Hz |
| d | Distortion | f = 1 kHz<br>$P_o$ = 0.05 to 3.5W $R_L$= 4Ω<br>$P_o$ = 0.05 to 5W $R_L$= 2Ω | | 0.2<br>0.2 | | %<br>% |
| $R_i$ | Input resistance (pin 1) | f = 1 kHz | 70 | 150 | | kΩ |
| $G_V$ | Voltage gain (open loop) | $R_L$= 4Ω f = 1 kHz | | 80 | | dB |
| $G_V$ | Voltage gain (closed loop) | $R_L$= 4Ω f = 1 kHz | 39.5 | 40 | 40.5 | dB |
| $e_N$ | Input noise voltage (*) | | | 4 | | μV |
| $i_N$ | Input noise current (*) | | | 60 | | pA |
| η | Efficiency | f = 1 kHz<br>$P_o$ = 5.2W $R_L$= 4Ω<br>$P_o$ = 8W $R_L$= 2Ω | | 68<br>58 | | %<br>% |
| SVR | Supply voltage rejection | $R_L$= 4Ω<br>$R_g$= 10 kΩ<br>$f_{ripple}$= 100 Hz | 30 | 35 | | dB |

(*) Filter with noise bandwidth: 22 Hz to 22 KHz.

Fig. 1 - Quiescent output voltage vs. supply voltage

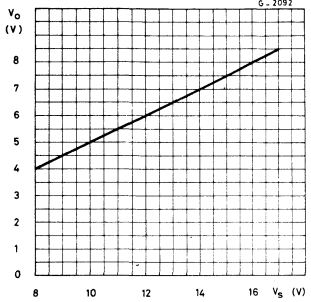



Fig. 2 - Quiescent drain current vs. supply voltage

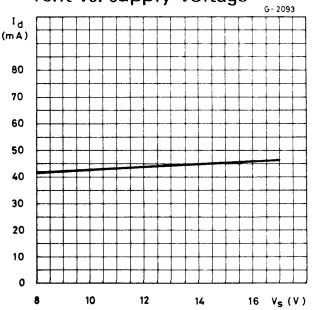



Fig. 3 - Output power vs. supply voltage

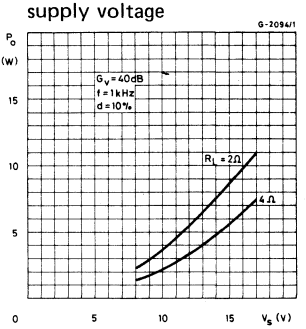



Fig. 4 - Output power vs. load resistance $R_L$

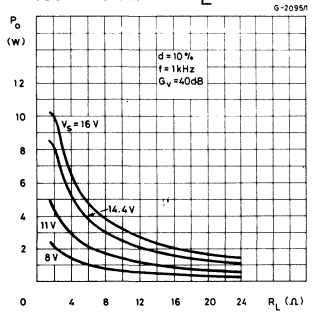



Fig. 5 - Input voltage vs. voltage gain ($R_L$ = 4Ω)

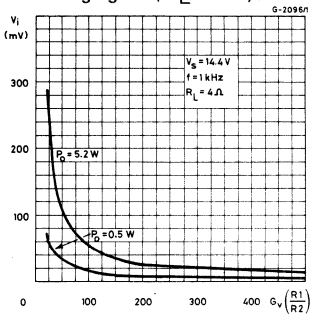



Fig. 6 - Input voltage vs. voltage gain ($R_L$ = 2Ω)

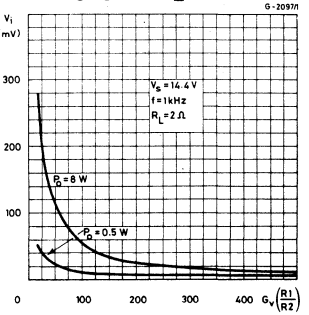



Fig. 7 - Distortion vs. output power

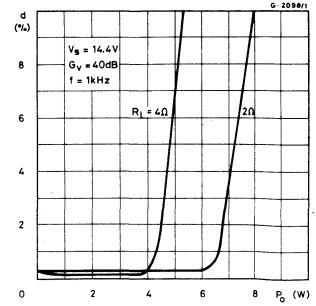



Fig. 8 - Distortion vs. frequency

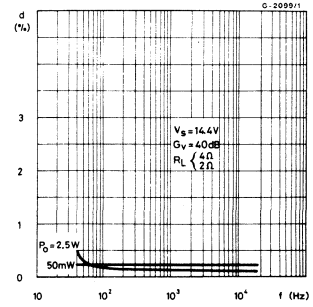



Fig. 9 - Supply voltage rejection vs. voltage gain

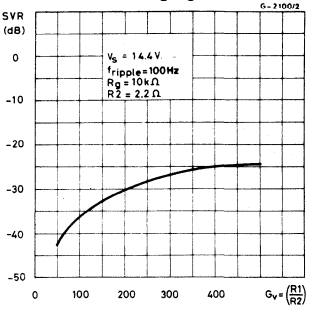


Fig. 10 - Supply voltage rejection vs. frequency

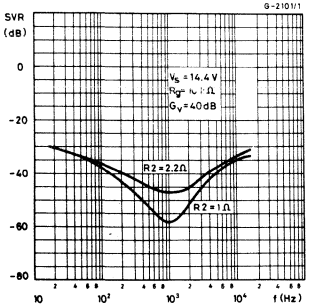



Fig. 11 - Power dissipation and efficiency vs. output power ($R_L = 4\Omega$)

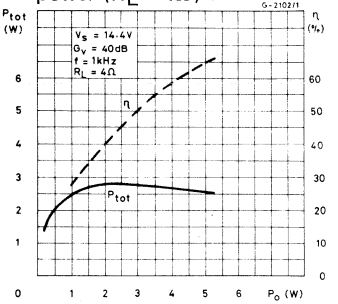



Fig. 12 - Power dissipation and efficiency vs. output power ($R_L = 2\Omega$)

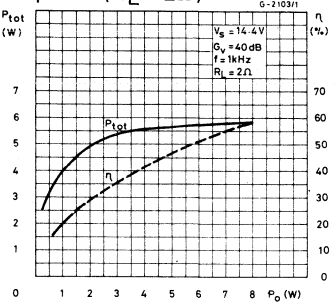



Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

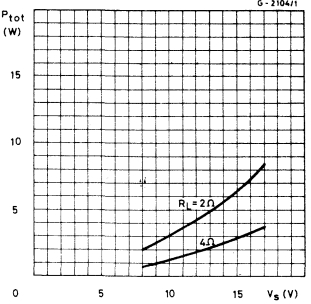



Fig. 14 - Maximim allowable power dissipation vs. ambient temperature

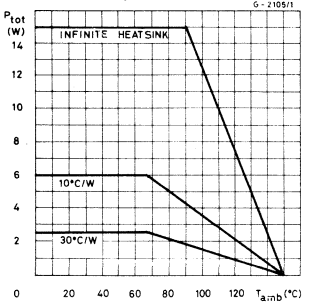
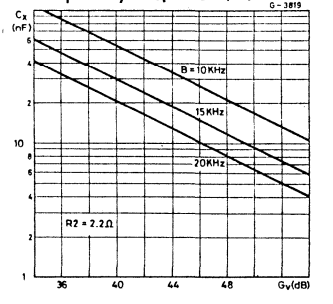



Fig. 15 - Values of capacitor ($C_X$) for different values of frequency response (B)




## APPLICATION INFORMATION

Fig. 16 - Application circuit

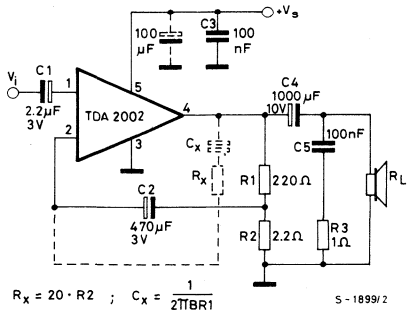
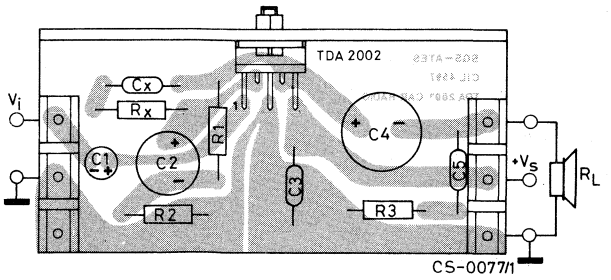



Fig. 17 - P.C. board and component layout for the circuit of fig. 16 (1:1 scale)



## LOAD DUMP VOLTAGE SURGE PROTECTION

The TDA 2002 has a circuit which enables it to withstand a voltage pulse train, on pin 5, of the type shown in fig. 18. If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig.18.
A suggested LC network is shown in fig. 19. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulsed or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 18

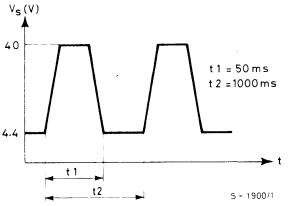
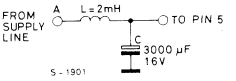



Fig. 19




## THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:
1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood
2) the heat-sink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that $P_o$ (and therefore $P_{tot}$) and $I_d$ are reduced (figs. 20 and 21)

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

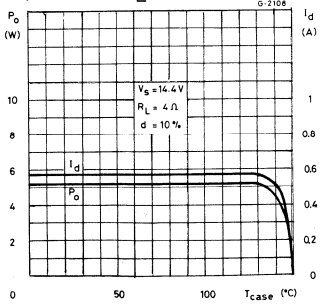
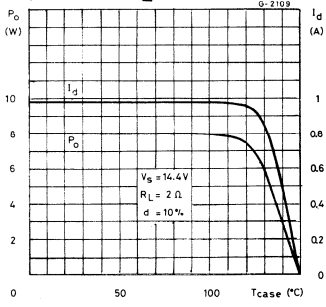



Fig. 21 - Output power and drain current vs. case temperature ($R_L = 2\Omega$)



## PRACTICAL CONSIDERATIONS

**Printed circuit board**

The layout shown in fig. 17 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

**Assembly suggestion**

No electrical insulation is needed between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260°C for 12 seconds.

**Application suggestions**

The recommended component values are those shown in the application circuits of fig. 16. Different values can be used. The following table is intended to aid the car-radio designer.

| Component | Recommended value | Purpose | Larger than recommended value | Smaller than recommended value |
|---|---|---|---|---|
| C1 | 2.2 $\mu$F | Input DC decoupling | | Noise at switch-on, switch-off |
| C2 | 470 $\mu$F | Ripple rejection | | Degradation of SVR |
| C3 | 0.1 $\mu$F | Supply bypassing | | Danger of oscillation |
| C4 | 1000 $\mu$F | Output coupling to load | | Higher low frequency cutoff |
| C5 | 0.1 $\mu$F | Frequency stability | | Danger of oscillation at high frequencies with inductive loads |
| $C_X$ | $\cong \frac{1}{2\pi B R1}$ | Upper frequency cutoff | Lower bandwidth | Larger bandwidth |
| R1 | $(G_V-1) \cdot R2$ | Setting of gain | | Increase of drain current |
| R2 | 2.2 $\Omega$ | Setting of gain and SVR | Degradation of SVR | |
| R3 | 1 $\Omega$ | Frequency stability | Danger of oscillation at high frequencies with inductive loads | |
| $R_X$ | $\cong$ 20 R2 | Upper frequency cutoff | Poor high frequency attenuation | Danger of oscillation |

## 10W CAR RADIO AUDIO AMPLIFIER

The TDA 2003 has improved performance with the same pin configuration as the TDA 2002. The additional features of TDA 2002, very low number of external components, ease of assembly, space and cost saving, are maintained.
The device provides a high output current capability (up to 3.5A) very low harmonic and cross-over distortion.
Completely safe operation is guaranteed due to protection against DC and AC short circuit between all pins and ground, thermal over-range, load dump voltage surge up to 40V, polarity inversion and fortuitous open ground.

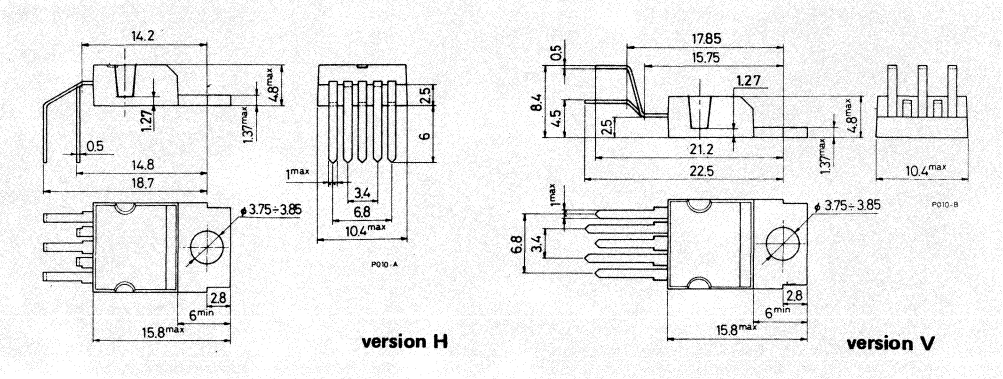
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Peak supply voltage (50 ms) | 40 | V |
| $V_s$ | DC supply voltage | 28 | V |
| $V_s$ | Operating supply voltage | 18 | V |
| $I_o$ | Output peak current (repetitive) | 3.5 | A |
| $I_o$ | Output peak current (non repetitive) | 4.5 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$= 90°C | 20 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

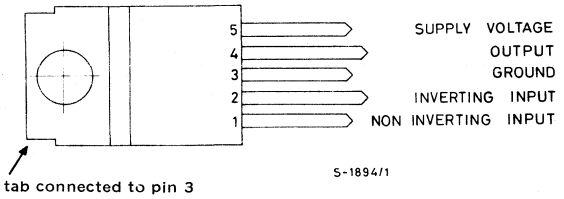
**ORDERING NUMBERS:** TDA 2003H
TDA 2003V

## MECHANICAL DATA

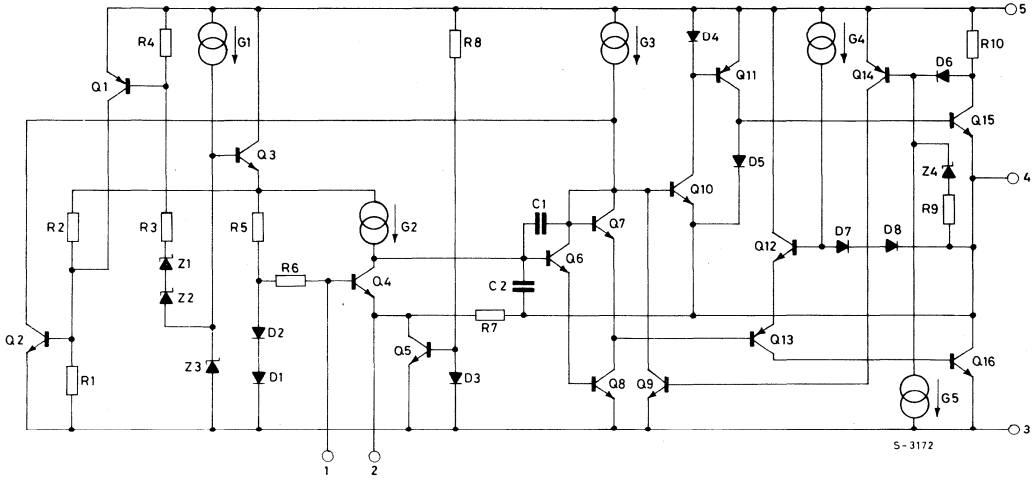
Dimensions in mm



## CONNECTION DIAGRAM
(top view)



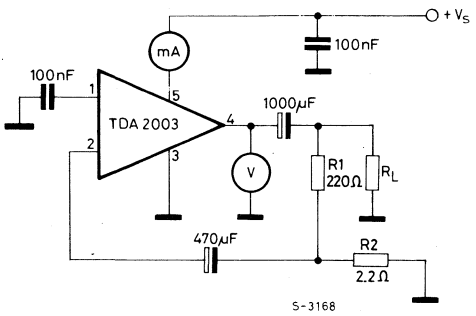

## SCHEMATIC DIAGRAM



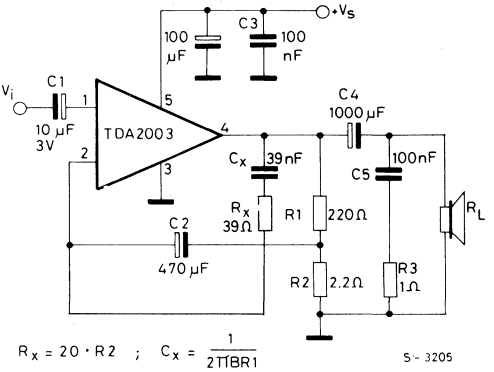

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

## DC TEST CIRCUIT




## AC TEST CIRCUIT




## ELECTRICAL CHARACTERISTICS ($V_s$= 14.4V, $T_{amb}$= 25°C unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** (Refer to DC test circuit) | | | | | | | |
| $V_s$ | Supply voltage | | | 8 | | 18 | V |
| $V_o$ | Quiescent output voltage (pin 4) | | | 6.1 | 6.9 | 7.7 | V |
| $I_d$ | Quiescent drain current (pin 5) | | | | 44 | 50 | mA |
| **AC CHARACTERISTICS** (Refer to AC test circuit, $G_v$= 40 dB) | | | | | | | |
| $P_o$ | Output power | d = 10%<br>f = 1 kHz | $R_L$= 4Ω<br>$R_L$= 2Ω<br>$R_L$= 3.2Ω<br>$R_L$= 1.6Ω | 5.5<br>9 | 6<br>10<br>7.5<br>12 | | W<br>W<br>W<br>W |
| $V_{i(rms)}$ | Input saturation voltage | | | 300 | | | mV |
| $V_i$ | Input sensitivity | f = 1 kHz<br>$P_o$ = 0.5W<br>$P_o$ = 6W<br>$P_o$ = 0.5W<br>$P_o$ = 10W | <br>$R_L$= 4Ω<br>$R_L$= 4Ω<br>$R_L$= 2Ω<br>$R_L$= 2Ω | | <br>14<br>55<br>10<br>50 | | <br>mV<br>mV<br>mV<br>mV |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| B | Frequency response (-3 dB) | $P_o$ = 1W<br>$R_L$ = 4Ω | | 40 to 15,000 | | Hz |
| d | Distortion | f = 1 kHz<br>$P_o$ = 0.05 to 4.5W $R_L$ = 4Ω<br>$P_o$ = 0.05 to 7.5W $R_L$ = 2Ω | | 0.15<br>0.15 | | %<br>% |
| $R_i$ | Input resistance (pin 1) | f = 1 kHz | 70 | 150 | | kΩ |
| $G_v$ | Voltage gain (open loop) | f = 1 kHz<br>f = 10 kHz | | 80<br>60 | | dB<br>dB |
| $G_v$ | Voltage gain (closed loop) | f = 1 kHz<br>$R_L$ = 4Ω | 39.5 | 40 | 40.5 | dB |
| $e_N$ | Input noise voltage (0) | | | 1 | 5 | μV |
| $i_N$ | Input noise current (0) | | | 60 | 200 | pA |
| η | Efficiency | f = 1 kHz<br>$P_o$ = 6W $R_L$ = 4Ω<br>$P_o$ = 10W $R_L$ = 2Ω | | 69<br>65 | | %<br>% |
| SVR | Supply voltage rejection | f = 100 Hz<br>$V_{ripple}$ = 0.5V<br>$R_g$ = 10 kΩ $R_L$ = 4Ω | 30 | 36 | | dB |

(0) Filter with noise bandwidth: 22 Hz to 22 kHz

Fig. 1 - Quiescent output voltage vs. supply voltage

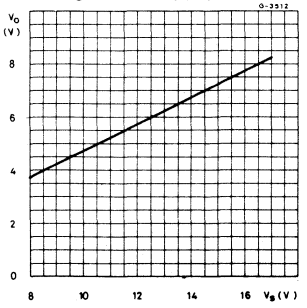



Fig. 2 - Quiescent drain current vs. supply voltage

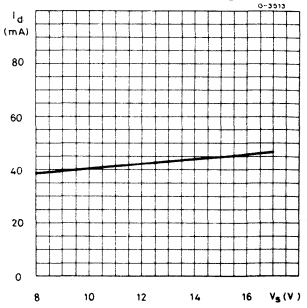



Fig. 3 - Output power vs. supply voltage

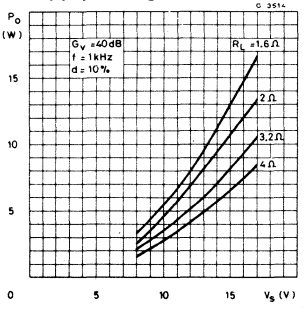


Fig. 4 - Output power vs. load resistance $R_L$

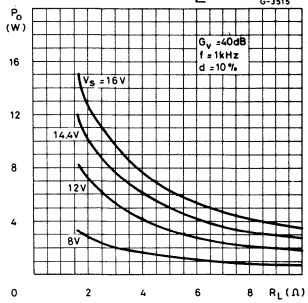



Fig. 5 - Gain vs. input sensitivity

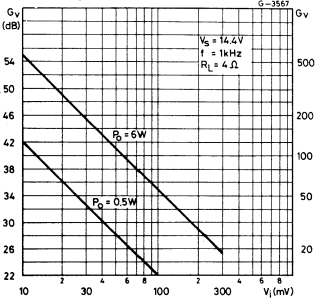



Fig. 6 - Gain vs. input sensitivity

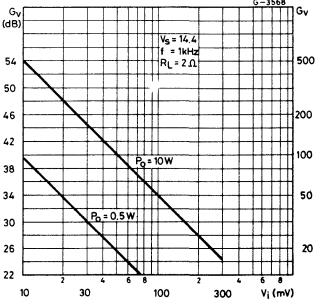



Fig. 7 - Distortion vs. output power

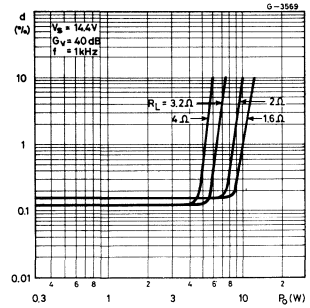



Fig. 8 - Distortion vs. frequency

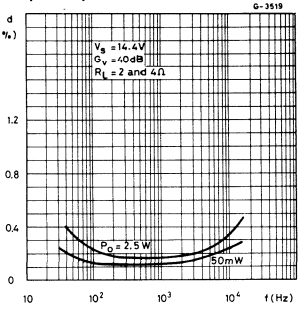



Fig. 9 - Supply voltage rejection vs. voltage gain

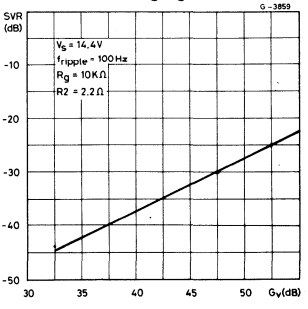



Fig. 10 - Supply voltage rejection vs. frequency

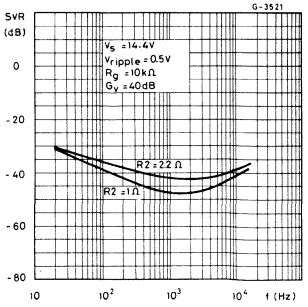



Fig. 11 - Power dissipation and efficiency vs. output power ($R_L = 4\Omega$)

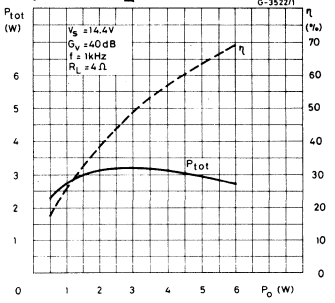



Fig. 12 - Power dissipation and efficiency vs. output power ($R_L = 2\Omega$)

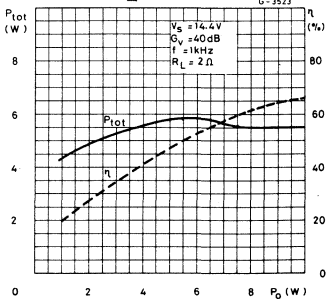


Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

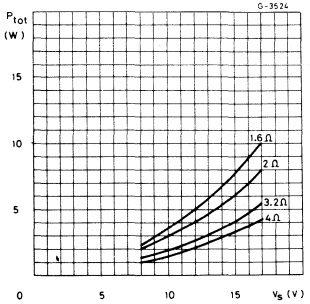



Fig. 14 - Maximum allowable power dissipation vs. ambient temperature

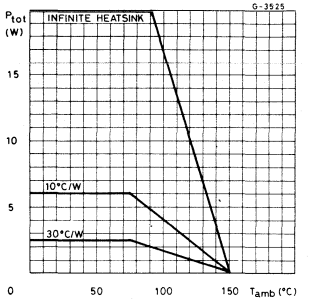
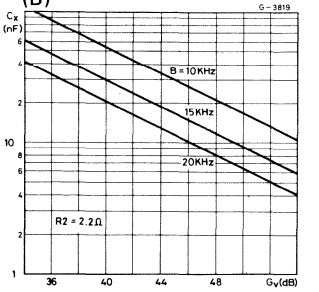



Fig. 15 - Typical values of capacitor ($C_X$) for different values of frequency response (B)




## APPLICATION INFORMATION

Fig. 16 - Typical application circuit

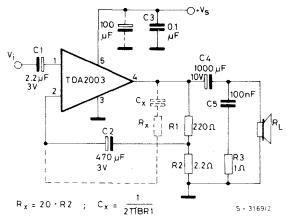



Fig. 17 - P.C. board and component layout for the circuit of fig. 16 (1:1 scale)

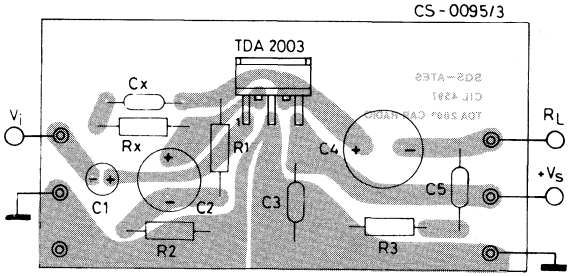
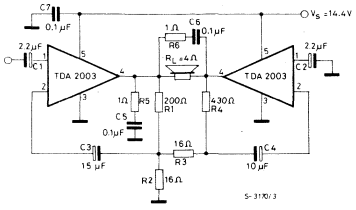
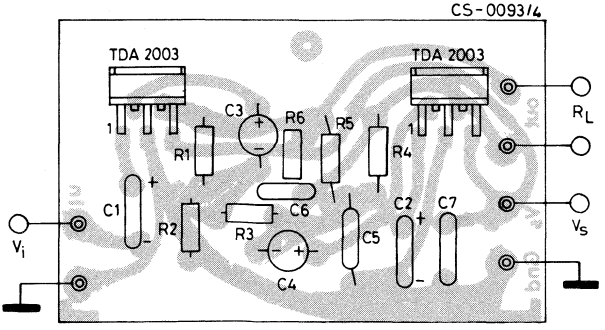



Fig. 18 - 20W bridge configuration application circuit (*)



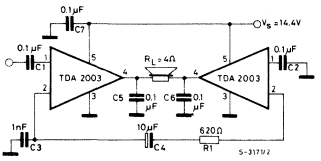

(*) The values of the capacitors C3 and C4 are different to optimize the SVR (Typ.= 40 dB)

Fig. 19 - P.C. board and component layout for the circuit of fig. 18 (1:1 scale)



## APPLICATION INFORMATION (continued)

Fig. 20 - Low cost bridge configuration application circuit (*) ($P_o$= 18W)




(*) In this application the device can support a short circuit between every side of the loudspeaker and ground.

Fig. 21 - P.C. board and component layout for the circuit of fig. 20 (1:1 scale)

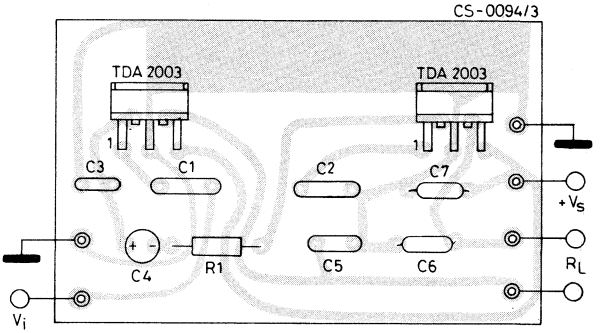
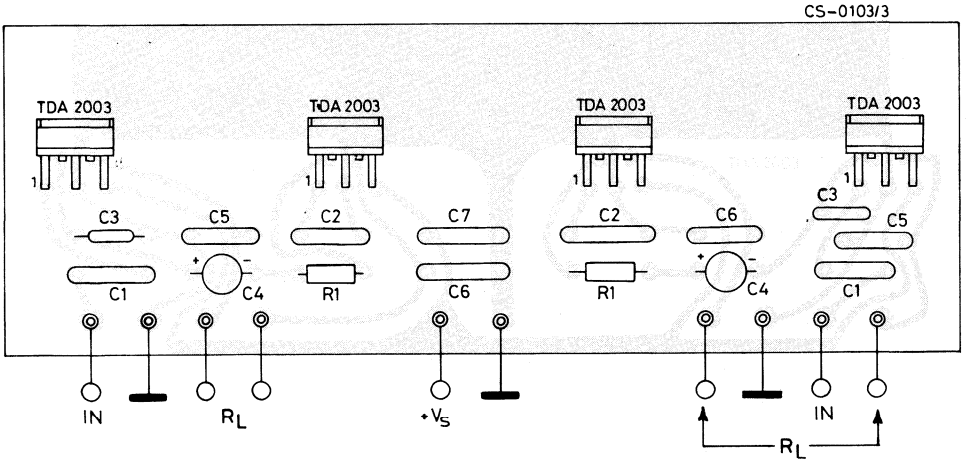



Fig. 22 - P.C. board and component layout for the low-cost bridge amplifier of fig. 20, in stereo version (1:1 scale)




## BUILT-IN PROTECTION SYSTEMS

### Load dump voltage surge

The TDA 2003 has a circuit which enables it to withstand a voltage pulse train, on pin 5, of the type shown in fig. 23.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 5, in order to assure that the pulses at pin 5 will be held within the limits shown in fig. 23. A suggested LC network is shown in fig. 24. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulsed or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 23

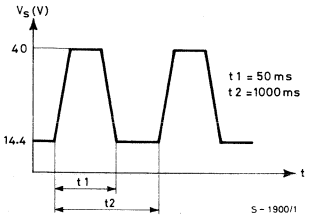
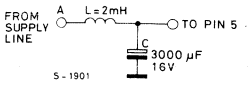



Fig. 24




## Short-circuit (AC and DC conditions)

The TDA 2003 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

## Polarity inversion

High current (up to 5A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 1A fuse (normally connected in series with the supply).
This feature is added to avoid destruction if, during fitting to the car, a mistake on the connection of the supply is made.

## Open ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA 2003 protection diodes are included to avoid any damage.

## Inductive load

A protection diode is provided between pin 4 and 5 (see the internal schematic diagram) to allow use of the TDA 2003 with inductive loads.
In particular, the TDA 2003 can drive a coupling transformer for audio modulation.

## DC voltage

The maximum operating DC voltage on the TDA 2003 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries were series connected to crank the engine.

## Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:
1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heat-sink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that $P_o$ (and therefore $P_{tot}$) and $I_d$ are reduced (figs. 25 and 26).

Fig. 25 - Output power and drain current vs. case temperature ($R_L$ = 4 Ω)

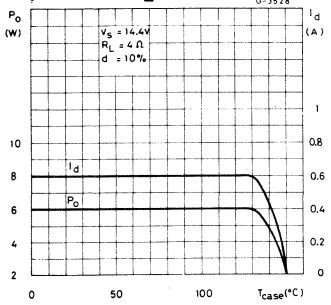
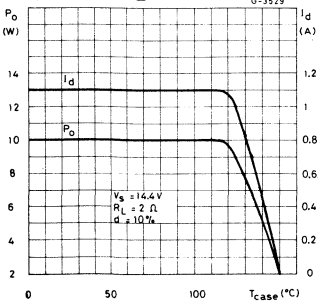



Fig. 26 - Output power and drain current vs. case temperature ($R_L$ = 2Ω)



## PRATICAL CONSIDERATIONS

**Printed circuit board**
The layout shown in fig. 17 is recommended. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground of the output through which a rather high current flows.

**Assembly suggestion**
No electrical insulation is required between the package and the heat-sink. Pin length should be as short as possible. The soldering temperature must not exceed 260° C for 12 seconds.

**Application suggestions**
The recommended component values are those shown in the application circuits of fig. 16. Different values can be used. The following table is intended to aid the car-radio designer.

| Component | Recommended value | Purpose | Larger than recommended value | Smaller than recommended value |
|---|---|---|---|---|
| C1 | 2.2 $\mu$F | Input DC decoupling | | Noise at switch-on, switch-off |
| C2 | 470 $\mu$F | Ripple rejection | | Degradation of SVR |
| C3 | 0.1 $\mu$F | Supply bypassing | | Danger of oscillation |
| C4 | 1000 $\mu$F | Output coupling to load | | Higher low frequency cutoff |
| C5 | 0.1 $\mu$F | Frequency stability | | Danger of oscillation at high frequencies with inductive loads |
| $C_X$ | $\cong \frac{1}{2\pi B R1}$ | Upper frequency cutoff | Lower bandwidth | Larger bandwidth |
| R1 | $(G_V-1) \cdot R2$ | Setting of gain | | Increase of drain current |
| R2 | 2.2 $\Omega$ | Setting of gain and SVR | Degradation of SVR | |
| R3 | 1 $\Omega$ | Frequency stability | Danger of oscillation at high frequencies with inductive loads | |
| $R_X$ | $\cong$ 20 R2 | Upper frequency cutoff | Poor high frequency attenuation | Danger of oscillation |

# TDA2004

## 10 + 10W STEREO AMPLIFIER FOR CAR RADIO

The TDA 2004 is a class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio applications: stereo amplifiers are easily designed using this device that provides a high current capability (up to 3.5A) and that can drive very low impedance loads (down to 1.6Ω).
Its main features are:

**Low distortion.**
**Low noise.**
**High reliability** of the chip and of the package with additional complete safety during operation thanks to protections against:
– output AC short circuit to ground
– very inductive loads
– overrating chip temperature
– load dump voltage surge
– fortuitous open ground
– polarity inversion
**Space and cost saving:** very low number of external components, very simple mounting system with no electrical isolation between the package and the heatsink (one screw only).

## ABSOLUTE MAXIMUM RATINGS

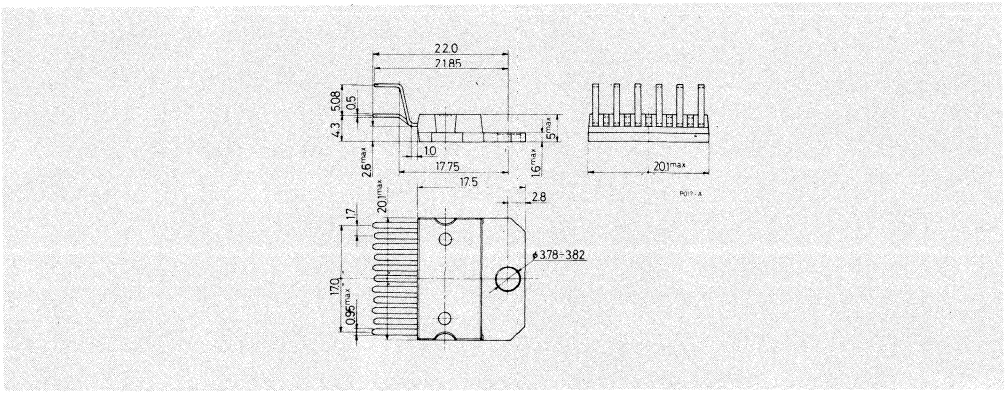
| | | | |
|---|---|---|---|
| $V_s$ | Operating supply voltage | 18 | V |
| $V_s$ | DC supply voltage | 28 | V |
| $V_s$ | Peak supply voltage (for 50 ms) | 40 | V |
| $I_o$ (*) | Output peak current (non repetitive t = 0.1 ms) | 4.5 | A |
| $I_o$ (*) | Output peak current (repetitive f ⩾ 10 Hz) | 3.5 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$ = 60 °C | 30 | W |
| $T_j$, $T_{stg}$ | Storage and junction temperature | -40 to 150 | °C |

(*) The max. output current is internally limited.

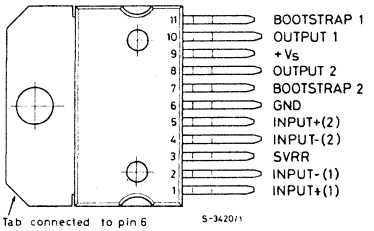
**ORDERING NUMBER:** TDA 2004

## MECHANICAL DATA

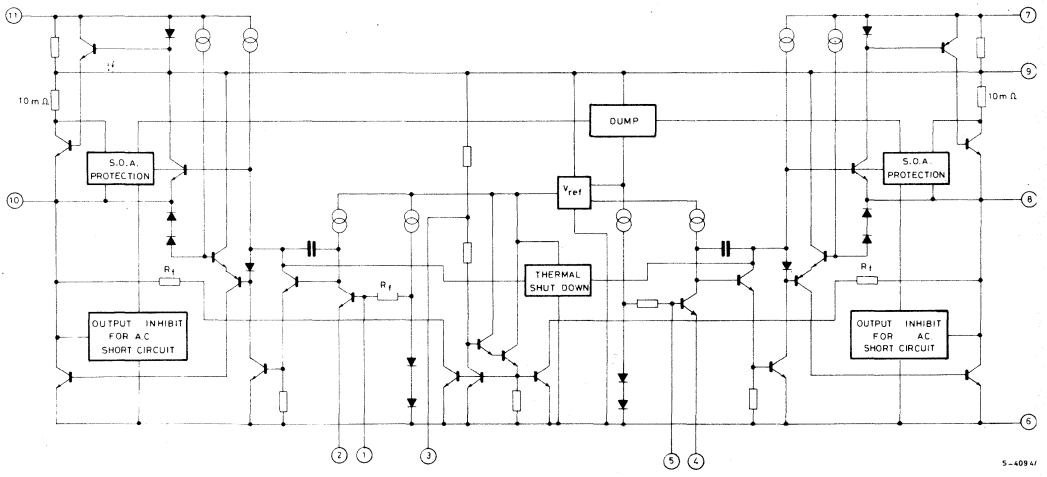
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## SCHEMATIC DIAGRAM




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

Fig. 1 - Test and application circuit

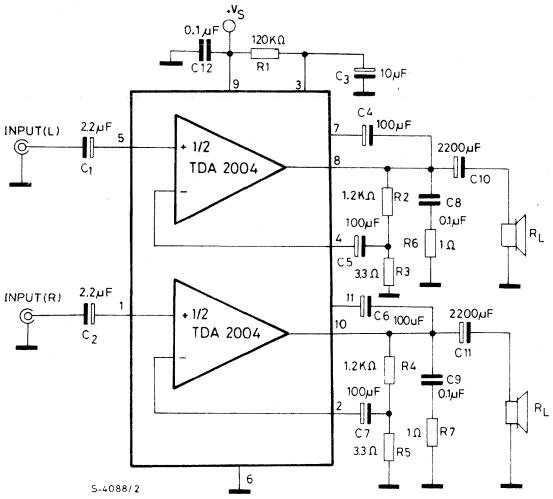
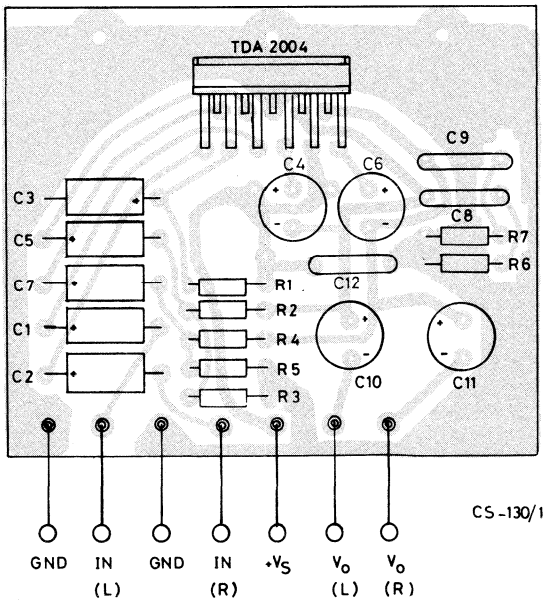



Fig. 2 - PC board and components layout (scale 1:1)



**ELECTRICAL CHARACTERISTICS** (Refer to the test circuit, $T_{amb}$= 25°C, $G_v$= 50 dB, $R_{th\ (heatsink)}$ = 4°C/W, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 8 | | 18 | V |
| $V_o$ | Quiescent output voltage | $V_s$ = 14.4V<br>$V_s$ = 13.2V | 6.6<br>6.0 | 7.2<br>6.6 | 7.8<br>7.2 | V<br>V |
| $I_d$ | Total quiescent drain current | $V_s$ = 14.4V<br>$V_s$ = 13.2V | | 65<br>62 | 120<br>120 | mA<br>mA |
| $I_{SB}$ | Stand-by current | Pin 3 grounded | | 5 | | mA |
| $P_o$ | Output power (each channel) | f = 1 KHz d = 10%<br>$V_s$ = 14.4V<br>$R_L$= 4Ω<br>$R_L$= 3.2Ω<br>$R_L$= 2Ω<br>$R_L$= 1.6Ω<br>$V_s$ = 13.2V<br>$R_L$= 3.2Ω<br>$R_L$= 1.6Ω<br>$V_s$ = 16V<br>$R_L$= 2 Ω | <br><br>6<br>7<br>9<br>10<br><br>6<br>9<br><br> | <br><br>6.5<br>8<br>10(*)<br>11<br><br>6.5<br>10<br><br>12 | | <br><br>W<br>W<br>W<br>W<br><br>W<br>W<br><br>W |
| d | Distortion (each channel) | f = 1 KHz<br>$V_s$ = 14.4V $R_L$= 4Ω<br>$P_o$= 50 mW to 4W<br>$V_s$ = 14.4V $R_L$= 2Ω<br>$P_o$= 50 mW to 6W<br>$V_s$ = 13.2V $R_L$= 3.2Ω<br>$P_o$= 50 mW to 3W<br>$V_s$ = 13.2V $R_L$= 1.6Ω<br>$P_o$= 50 mW to 6W | | <br><br>0.2<br><br>0.3<br><br>0.2<br><br>0.3 | <br><br>1<br><br>1<br><br>1<br><br>1 | <br><br>%<br><br>%<br><br>%<br><br>% |
| CT | Cross talk | $V_s$ = 14.4V<br>$V_o$= 4 $V_{rms}$ $R_L$= 4Ω<br>f = 1 KHz<br>f = 10 KHz $R_g$ = 5 KΩ | <br><br>50<br>40 | <br><br>60<br>45 | | <br><br>dB<br>dB |
| $V_i$ | Input sensitivity | f = 1 KHz<br>$P_o$ = 1W<br>$R_L$= 4Ω<br>$R_L$= 3.2Ω | | <br><br>6<br>5.5 | | <br><br>mV<br>mV |
| $V_i$ | Input saturation voltage | | 300 | | | mV |
| $R_i$ | Input resistance (non inverting input) | f = 1 KHz | 70 | 200 | | KΩ |
| $R_i$ | Input resistance (inverting input) | f = 1 KHz | | 10 | | KΩ |
| $f_L$ | Low frequency roll off (-3 dB) | $R_L$= 4Ω<br>$R_L$= 2Ω<br>$R_L$= 3.2Ω<br>$R_L$= 1.6Ω | | | 35<br>50<br>40<br>55 | Hz<br>Hz<br>Hz<br>Hz |
| $f_H$ | High frequency roll off (-3 dB) | $R_L$= 4Ω<br>$R_L$= 2Ω<br>$R_L$= 3.2Ω<br>$R_L$= 1.6Ω | 15<br>15<br>15<br>15 | | | KHz<br>KHz<br>KHz<br>KHz |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameters | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $G_v$ | Voltage gain (open loop) | f = 1 KHz | | 90 | | dB |
| $G_v$ | Voltage gain (closed loop) | f = 1 KHz | 48 | 50 | 51 | dB |
| | Closed loop gain matching | | | 0.5 | | dB |
| $e_N$ | Total input noise voltage | $R_g$= 10 KΩ(°) | | 1.5 | 5 | μV |
| SVR | Supply voltage rejection | $f_{ripple}$= 100 Hz $R_g$= 10 KΩ<br>$C_3$= 10 μF $V_{ripple}$=0.5$V_{rms}$ | 35 | 45 | | dB |
| $\eta$ | Efficiency | $V_S$ = 14.4V f = 1 KHz<br>$R_L$= 4Ω $P_o$= 6.5W<br>$R_L$= 2Ω $P_o$= 10W<br>$V_S$ = 13.2V f = 1 KHz<br>$R_L$= 3.2Ω $P_o$= 6.5W<br>$R_L$= 1.6Ω $P_o$= 10W | | 70<br>60<br><br>70<br>60 | | %<br>%<br><br>%<br>% |
| $T_{sd}$ | Thermal shut down case temperature | $V_S$ = 14.4V $R_L$= 4Ω<br>f = 1 KHz<br>$P_{tot}$= 5.5W | 125 | 135 | | °C |

(*) 9.3W without bootstrap.
(°) Bandwidth filter: 22 Hz to 22 KHz.

Fig. 3 - Quiescent output voltage vs. supply voltage

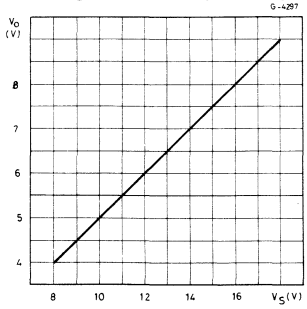



Fig. 4 - Quiescent drain current vs. supply voltage

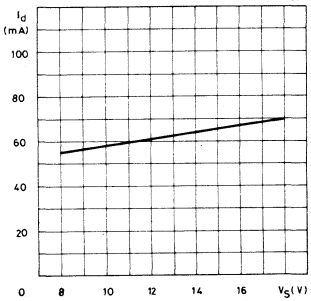



Fig. 5 - Distortion vs. output power

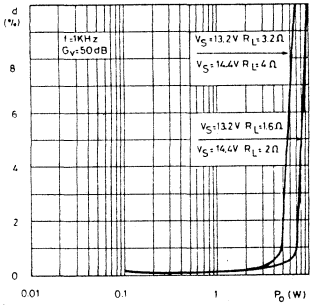



Fig. 6 - Output power vs. supply voltage

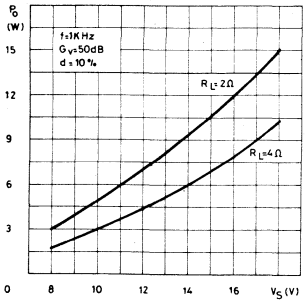



Fig. 7 - Output power vs. supply voltage

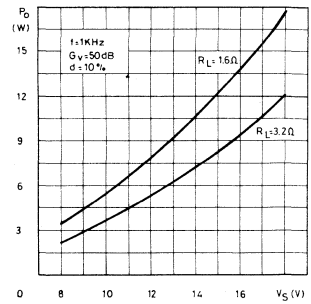



Fig. 8 - Distortion vs. frequency

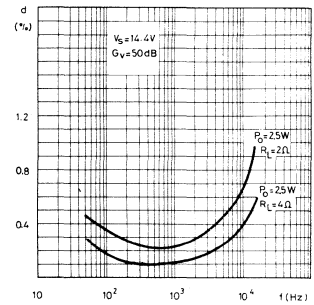


Fig. 9 - Distortion vs. frequency

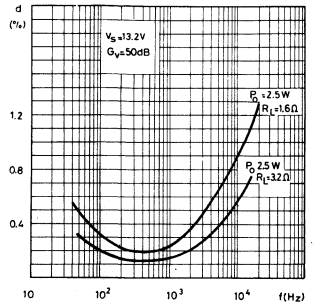



Fig. 10 - Supply voltage rejection vs. $C_3$

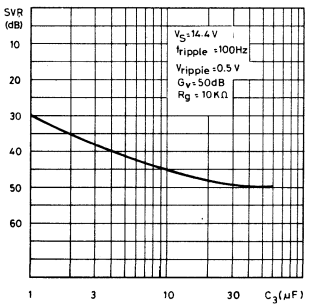



Fig. 11 - Supply voltage rejection vs. frequency

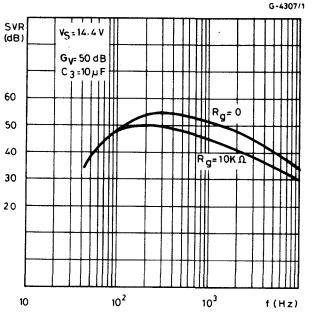



Fig. 12 - Supply voltage rejection vs. values of capacitors $C_2$ and $C_3$

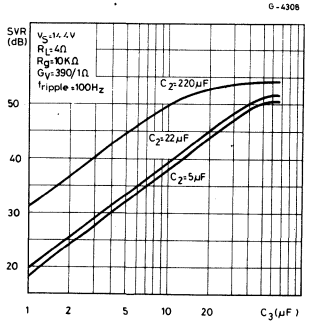



Fig. 13 - Supply voltage rejection vs. values of capacitors $C_2$ and $C_3$

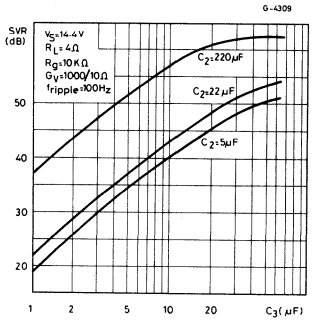



Fig. 14 - Gain vs. input sensitivity

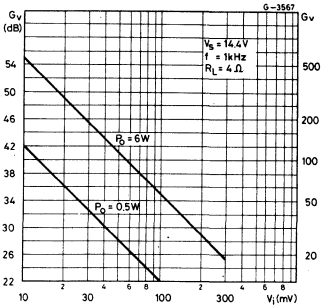



Fig. 15 - Gain vs. input sensitivity

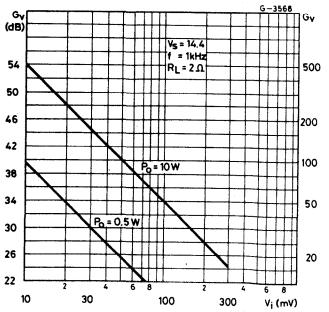



Fig. 16 - Total power dissipation and efficiency vs. output power

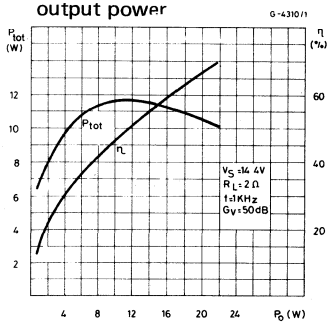
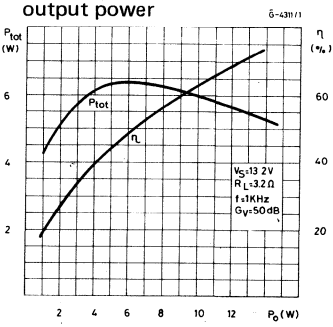



Fig. 17 - Total power dissipation and efficiency vs. output power



## APPLICATION SUGGESTION

The recommended values of the components are those shown on application circuit of fig. 1. Different values can be used; the following table can help the designer.

| Component | Recomm. value | Purpose | Larger than | Smaller than |
|---|---|---|---|---|
| $R_1$ | 120 KΩ | Optimisation of the output signal simmetry | Smaller $P_o$ max | Smaller $P_o$ max |
| $R_2$ and $R_4$ | 1 KΩ | Close loop gain setting | Increase of gain | Decrease of gain |
| $R_3$ and $R_5$ | 3.3 Ω | | Decrease of gain | Increase of gain |
| $R_6$ and $R_7$ | 1 Ω | Frequency stability | Danger of oscillation at high frequency with inductive load | |
| $C_1$ and $C_2$ | 2.2 μF | Input DC decoupling | High turn-on delay | High turn-on pop Higher low frequency cutoff. Increase of noise. |
| $C_3$ | 10 μF | Ripple rejection | Increase of SVR. Increase of the switch-on time. | Degradation of SVR. |
| $C_4$ and $C_6$ | 100 μF | Bootstrapping | | Increase of distortion at low frequency. |
| $C_5$ and $C_7$ | 100 μF | Feedback Input DC decoupling. | | |
| $C_8$ and $C_9$ | 0.1 μF | Frequency stability. | | Danger of oscillation. |
| $C_{10}$ and $C_{11}$ | 1000 μF to 2200 μF | Output DC decoupling. | | Higher low-frequency cut-off. |

## BUILT-IN PROTECTION SYSTEMS

### Load dump voltage surge

The TDA 2004 has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in fig. 19.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.
A suggested LC network is shown in fig. 18. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied to point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 18

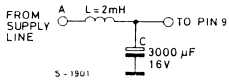
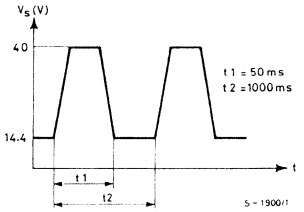



Fig. 19




### Short circuit (AC conditions)

The TDA 2004 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

### Polarity inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

### Open ground

When the radio is the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA 2004 protection diodes are included to avoid any damage.

### Inductive load

A protection diode is provided to allow use of the TDA 2004 with inductive loads.

### DC voltage

The maximum operating DC voltage on the TDA 2004 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

## BUILD-IN PROTECTION SYSTEMS (continued)

### Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that $P_o$ (and therefore $P_{tot}$) and $I_d$ are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 20 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 20 - Maximum allowable power dissipation vs. ambient temperature

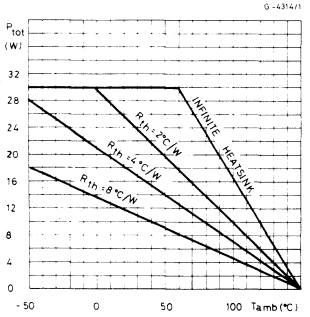



Fig. 21 - Output power and drain current vs. case temperature

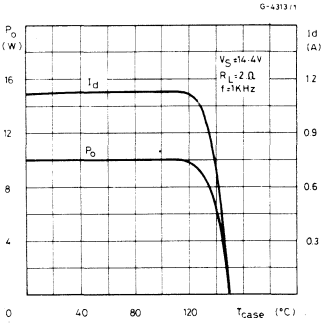
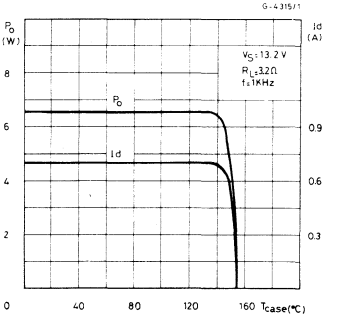



Fig. 22 - Output power and drain current vs. case temperature

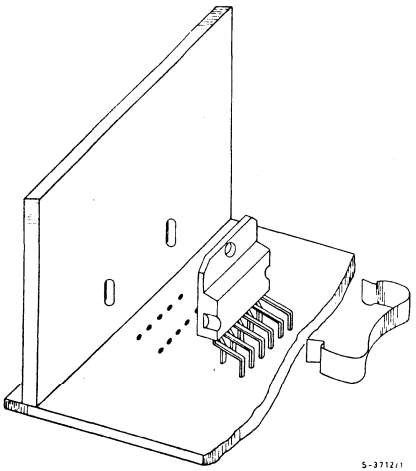


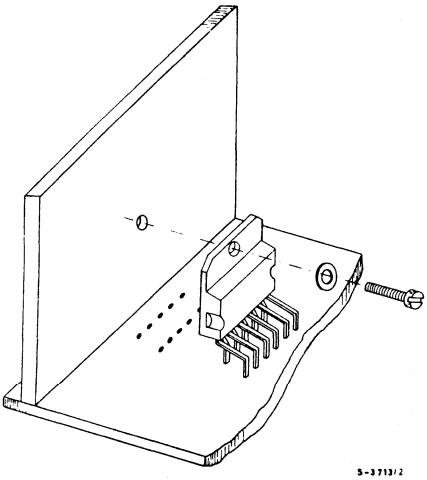

## MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

## MOUNTING INSTRUCTIONS (continued)

Fig. 23 - Mounting examples



# TDA2005

## 20 W BRIDGE AMPLIFIER FOR CAR RADIO

The TDA 2005 is a class B dual audio power amplifier in MULTIWATT® package specifically designed for car radio application: **power booster amplifiers** are easily designed using this device that provides a high current capability (up to 3.5A) and that can drive very low impedance loads (down to 1.6 Ω in stereo applications) obtaining an output power of more than 20W (bridge configuration).

**High output power:** $P_o = 10 + 10W$ @ $R_L = 2\Omega$, d = 10% ; $P_o = 20W$ @ $R_L = 4\Omega$, d = 10%

**High reliability** of the chip and package with additional complete safety during operation thanks to protection against:

- output DC and AC short circuit to ground.
- overrating chip temperature (150°C)
- load dump voltage surge.
- fortuitous open ground.
- polarity inversion.
- very inductive loads.

**Flexibility in use:** bridge or stereo booster amplifiers with or without bootstrap and with programmable gain and bandwidth.

**Space and cost saving:** very low number of external components, very simple mounting system with no electrical isolation between the package and the heatsink (one screw only).
In addition, the circuit offers **loudspeaker protection** during short circuit for one wire to ground.

## ABSOLUTE MAXIMUM RATINGS

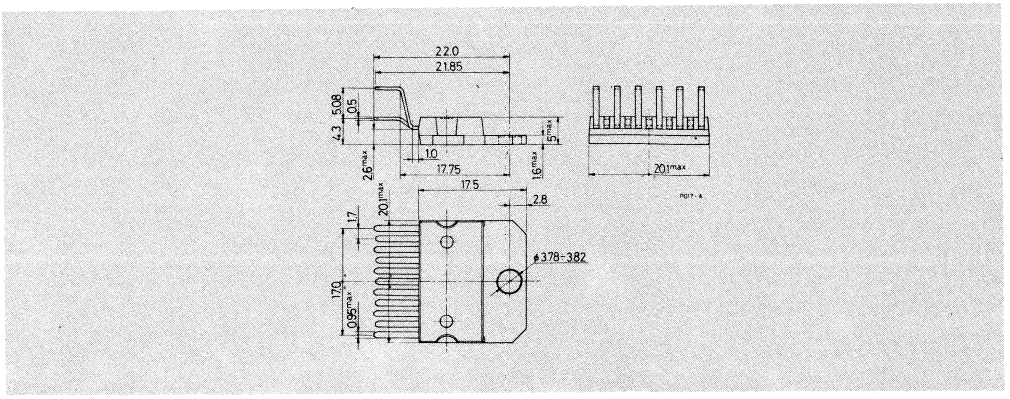
| | | | |
|---|---|---|---|
| $V_s$ | Operating supply voltage | 18 | V |
| $V_s$ | DC supply voltage | 28 | V |
| $V_s$ | Peak supply voltage (for 50 ms) | 40 | V |
| $I_o$ (*) | Output peak current (non repetitive t = 0.1 ms) | 4.5 | A |
| $I_o$ (*) | Output peak current (repetitive f ⩾ 10Hz) | 3.5 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$ = 60°C | 30 | W |
| $T_{stg}, T_j$ | Storage and junction temperature | -40 to 150° | C |

(*) The max. output current is internally limited

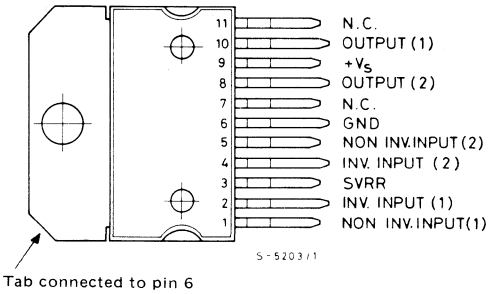
**ORDERING NUMBERS:** TDA 2005 M - Bridge application
TDA 2005 S - Stereo application

## MECHANICAL DATA

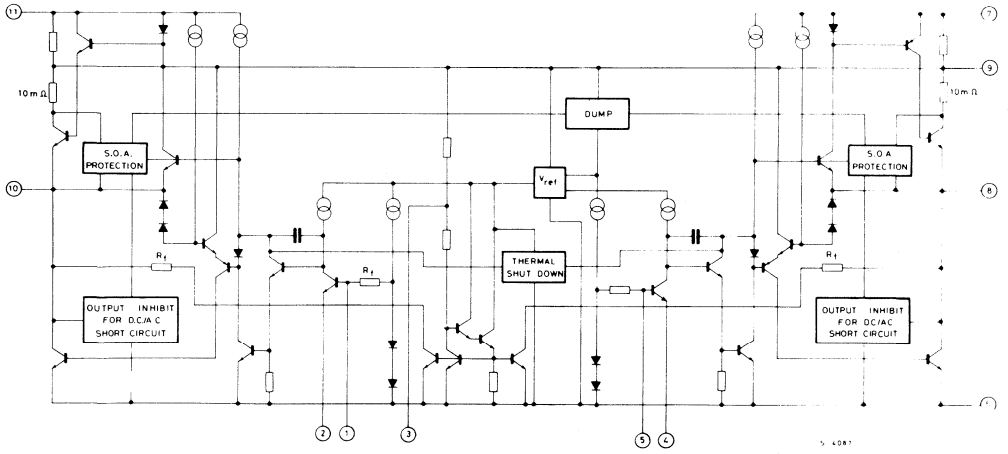
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## SCHEMATIC DIAGRAM




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

## BRIDGE AMPLIFIER APPLICATION (TDA 2005M)

Fig. 1 - Test and application circuit (Bridge amplifier)

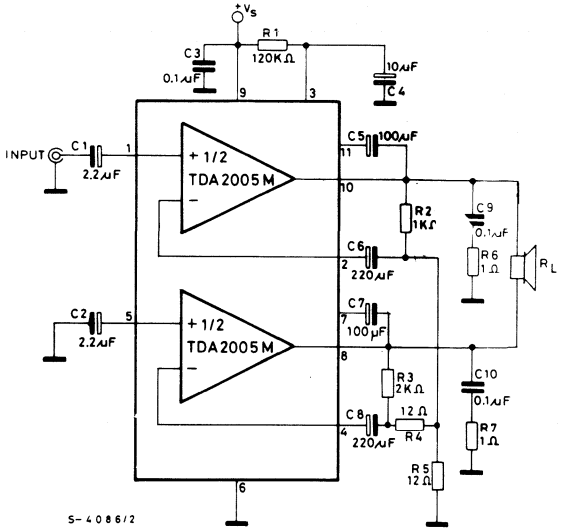
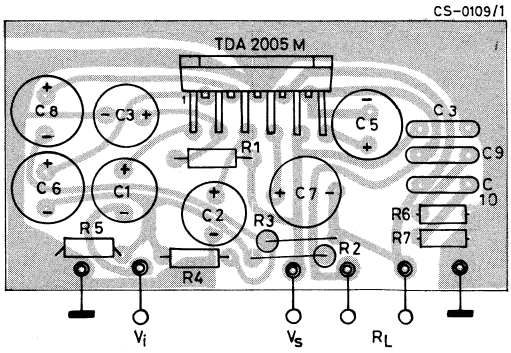



Fig. 2 - P.C. board and component layout (scale 1:1)



**ELECTRICAL CHARACTERISTICS** (Refer to the **bridge** application circuit, $T_{amb}$= 25°C, $G_v$= 50 dB, $R_{th\ (heatsink)}$= 4°C/W, unless otherwise specified).

| Parameters | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 8 | | 18 | V |
| $V_{os}$ | Output offset voltage(°) (between pin 8 and 10) | $V_s$ = 14.4V<br>$V_s$ = 13.2V | | | 150<br>150 | mV<br>mV |
| $I_d$ | Total quiescent drain current | $V_s$ = 14.4V $R_L$= 4Ω | | 75 | 150 | mA |
| | | $V_s$ = 13.2V $R_L$= 3.2 Ω | | 70 | 160 | mA |
| $P_o$ | Output power | d = 10% f = 1 KHz | | | | |
| | | $V_s$ = 14.4V $R_L$= 4Ω | 18 | 20 | | W |
| | | $R_L$= 3.2Ω | 20 | 22 | | W |
| | | $V_s$ = 13.2V $R_L$= 3.2Ω | 17 | 19 | | W |
| d | Distortion | f = 1 KHz<br>$V_s$ = 14.4V $R_L$= 4Ω<br>$P_o$ = 50 mW to 15W | | | 1 | % |
| | | $V_s$ = 13.2V $R_L$= 3.2Ω<br>$P_o$ = 50 mW to 13W | | | 1 | % |
| $V_i$ | Input sensitivity | f = 1 KHz<br>$P_o$ = 2W $R_L$= 4Ω | | 9 | | mV |
| | | $P_o$ = 2W $R_L$= 3.2Ω | | 8 | | mV |
| $R_i$ | Input resistance | f = 1 KHz | 70 | | | KΩ |
| $f_L$ | Low frequency roll off (-3 dB) | $R_L$= 3.2 Ω | | | 40 | Hz |
| $f_H$ | High frequency roll off (-3 dB) | $R_L$= 3.2 Ω | 20 | | | KHz |
| $G_v$ | Closed loop voltage gain | f = 1 KHz | | 50 | | dB |
| $e_N$ | Total input noise voltage | $R_g$= 10 KΩ(°°) | | 3 | 10 | μV |
| SVR | Supply voltage rejection | $R_g$= 10 KΩ $C_4$= 10 μF<br>$f_{ripple}$= 100 Hz<br>$V_{ripple}$= 0.5 V | 45 | 55 | | dB |
| η | Efficiency | $V_s$ = 14.4V f = 1 KHz<br>$P_o$ = 20W $R_L$= 4Ω | | 60 | | % |
| | | $P_o$ = 22W $R_L$= 3.2Ω | | 60 | | % |
| | | $V_s$ = 13.2V f = 1 KHz<br>$P_o$ = 19W $R_L$= 3.2Ω | | 58 | | % |
| $T_{sd}$ | Thermal shut-down case temperature | $V_s$ = 14.4V $R_L$= 4Ω<br>f = 1 KHz $P_{tot}$= 13W | 100 | 110 | | °C |
| $V_{OSH}$ | Output voltage with one side of the speaker shorted to ground | $V_s$ = 14.4V $R_L$= 4Ω<br>$V_s$ = 13.2V $R_L$= 3.2Ω | | | 2 | V |

(°) For TDA 2005M only.
(°°) Bandwidth filter: 22 Hz to 22 KHz.

Fig. 3 - Output offset voltage vs. supply voltage

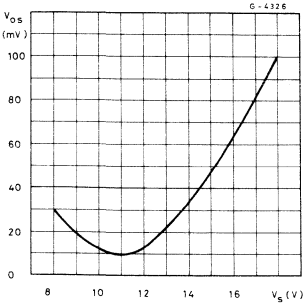



Fig. 4 - Distortion vs. output power (Bridge amplifier)

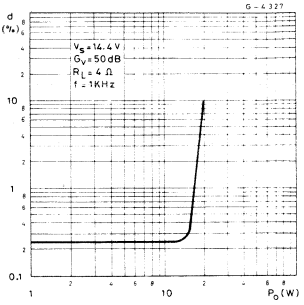
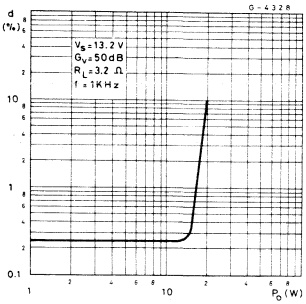



Fig. 5 - Distorsion vs. output power (Bridge amplifier)




## BRIDGE AMPLIFIER DESIGN

The following considerations can be useful when designing a bridge amplifier.

| Parameter | | Single ended | Bridge |
|---|---|---|---|
| $V_{o\ max}$ | Peak output voltage (before clipping) | $\frac{1}{2}(V_s - 2V_{CE\ sat})$ | $V_s - 2V_{CE\ sat}$ |
| $I_{o\ max}$ | Peak output current (before clipping) | $\frac{1}{2}\frac{(V_s - 2V_{CE\ sat})}{R_L}$ | $\frac{V_s - 2V_{CE\ sat}}{R_L}$ |
| $P_{o\ max}$ | rms output power (before clipping) | $\frac{1}{4}\frac{(V_s - 2V_{CE\ sat})^2}{2R_L}$ | $\frac{(V_s - 2V_{CE\ sat})^2}{2R_L}$ |

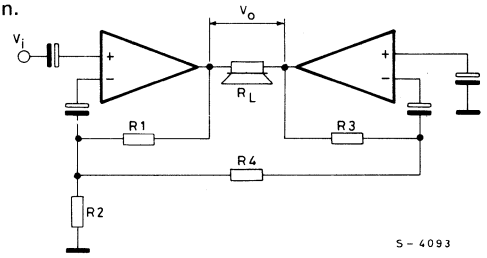
where: $V_{CE\ sat}$ = output transistors saturation voltage
$V_S$ = allowable supply voltage
$R_L$ = load impedance.

Voltage and current swings are twice for a bridge amplifier in comparison with single ended amplifier. In other words, with the same $R_L$ the bridge configuration can deliver an output power that is four times the output power of a single ended amplifier, while, with the same max output current the bridge configuration can deliver an output power that is twice the output power of a single ended amplifier. Care must be taken when selecting $V_s$ and $R_L$ in order to avoid an output peak current above the absolute maximum rating.
From the expression for $I_{o\ max}$, assuming $V_s$ = 14.4V and $V_{CEsat}$= 2V, the minimum load that can be driven by TDA 2005 in bridge configuration is:

$$R_{Lmin} = \frac{V_s - 2V_{CEsat}}{I_{o\ max}} = \frac{14.4 - 4}{3.5} = 2.97\ \Omega$$

## BRIDGE AMPLIFIER DESIGN (continued)

Fig. 6 - Bridge configuration.




The voltage gain of the bridge configuration is given by (see fig. 6):

$$G_v = \frac{V_o}{V_i} = 1 + \frac{R_1}{\left(\frac{R_2 \cdot R_4}{R_2 + R_4}\right)} + \frac{R_3}{R_4}$$

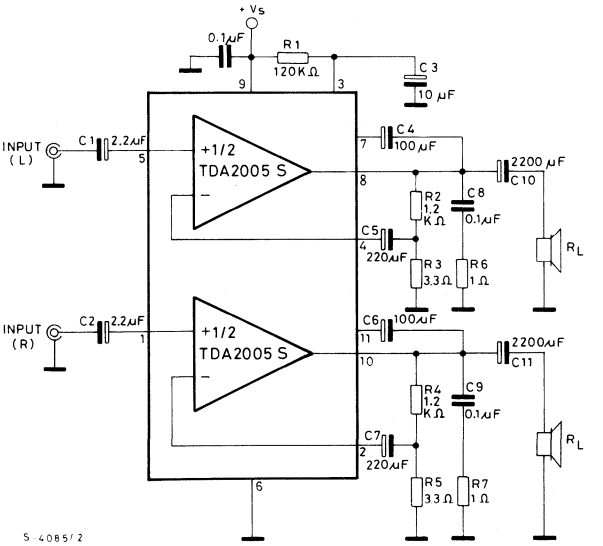
For sufficiently high gains (40 ÷ 50 dB) it is possible to put $R_2 = R_4$ and $R_3 = 2\,R_1$, simplifing the formula in:

$$G_v = 4\,\frac{R_1}{R_2}$$

| $G_v$ (dB) | $R_1$ (Ω) | $R_2 = R_4$ (Ω) | $R_3$ (Ω) |
|---|---|---|---|
| 40 | 1000 | 39 | 2000 |
| 50 | 1000 | 12 | 2000 |

## STEREO AMPLIFIER APPLICATION (TDA 2005S)

Fig. 7 - Typical application circuit



**ELECTRICAL CHARACTERISTICS** (Refer to the **stereo** application circuit, $T_{amb}$= 25°C, $G_v$= 50 dB, $R_{th\ (heatsink)}$= 4°C/W, unless otherwise specified).

| Parameters | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 8 | | 18 | V |
| $V_o$ | Quiescent output voltage | $V_s$ = 14.4V<br>$V_s$ = 13.2V | 6.6<br>6 | 7.2<br>6.6 | 7.8<br>7.2 | V<br>V |
| $I_d$ | Total quiescent drain current | $V_s$ = 14.4V<br>$V_s$ = 13.2V | | 65<br>62 | 120<br>120 | mA<br>mA |
| $P_o$ | Output power (each channel) | f = 1 KHz d = 10%<br>$V_s$ = 14.4V $R_L$= 4Ω<br>$R_L$= 3.2Ω<br>$R_L$= 2Ω<br>$R_L$= 1.6Ω<br>$V_s$ = 13.2V $R_L$= 3.2Ω<br>$R_L$= 1.6Ω<br>$V_s$ = 16V $R_L$= 2Ω | <br>6<br>7<br>9<br>10<br>6<br>9 | <br>6.5<br>8<br>10<br>11<br>6.5<br>10<br>12 | | <br>W<br>W<br>W<br>W<br>W<br>W<br>W |
| d | Distortion (each channel) | f = 1 KHz<br>$V_s$ = 14.4V $R_L$= 4Ω<br>$P_o$ = 50 mW to 4W<br>$V_s$ = 14.4V $R_L$= 2Ω<br>$P_o$ = 50 mW to 6W<br>$V_s$ = 13.2V $R_L$= 3.2Ω<br>$P_o$= 50 mW to 3W<br>$V_s$ = 13.2V $R_L$= 1.6Ω<br>$P_o$ = 40 mW to 6W | | <br>0.2<br>0.3<br>0.2<br>0.3 | <br>1<br>1<br>1<br>1 | <br>%<br>%<br>%<br>% |
| CT | Cross talk (°) | $V_s$= 14.4V $R_L$= 4Ω f = 1 KHz<br>$V_o$ = 4$V_{rms}$ $R_g$= 5 KΩ f = 10 KHz | | 60<br>45 | | dB<br>dB |
| $V_i$ | Input saturation voltage | | 300 | | | mV |
| $V_i$ | Input sensitivity | f = 1 KHz $P_o$ = 1W<br>$R_L$= 4Ω<br>$R_L$= 3.2Ω | | <br>6<br>5.5 | | mV |
| $R_i$ | Input resistance | f = 1 KHz non inverting input<br>inverting input | 70 | 200<br>10 | | KΩ<br>KΩ |
| $f_L$ | Low frequency roll off (-3 dB) | $R_L$= 2Ω | | | 50 | Hz |
| $f_H$ | High frequency roll off (-3 dB) | $R_L$= 2Ω | 15 | | | KHz |
| $G_v$ | Voltage gain (open loop) | f = 1 KHz | | 90 | | dB |
| $G_v$ | Voltage gain (closed loop) | f = 1 KHz | 48 | 50 | 51 | dB |
| $\Delta G_v$ | Closed loop gain matching | | | 0.5 | | dB |
| $e_N$ | Total input noise voltage | $R_g$= 10 KΩ (°°) | | 1.5 | 5 | μV |

(°) For TDA 2005S only.
(°°) Bandwidth filter: 22 Hz to 22 KHz.

## ELECTRICAL CHARACTERISTICS (continued)

| Parameters | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SVR | Supply voltage rejection | $R_g$= 10 KΩ $f_{ripple}$= 100 Hz<br>$C_3$= 10 μF $V_{ripple}$= 0.5V | 35 | 45 | | dB |
| η | Efficiency | $V_s$ = 14.4V f = 1 KHz<br>$R_L$= 4Ω $P_o$= 6.5W<br>$R_L$= 2Ω $P_o$= 10W<br>$V_s$ = 13.2V f = 1 KHz<br>$R_L$= 3.2Ω $P_o$= 6.5W<br>$R_L$= 1.6Ω $P_o$= 10W | | <br>70<br>60<br><br>70<br>60 | | <br>%<br>%<br><br>%<br>% |
| $T_{sd}$ | Thermal shut-down case temperature | $V_s$ = 14.4V $R_L$= 2Ω<br>$P_{tot}$= 6.6W | 120 | 130 | | °C |

Fig. 8 - Quiescent output voltage vs. supply voltage

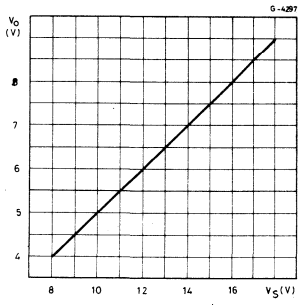



Fig. 9 - Quiescent drain current vs. supply voltage

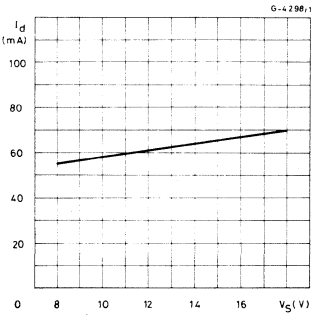



Fig. 10 - Distortion vs. output power

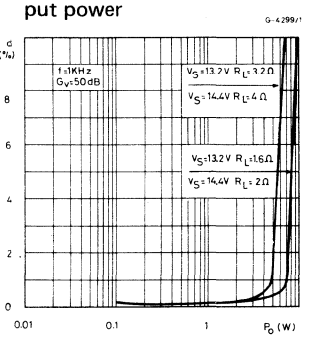



Fig. 11 - Output power vs. supply voltage

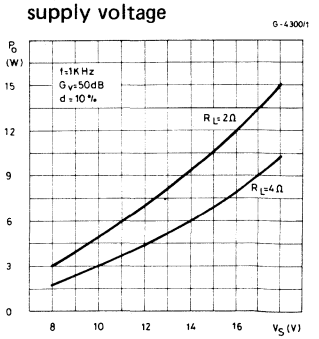



Fig. 12 - Output power vs. supply voltage

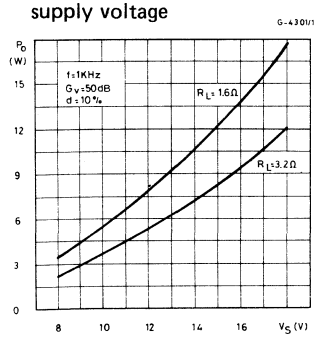



Fig. 13 - Distortion vs. frequency

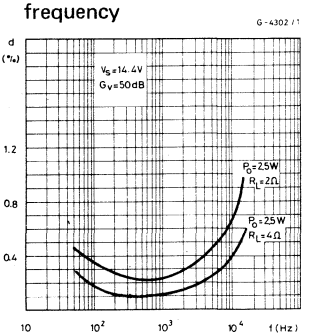


Fig. 14 - Distorsion vs. frequency

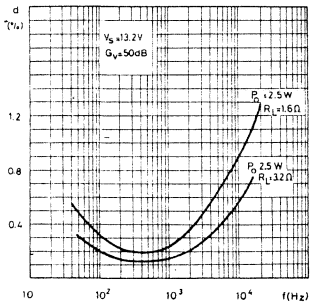



Fig. 15 - Supply voltage rejection vs. $C_3$

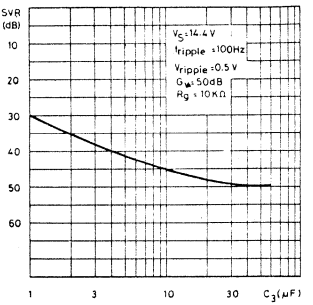



Fig. 16 - Supply voltage rejection vs. frequency

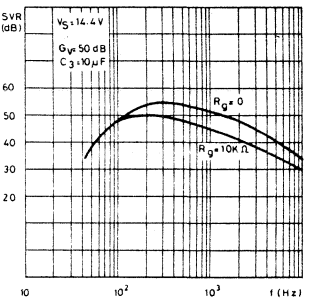



Fig. 17 - Supply voltage rejection vs. values of capacitors $C_2$ and $C_3$

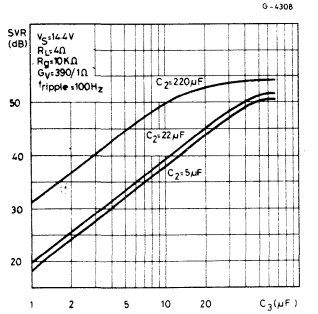



Fig. 18 - Supply voltage rejection vs. values of capacitors $C_2$ and $C_3$

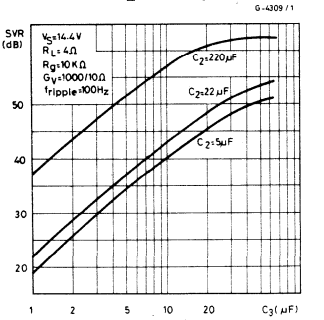



Fig. 19 - Gain vs. input sensitivity

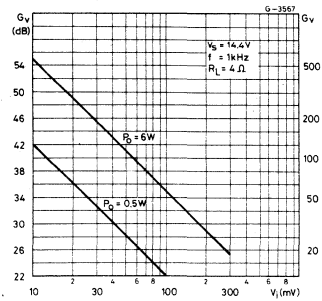



Fig. 20 - Gain vs. input sensitivity

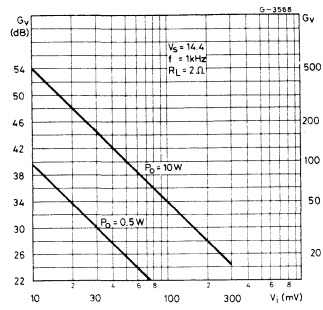



Fig. 21 - Total power dissipation and efficiency vs. output power (bridge)

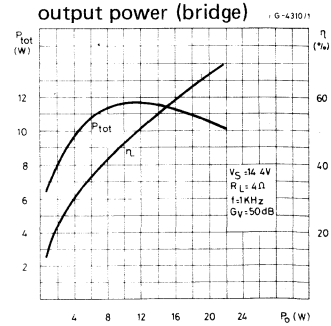
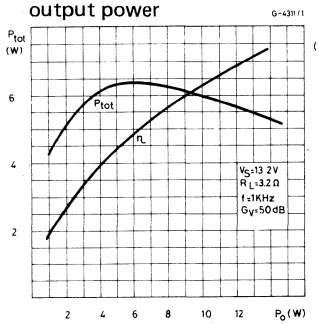



Fig. 22 - Total power dissipation and efficiency vs. output power



## APPLICATION INFORMATION

Fig. 23 - 10 + 10W stereo amplifier with tone balance and loudness control

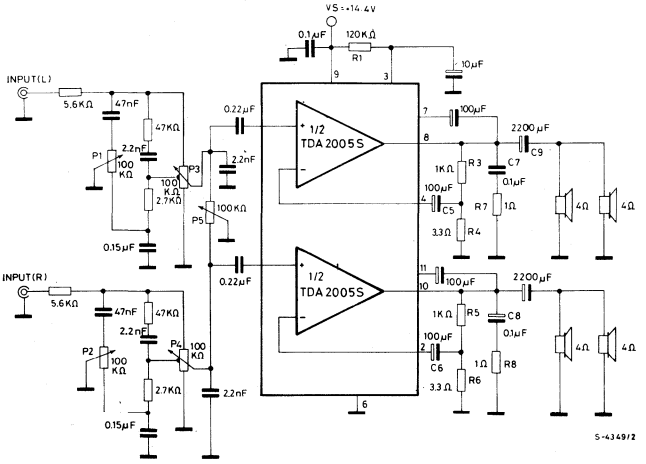



Fig. 24 - Tone control response (circuit of fig. 23)

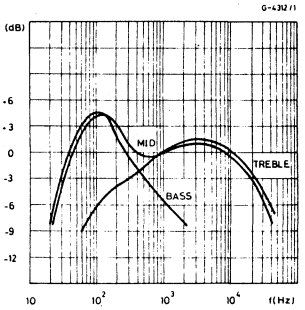



Fig. 25 - 20W Bus amplifier

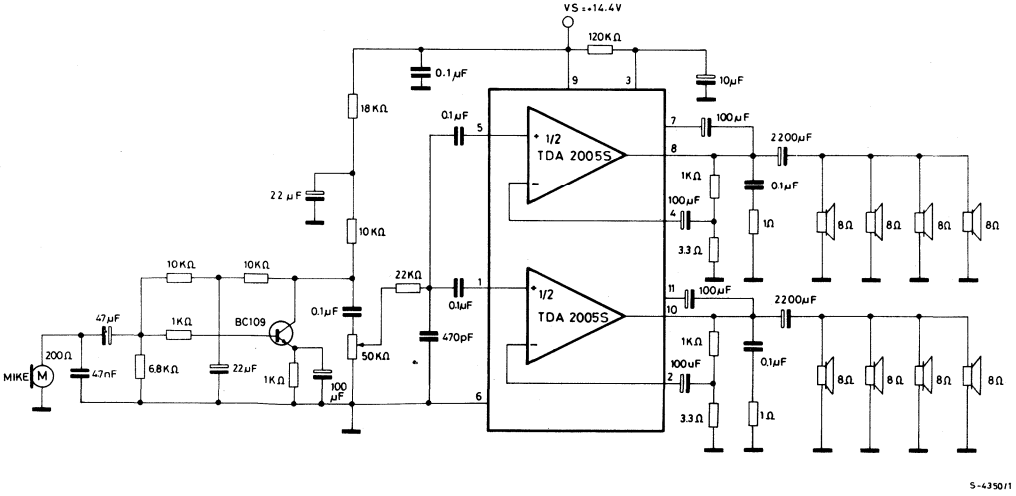


Fig. 26 - Simple 20W two way amplifier ($f_c$ = 2 KHz)

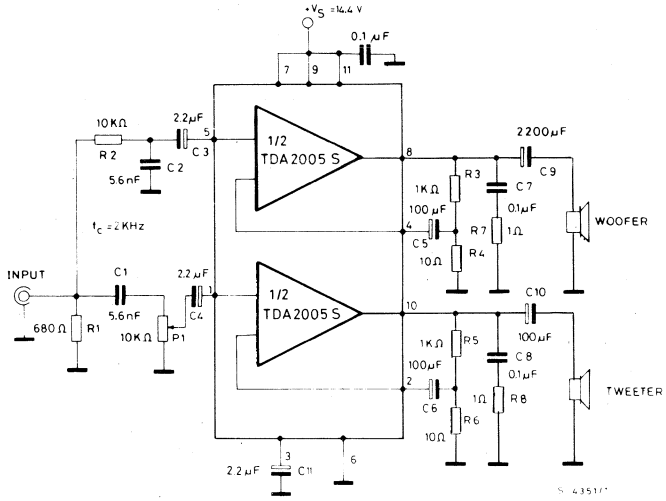
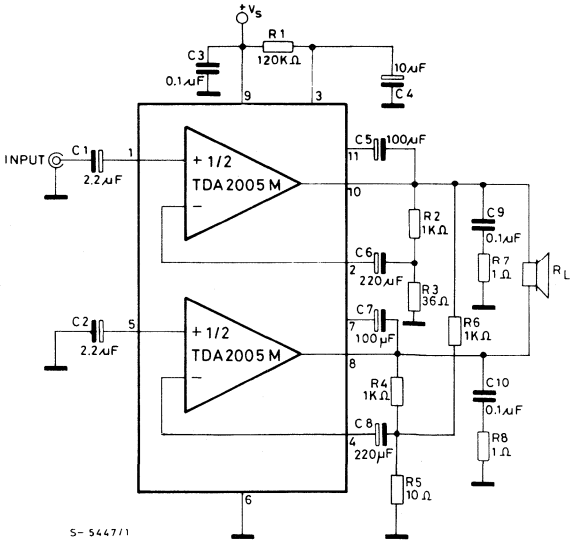



Fig. 27 - Bridge amplifier circuit suited for low-gain applications ($G_V$= 34 dB)



## APPLICATION SUGGESTION

The recommended values of the components are those shown on Bridge application circuit of fig. 1. Different values can be used, the following table can help the designer.

| Component | Recommended Value | Purpose | Larger than | Smaller than |
|---|---|---|---|---|
| $R_1$ | 120 KΩ | Optimization of the output symmetry | Smaller $P_o$ max | Smaller $P_o$ max |
| $R_2$ | 1 KΩ | Closed loop gain setting (see BRIDGE AMPLIFIER DESIGN) | | |
| $R_3$ | 2 KΩ | | | |
| $R_4$ and $R_5$ | 12 Ω | | | |
| $R_6$ and $R_7$ | 1 Ω | Frequency stability | Danger of oscillation at high frequency with inductive loads | |
| $C_1$ | 2.2 μF | Input DC decoupling | High turn on delay | Higher turn on pop. Higher low frequency cutoff. Increase of noise. |
| $C_2$ | 2.2 μF | Optimization of turn on pop and turn on delay. | | |
| $C_3$ | 0.1 μF | Supply by pass | | Danger of oscillation. |
| $C_4$ | 10 μF | Ripple Rejection | Increase of SVR. Increase of the switch-on time. | Degradation of SVR. |
| $C_5$ and $C_7$ | 100 μF | Bootstrapping | | Increase of distortion at low frequency. |
| $C_6$ and $C_8$ | 220 μF | Feedback input DC decoupling, low frequency cutoff. | | Higher low frequency cutoff. |
| $C_9$ and $C_{10}$ | 0.1 μF | Frequency stability. | | Danger of oscillation. |

## BUILT-IN PROTECTION SYSTEMS

### Load dump voltage surge

The TDA 2005 has a circuit which enables it to withstand a voltage pulse train, on pin 9, of the type shown in fig. 29.
If the supply voltage peaks to more than 40V, then an LC filter must be inserted between the supply and pin 9, in order to assure that the pulses at pin 9 will be held within the limits shown.
A suggested LC network is shown in fig. 28. With this network, a train of pulses with amplitude up to 120V and width of 2 ms can be applied at point A. This type of protection is ON when the supply voltage (pulse or DC) exceeds 18V. For this reason the maximum operating supply voltage is 18V.

Fig. 28

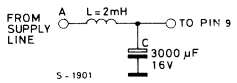
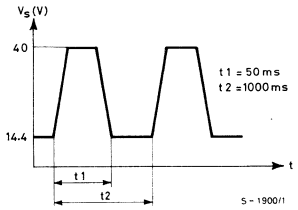



Fig. 29




### Short circuit (AC and DC conditions)

The TDA 2005 can withstand a permanent short-circuit on the output for a supply voltage up to 16V.

### Polarity inversion

High current (up to 10A) can be handled by the device with no damage for a longer period than the blow-out time of a quick 2A fuse (normally connected in series with the supply). This feature is added to avoid destruction, if during fitting to the car, a mistake on the connection of the supply is made.

### Open ground

When the radio is in the ON condition and the ground is accidentally opened, a standard audio amplifier will be damaged. On the TDA 2005 protection diodes are included to avoid any damage.

### Inductive load

A protection diode is provided to allow use of the TDA 2005 with inductive loads.

### DC voltage

The maximum operating DC voltage for the TDA 2005 is 18V.
However the device can withstand a DC voltage up to 28V with no damage. This could occur during winter if two batteries are series connected to crank the engine.

### Thermal shut-down

The presence of a thermal limiting circuit offers the following advantages:

1) an overload on the output (even if it is permanent), or an excessive ambient temperature can be easily withstood.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that $P_o$ (and therefore $P_{tot}$) and $I_d$ are reduced.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 30 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 30 - Maximum allowable power dissipation vs. ambient temperature

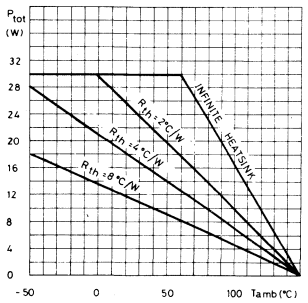



Fig. 31 - Output power and drain current vs. case temperature

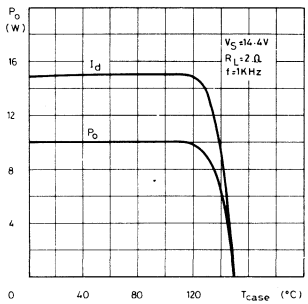
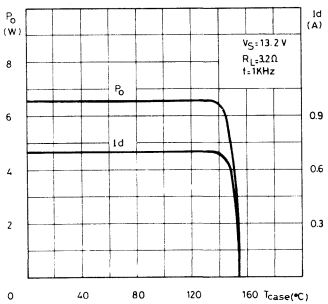



Fig. 32 - Output power and drain current vs. case temperature



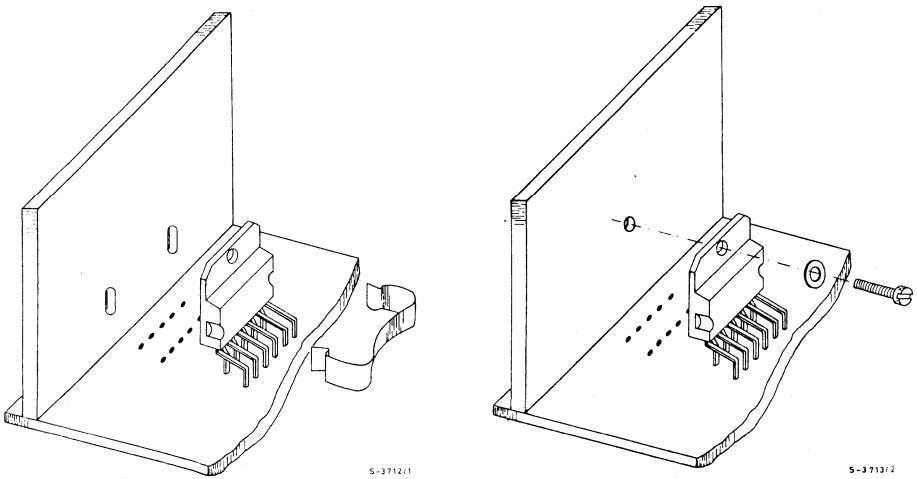

## Loudspeaker protection

The circuit offers loudspeaker protection during short circuit for one wire to ground.

## MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 33 - Mounting examples



# LINEAR INTEGRATED CIRCUITS

**TDA2006**

## 10W AUDIO AMPLIFIER

The TDA 2006 is a monolithic integrated circuit in Pentawatt® package, intended for use as a low frequency class "AB" amplifier. At ± 12V, d = 10% typically it provides 12W output power on a 4Ω load and 8W on a 8Ω. The TDA 2006 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA 2006 is pin to pin equivalent to the TDA 2030.

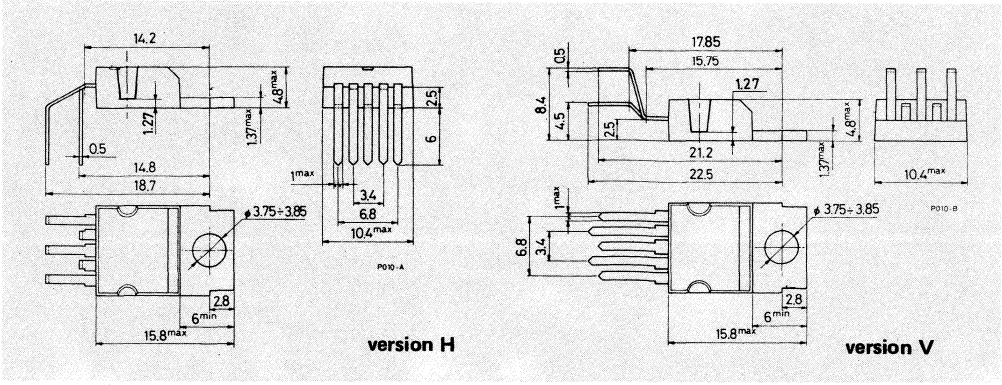
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | ± 15 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential input voltage | ± 12 | V |
| $I_o$ | Output peak current (internally limited) | 3 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$ = 90°C | 20 | W |
| $T_{stg}, T_j$ | Storage and junction temperature | -40 to 150 | °C |

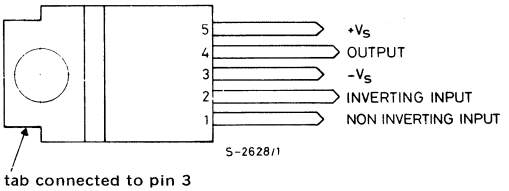
**ORDERING NUMBERS:** TDA 2006H; TDA 2006V

## MECHANICAL DATA

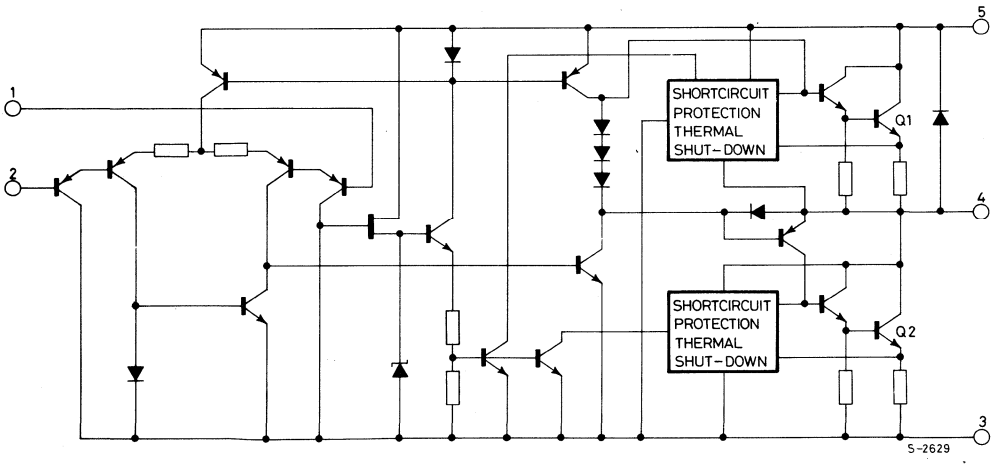
Dimensions in mm



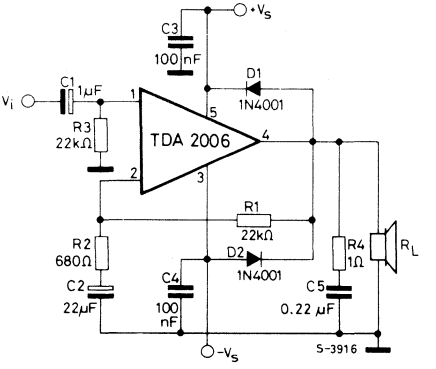
## CONNECTION DIAGRAM




## SCHEMATIC DIAGRAM



## TEST AND APPLICATION CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\text{-}j\ case}$ | Thermal resistance junction-case | max | 3 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit; $V_s$= ±12V, $T_{amb}$= 25°C unless otherwise specified)

| Parameters | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | ± 6 | | ± 15 | V |
| $I_d$ | Quiescent drain current | $V_s$ = ± 15V | | 40 | 80 | mA |
| $I_b$ | Input bias current | | | 0.2 | 3 | µA |
| $V_{OS}$ | Input offset voltage | | | ± 8 | | mV |
| $I_{OS}$ | Input offset current | | | ± 80 | | nA |
| $V_{OS}$ | Output offset voltage | | | ± 10 | ± 100 | mV |
| $P_o$ | Output power | d = 10%<br>f = 1 KHz<br>$R_L$= 4Ω<br>$R_L$= 8Ω | <br><br><br>6 | <br><br>12<br>8 | | <br><br>W<br>W |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| d | Distortion | $P_o$= 0.1 to 8W<br>$R_L$= 4Ω<br>f = 1 KHz | | 0.2 | | % |
| | | $P_o$= 0.1 to 4W<br>$R_L$= 8Ω<br>f = 1 KHz | | 0.1 | 1 | % |
| $V_i$ | Input sensitivity | f = 1 KHz<br>$P_o$= 10W $R_L$= 4Ω<br>$P_o$= 6W $R_L$= 8Ω | | 200<br>220 | | mV<br>mV |
| B | Frequency response (-3 dB) | $P_o$= 8W $R_L$= 4Ω | 10 to 140,000 | | | Hz |
| $R_i$ | Input resistance (pin 1) | f = 1 KHz | 0.5 | 5 | | MΩ |
| $G_v$ | Voltage gain (open loop) | | | 75 | | dB |
| $G_v$ | Voltage gain (closed loop) | | 29.5 | 30 | 30.5 | dB |
| $e_N$ | Input noise voltage | B (-3 dB) = 22Hz to 22kHz<br>$R_L$= 4Ω | | 3 | 10 | μV |
| $i_N$ | Input noise current | | | 80 | 200 | pA |
| SVR | Supply voltage rejection | $R_L$= 4Ω<br>$R_g$= 22 KΩ<br>$f_{ripple}$= 100 Hz (*) | 40 | 50 | | dB |
| $I_d$ | Drain current | $P_o$= 12W $R_L$= 4Ω<br>$P_o$= 8W $R_L$= 8Ω | | 850<br>500 | | mA<br>mA |
| $T_j$ | Thermal shut down junction temperature | | | 145 | | °C |

(*) Referring to fig. 15, single supply.

Fig. 1 - Output power vs. supply voltage

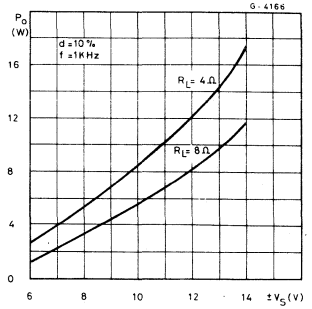



Fig. 2 - Distortion vs. output power

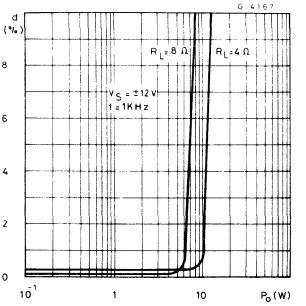



Fig. 3 - Distortion vs. frequency

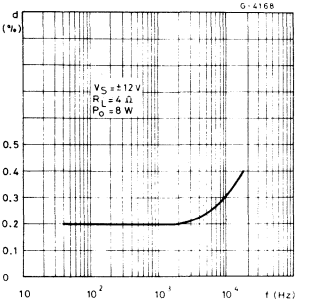



Fig. 4 - Distortion vs. frequency

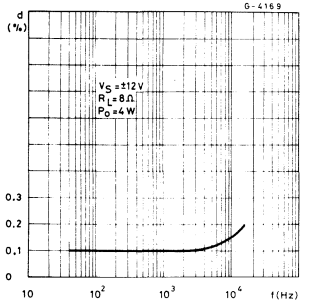



Fig. 5 - Sensitivity vs. output power

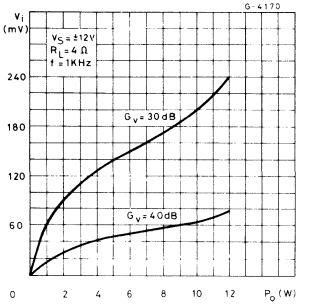



Fig. 6 - Sensitivity vs. output power

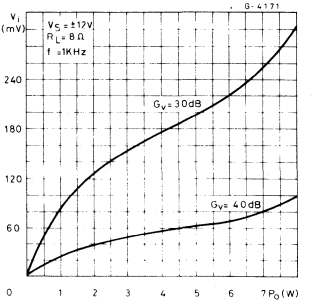



Fig. 7 - Frequency response with different values of the rolloff capacitor $C_8$ (see fig. 13)

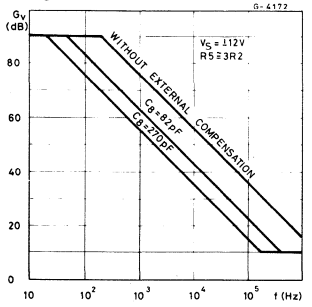



Fig. 8 - Value of $C_8$ vs. voltage gain for different bandwidths (see fig. 13)

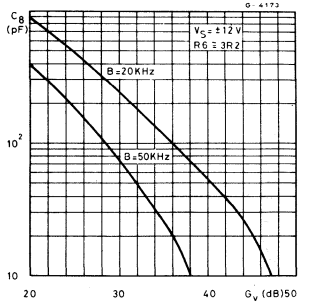



Fig. 9 - Quiescent current vs. supply voltage

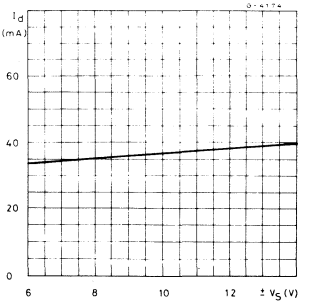


Fig. 10 - Supply voltage rejection vs. voltage gain

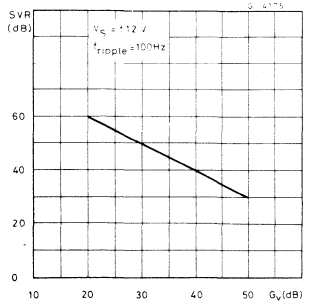



Fig. 11 - Power dissipation and efficiency vs. output power

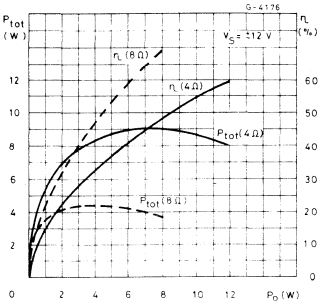



Fig. 12 - Maximum power dissipation vs. supply voltage (sine wave operation)

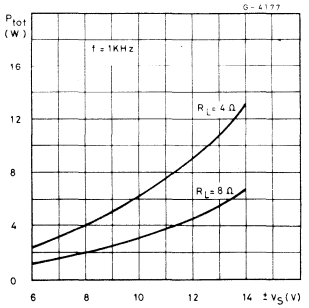



Fig. 13 - Application circuit with split power supply

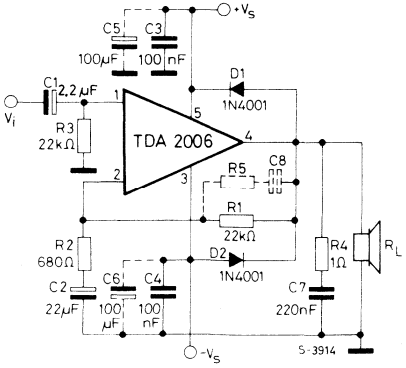



Fig. 14 - P.C. board and component layout for the circuit of fig. 13

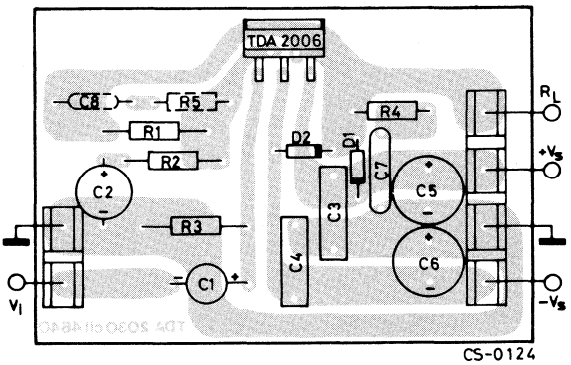


Fig. 15 - Application circuit with single power supply

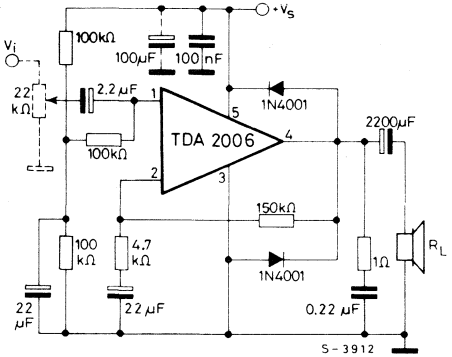



Fig. 16 - P.C. board and component layout for the circuit of fig. 15

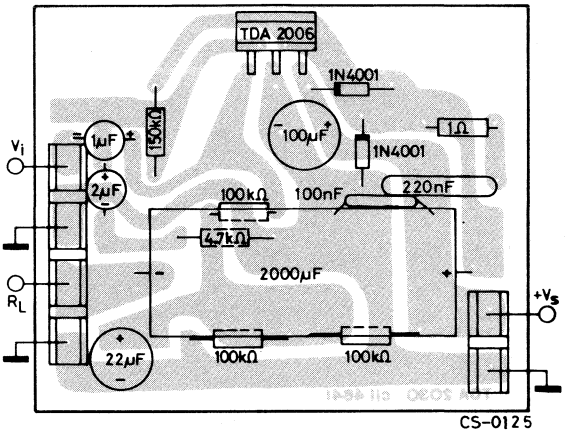
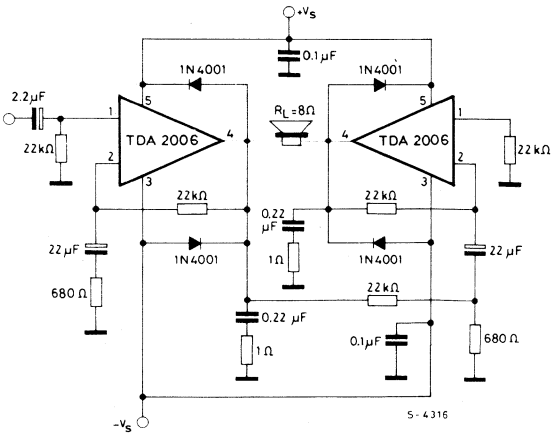



Fig. 17 - Bridge amplifier configuration with split power supply (Po = 24W, $V_S = \pm 12V$)



## PRACTICAL CONSIDERATION

### Printed circuit board

The layout shown in fig. 14 should be adopted by the designers. If different layout are used, the ground points of input 1 and input 2 must be well decoupled from ground of the output on which a rather high current flows.

### Assembly suggestion

No electrical isolation is needed between the package and the heat-sink with single supply voltage configuration.

### Application suggestion

The recommended values of the components are the ones shown on application circuits of fig. 13. Different values can be used. The following table can help the designers.

| Component | Recommended value | Purpose | Larger than recommended value | Smaller than recommended value |
|---|---|---|---|---|
| $R_1$ | 22 KΩ | Closed loop gain setting | Increase of gain | Decrease of gain |
| $R_2$ | 680Ω | Closed loop gain setting | Decrease of gain | Increase pf gain |
| $R_3$ | 22 KΩ | Non inverting input biasing | Increase of input impedance | Decrease of input impedance |
| $R_4$ | 1Ω | Frequency stability | Danger of oscillation at high frequencies with inductive loads | |
| $R_5$ | $3\,R_2$ | Upper frequency cutoff | Poor high frequencies attenuation | Danger of oscillation |
| $C_1$ | 2.2 μF | Input DC decoupling | | Increase of low freqencies cut off |
| $C_2$ | 22 μF | Inverting input DC decoupling | | Increase of low frequencies cutoff |
| $C_3C_4$ | 0.1 μF | Supply voltage by pass | | Danger of oscillation |
| $C_5C_6$ | 100 μF | Supply voltage by pass | | Danger of oscillation |
| $C_7$ | 0.22 μF | Frequency stability | | Danger of oscillation |
| $C_8$ | $\frac{1}{2\pi BR_1}$ | Upper frequency cutoff | Lower bandwidth | Larger bandwidth |
| $D_1D_2$ | 1N4001 | To protect the device against output voltage spikes. | | |

## SHORT CIRCUIT PROTECTION

The TDA 2006 has an original circuit which limits the current of the output transistors. Fig. 18 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (fig. 19).
This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2006 is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time, the thermal shutdown protection keeps the junction temperature within safe limits.

Fig. 18 - Maximum output current vs. voltage $V_{Ce(sat)}$ across each output transistor

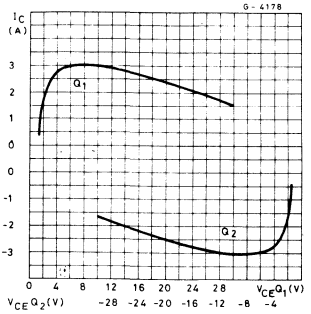
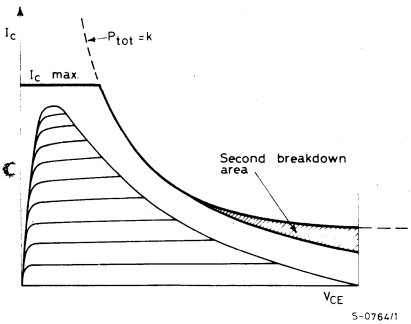



Fig. 19 - Safe operating area and collector characteristics of the protected power transistor




## THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the $T_j$ cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

   If for any reason, the junction temperature increases up to 150°C, the thermal shutdown simply reduces the power dissipation and the current consumption.

Fig. 20 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

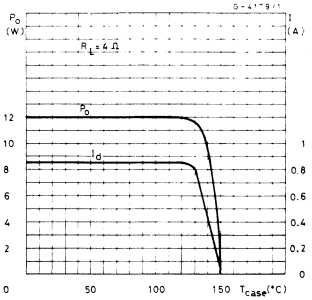
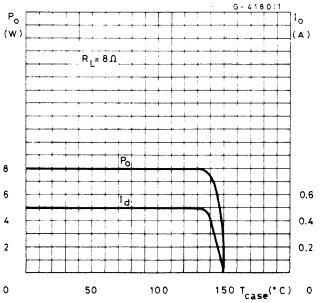



Fig. 21 - Output power and drain current vs. case temperature ($R_L = 8\Omega$)




The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 22 shows this dissipable power as a function of ambient temperature for different thermal resistances.

Fig. 22 - Maximum allowable power dissipation vs. ambient temperature

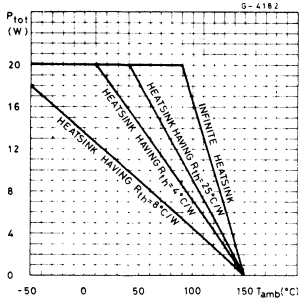
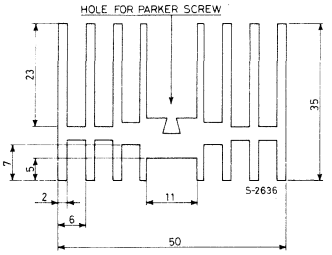



Fig. 23 - Example of heatsink




**Dimension suggestion**

The following table shows the lenght of the heatsink in fig. 23 for several values of $P_{tot}$ and $R_{th}$.

| $P_{tot}$ (W) | 12 | 8 | 6 |
|---|---|---|---|
| Lenght of heatsink (mm) | 60 | 40 | 30 |
| $R_{th}$ of heatsink (°C/W) | 4.2 | 6.2 | 8.3 |

# TDA2008

## 12W AUDIO AMPLIFIER ($V_s$ = 22V, $R_L$ = 4Ω)

The TDA 2008 is a monolithic class B audio power amplifier in Pentawatt® package designed for driving low impedance loads (down to 3.2Ω). The device provides a high output current capability (up to 3A), very low harmonic and crossover distortion.
In addition, the device offers the following features:

- very low number of external components
- assembly ease, due to Pentawatt® power package with no electrical insulation requirement
- space and cost saving
- high reliability
- flexibility in use
- thermal protection

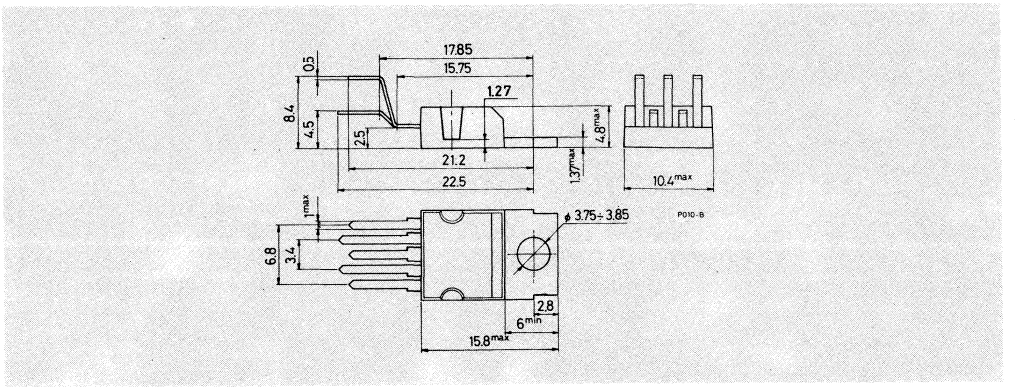
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | DC supply voltage | 28 | V |
| $I_o$ | Output peak current (repetitive) | 3 | A |
| $I_o$ | Output peak current (non repetitive) | 4 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$ = 90°C | 20 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

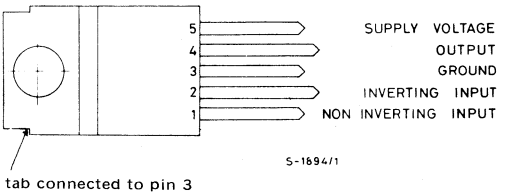
**ORDERING NUMBERS:** TDA 2008V

## MECHANICAL DATA

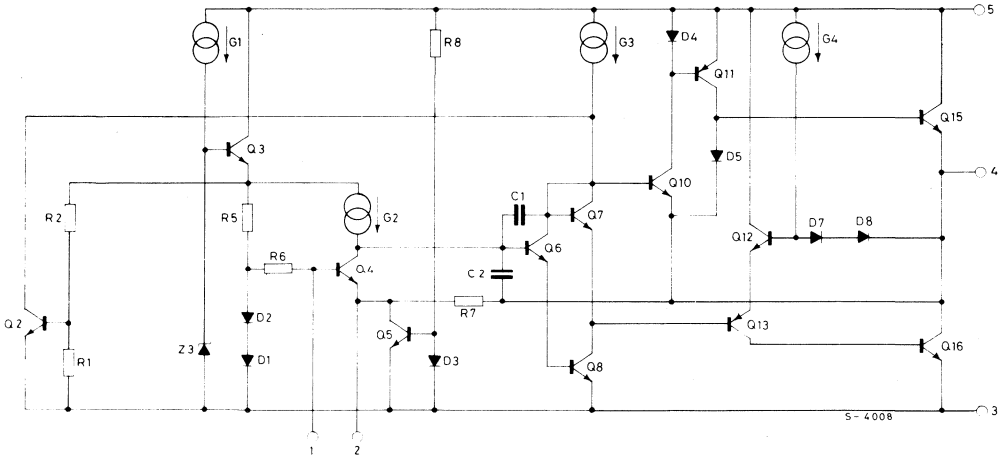
Dimensions in mm



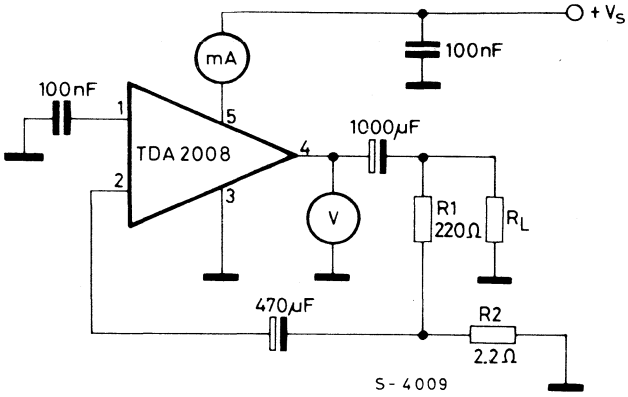
## CONNECTION DIAGRAM (top view)



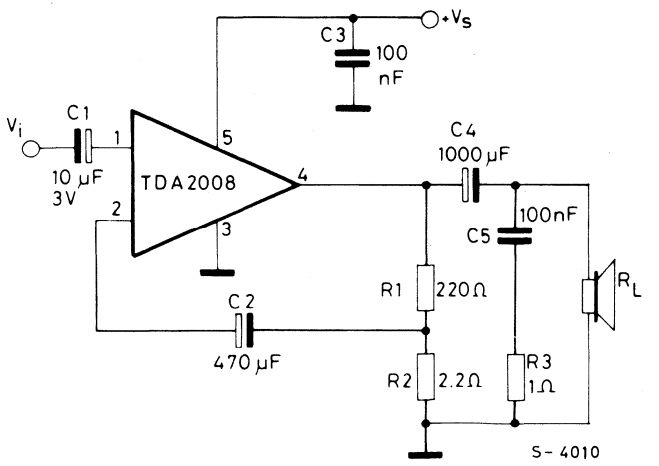

## SCHEMATIC DIAGRAM



## DC TEST CIRCUIT




## AC TEST CIRCUIT



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_s$ = 22V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | 10 | | 28 | V |
| $V_o$ | Quiescent output voltage (pin 4) | | | | 10.5 | | V |
| $I_d$ | Quiescent drain current (pin 5) | | | | 65 | 115 | mA |
| $P_o$ | Output power | d = 10% | $R_L$ = 8Ω | | 8 | | W |
| | | f = 1 KHz | $R_L$ = 4Ω | 10 | 12 | | W |
| $V_i$ (RMS) | Input saturation voltage | | | 300 | | | mV |
| $V_i$ | Input sensitivity | f = 1 KHz<br>$P_o$ = 0.5W<br>$P_o$ = 8W<br>$P_o$ = 0.5W<br>$P_o$ = 12W | <br>$R_L$ = 8Ω<br>$R_L$ = 8Ω<br>$R_L$ = 4Ω<br>$R_L$ = 4Ω | | <br>20<br>80<br>14<br>70 | | <br>mV<br>mV<br>mV<br>mV |
| B | Frequency response (-3 dB) | $P_o$ = 1W<br>$R_L$ = 4Ω | | 40 to 15 000 | | | Hz |
| d | Distortion | f = 1 KHz<br>$P_o$ = 0.05 to 4W<br>$P_o$ = 0.05 to 6W | <br>$R_L$ = 8Ω<br>$R_L$ = 4Ω | | <br>0.15<br>0.15 | | <br>%<br>% |
| $R_i$ | Input resistance (pin 1) | f = 1 KHz | | 70 | 150 | | KΩ |
| $G_v$ | Voltage gain (open loop) | f = 1 KHz | $R_L$ = 8Ω | | 80 | | dB |
| $G_v$ | Voltage gain (closed loop) | | | 39.5 | 40 | 40.5 | dB |
| $e_N$ | Input noise voltage | BW= 22Hz to 22 KHz | | | 1 | 5 | μV |
| $i_N$ | Input noise current | | | | 60 | 200 | pA |
| SVR | Supply voltage rejection | $V_{ripple}$ = 0.5V<br>$R_g$ = 10KΩ<br>$R_L$ = 4Ω | f = 100 Hz | 30 | 36 | | dB |
| | | | f = 15 KHz | | 36 | | dB |

## APPLICATION INFORMATION

Fig. 1 - Typical application circuit

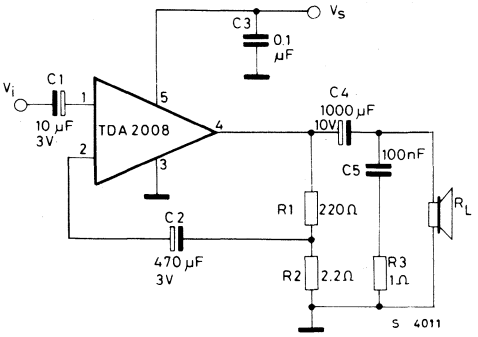



Fig. 2 - P.C. board and component layout for the circuit of fig. 1 (1:1 scale)

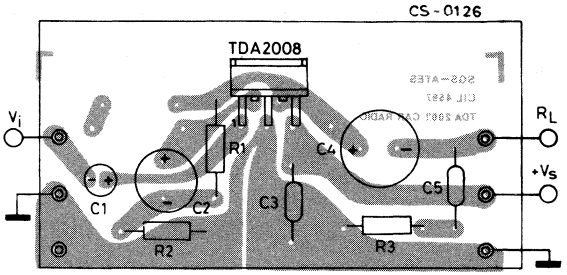



Fig. 3 - 25W bridge configuration application circuit (°)

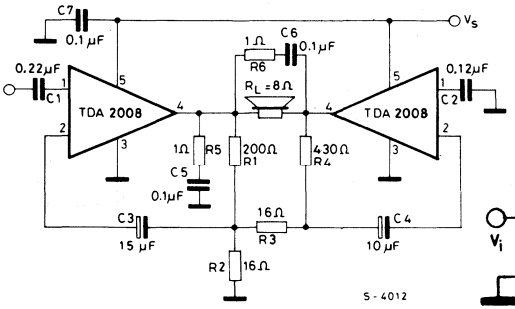
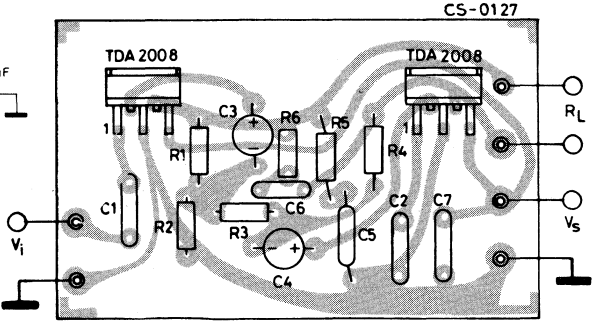



Fig. 4 - P.C. board and component layout for the circuit of fig. 3 (1:1 scale)




(°) The value of the capacitors C3 and C4 are different to optimize the SVR (Typ. = 40 dB)

# TDA2009

# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## 10 + 10W HIGH QUALITY STEREO AMPLIFIER

The TDA 2009 is class AB dual Hi-Fi Audio power amplifier assembled in Multiwatt® package, specially designed for high quality stereo applications as Hi-Fi TV and music centers. Its main features are:

- High output power (10 + 10W min. @ d = 0.5%)
- High current capability (up to 3.5A)
- Thermal overload protection
- Space and cost saving: very low number of external components and simple mounting thanks to the Multiwatt® package.

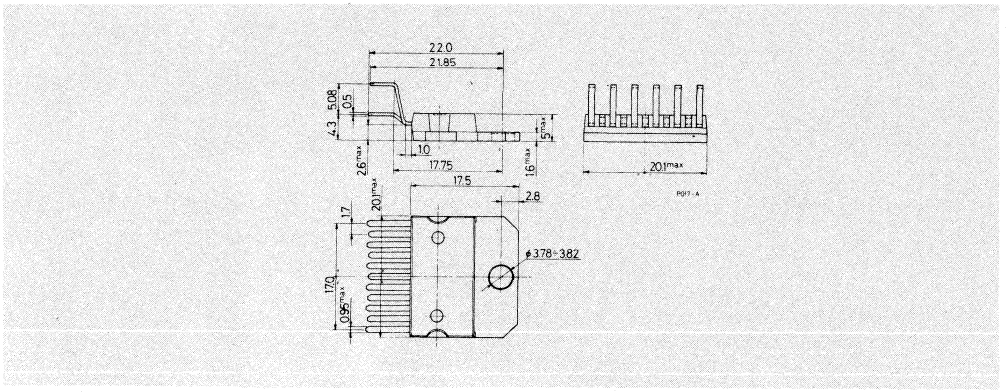
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 28 | V |
| $I_o$ | Output peak current (repetitive f ⩾ 20 Hz) | 3.5 | A |
| $I_o$ | Output peak current (non repetitive, t = 100 μs) | 4.5 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$ = 90°C | 20 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

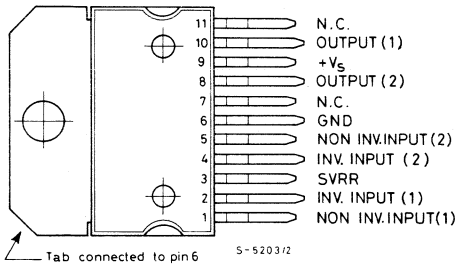
**ORDERING NUMBER:** TDA 2009

## MECHANICAL DATA

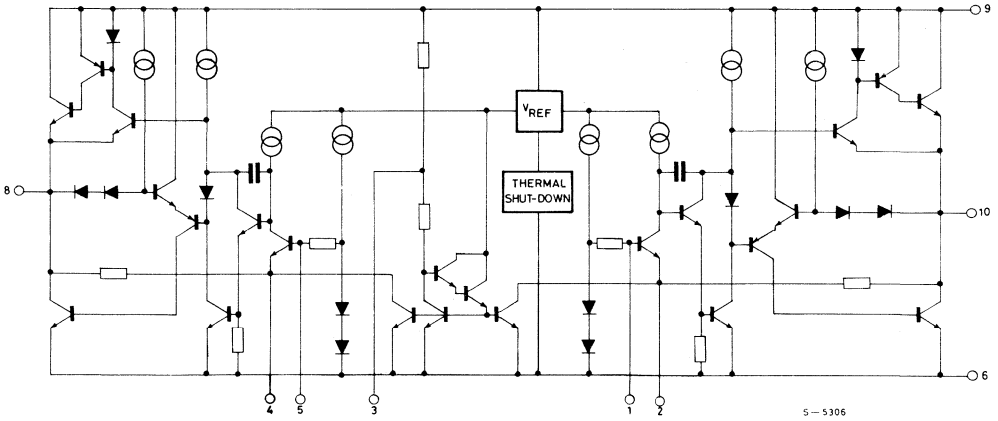
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## SCHEMATIC DIAGRAM




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

Fig. 1 - Test and application circuit ($G_v$ = 36 dB)

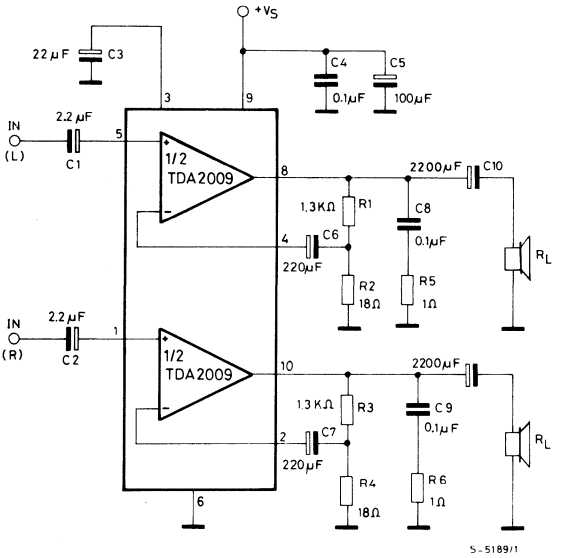
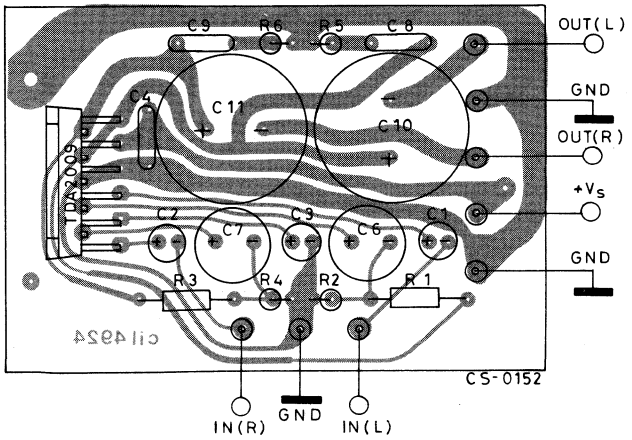



Fig. 2 - P.C. board and components layout of the circuit of fig. 1 (1 : 1 scale)



**ELECTRICAL CHARACTERISTICS** (Refer to the **stereo** application circuit, $T_{amb}$= 25°C, $G_v$ = 36 dB, unless otherwise specified)

| Parameters | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | 8 | | 28 | V |
| $V_o$ | Quiescent output voltage | $V_s$ = 23V | | | 11 | | V |
| $I_d$ | Total quiescent drain current | $V_s$ = 23V | | | 80 | 120 | mA |
| $P_o$ | Output power (each channel) | f = 50 Hz to 16 KHz<br>d = 0.5%<br>$V_s$ = 23V $R_L$= 4 Ω<br>$R_L$= 8 Ω<br>$V_s$ = 18V $R_L$= 4 Ω<br>$R_L$= 8 Ω | | 10<br><br>5.5 | 11<br>7<br>6.5<br>4 | | W<br>W<br>W<br>W |
| d | Distortion (each channel) | f = 1 KHz<br>$V_s$ = 23V $R_L$= 4 Ω<br>$P_o$= 100 mW to 8W<br>$V_s$ = 23V $R_L$= 8 Ω<br>$P_o$= 100 mW to 3W | | | 0.1<br><br>0.05 | | % |
| CT | Cross talk (°°°) | $R_L$= ∞ | f = 1 KHz | | 60 | | dB |
| | | $R_g$ = 10 KΩ | f = 10 KHz | | 50 | | dB |
| $V_i$ | Input saturation voltage (rms) | | | 300 | | | mV |
| $R_i$ | Input resistance | f = 1 KHz | non inverting input | 70 | 200 | | KΩ |
| | | | inverting input | | 10 | | KΩ |
| $f_L$ | Low frequency roll off (-3 dB) | $R_L$ = 4Ω | | | 20 | | Hz |
| $f_H$ | High frequency roll off (-3 dB) | | | | 80 | | KHz |
| $G_v$ | Voltage gain (open loop) | f = 1 KHz | | | 85 | | dB |
| $G_v$ | Voltage gain (closed loop) | f = 1 KHz | | 35.5 | 36 | 36.5 | dB |
| $\Delta G_v$ | Closed loop gain matching | | | | 0.5 | | dB |
| $e_N$ | Total input noise voltage | $R_g$ = 10 KΩ (°) | | | 1.5 | | μV |
| | | $R_g$ = 10 KΩ (°°) | | | 2.5 | 8 | μV |
| SVR | Supply voltage rejection (each channel) | $R_g$ = 10 KΩ<br>$f_{ripple}$= 100 Hz<br>$V_{ripple}$= 0.5V | | | 55 | | dB |
| $T_J$ | Thermal shut-down junction temperature | | | | 145 | | °C |

(°) Curve A. (°°) 22 Hz to 22 KHz. (°°°) Optimized test box.

Fig. 3 - Output power vs. supply voltage

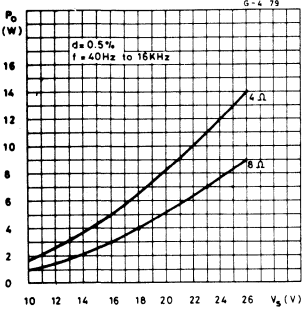



Fig. 4 - Output power vs. supply voltage

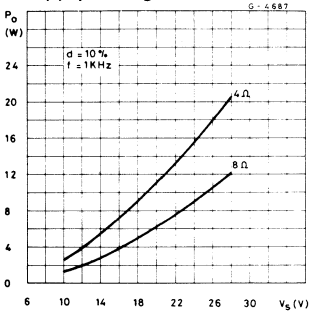



Fig. 5 - Distortion vs. output power

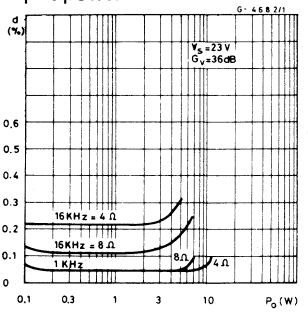



Fig. 6 - Distortion vs. frequency

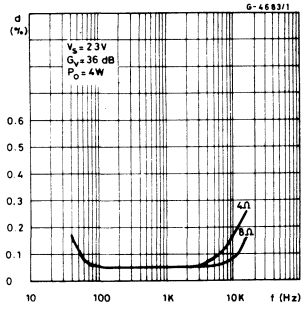



Fig. 7 - Quiescent current vs. supply voltage

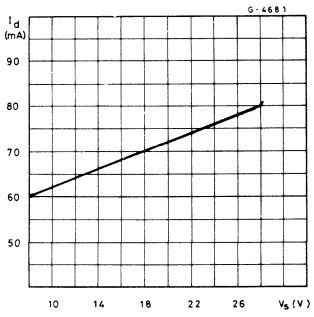



Fig. 8 - Supply voltage rejection vs. value of capacitor C3

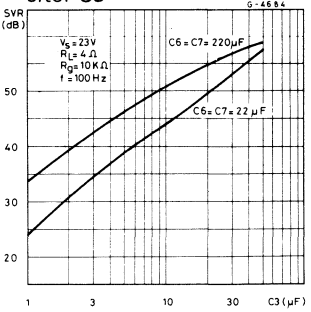



Fig. 9 - Supply voltage rejection vs. frequency

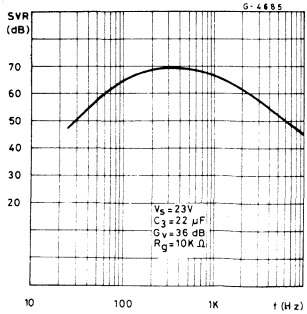



Fig. 10 - Total power dissipation an efficiency vs. output power

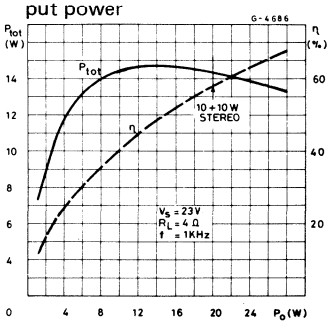
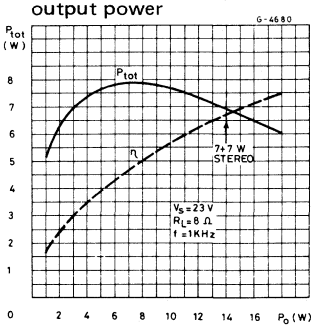



Fig. 11 - Total power dissipation and efficiency vs. output power



## APPLICATION INFORMATION

Fig. 12 - 10 + 10W stereo amplifier with tone balance and loudness control

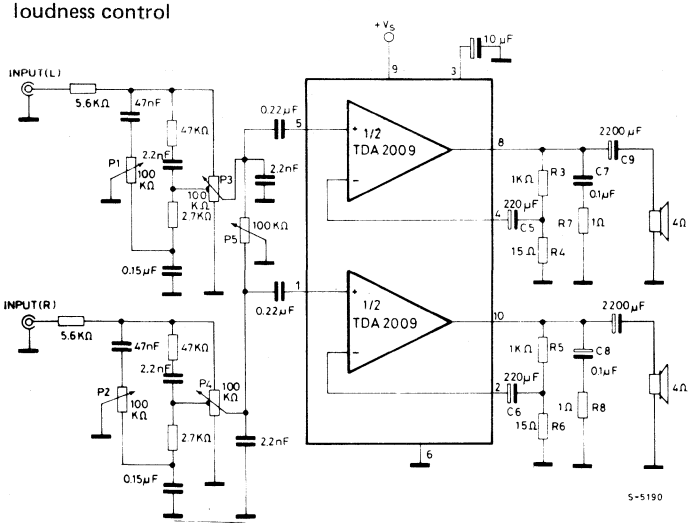



Fig. 13 - Tone control response (circuit of fig. 12)

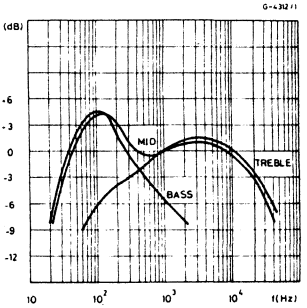
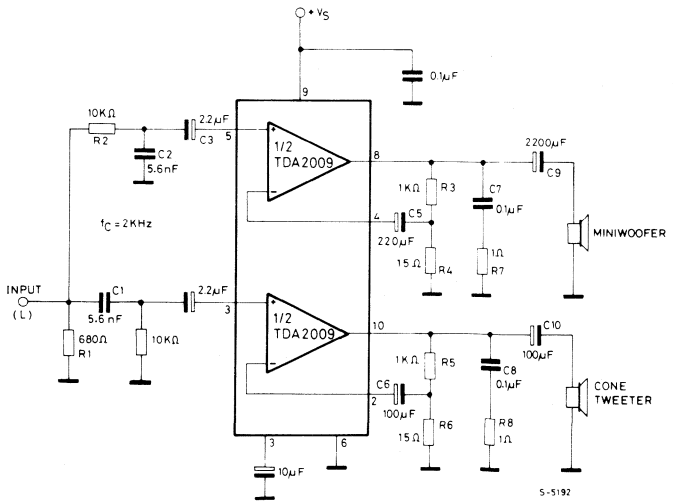
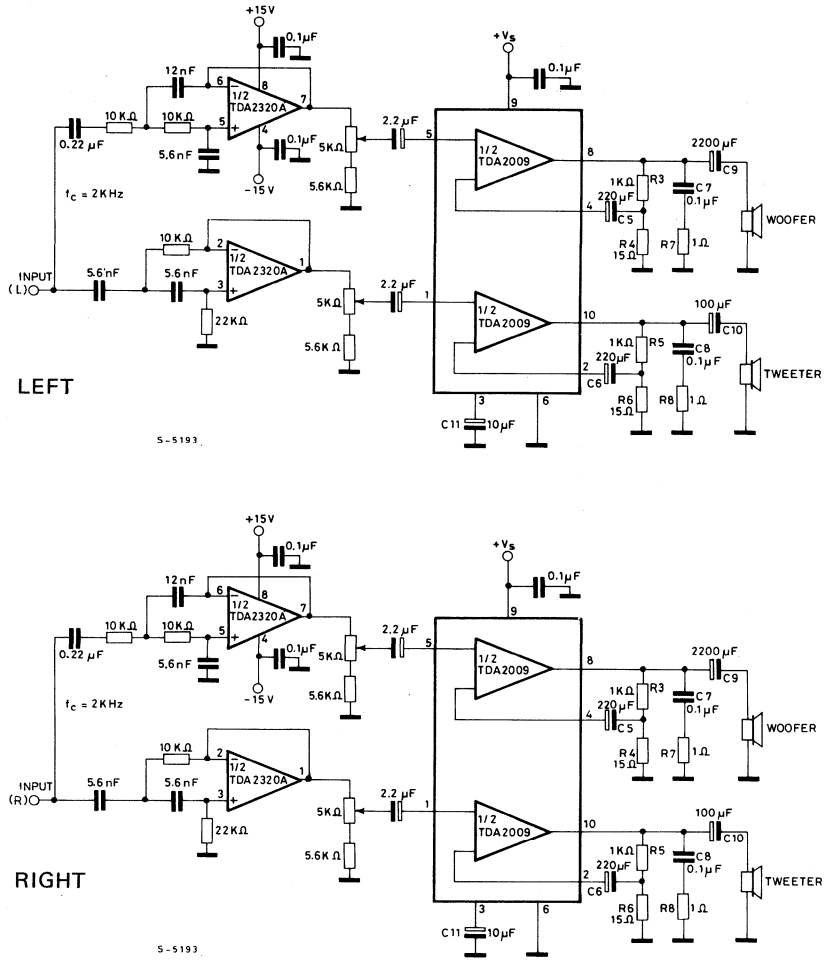



Fig. 14 - 20W Hi-Fi TV two way amplifier ($f_c$ = 2 KHz)



## APPLICATION INFORMATION (continued)

Fig. 15 - High quality 20 + 20W two way amplifier for stereo music center



## APPLICATION INFORMATION (continued)

Fig. 16 - 18W bridge amplifier (d = 0.5%, $G_v$ = 40 dB)

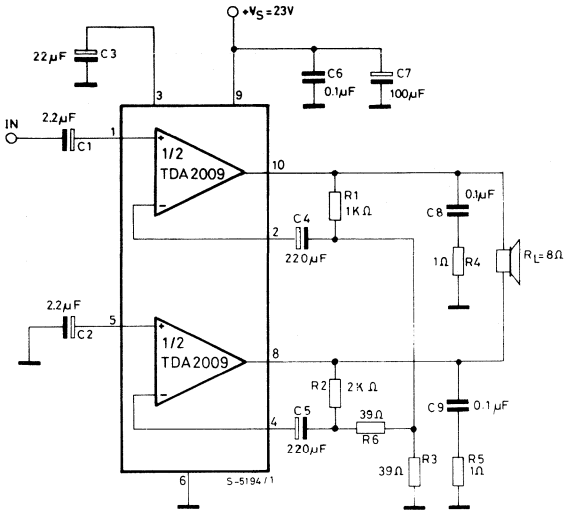
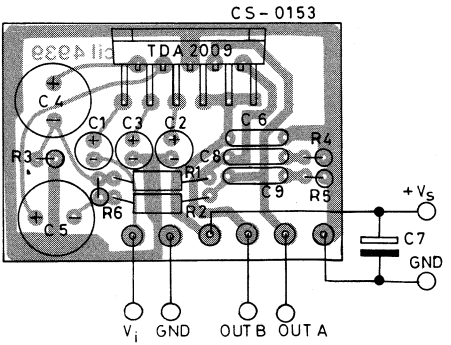



Fig. 17 - P.C. board and components layout of the circuit of fig. 16 (1 : 1 scale)



## APPLICATION SUGGESTION

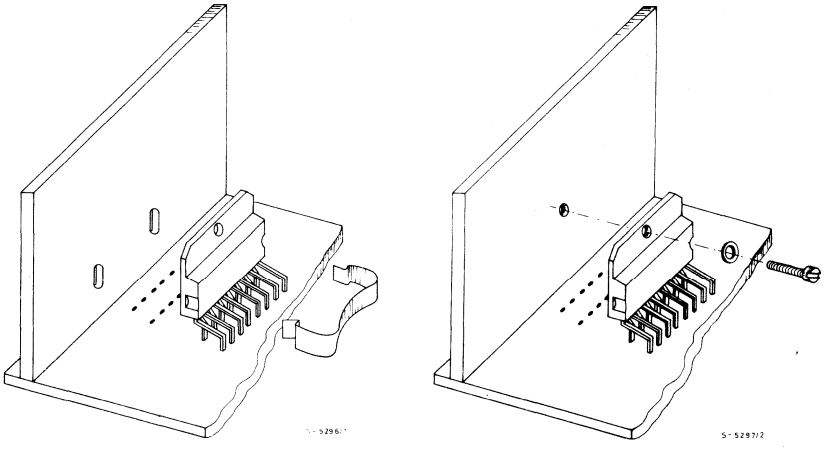
The recommended values of the components are those shown on application circuit of fig. 1 . Different values can be used; the following table can help the designer.

| Component | Recomm. value | Purpose | Larger than | Smaller than |
|---|---|---|---|---|
| R1 and R3 | 1.2 KΩ | Close loop gain setting | Increase of gain | Decrease of gain |
| R2 and R4 | 18 Ω | | Decrease of gain | Increase of gain |
| R5 and R6 | 1 Ω | Frequency stability | Danger of oscillation at high frequency with inductive load | |
| C1 and C2 | 2.2 μF | Input DC decoupling | High turn-on delay | High turn-on pop<br>Higher low frequency cutoff. Increase of noise |
| C3 | 22 μF | Ripple rejection | Better SVR.<br>Increase of the switch-on time | Degradation of SVR. |
| C6 and C7 | 220 μF | Feedback Input DC decoupling. | | |
| C8 and C9 | 0.1 μF | Frequency stability. | | Danger of oscillation. |
| C10 and C11 | 1000 μF to 2200 μF | Output DC decoupling. | | Higher low-frequency cut-off. |

## MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 18 - Mounting examples



# TDA2010

# LINEAR INTEGRATED CIRCUITS

**NOT FOR NEW DESIGN**

## 12W Hi-Fi AUDIO AMPLIFIER

The TDA 2010 is a monolithic integrated operational amplifier in a 14-lead quad in-line plastic package, inteded for use as a low frequency class B power amplifier. Typically it provides 12W output power (d = 1% ) at ± 14V/4Ω; at $V_s$ = ± 14V the guaranteed output power is 10W on a 4Ω load and 8W on a 8Ω load (DIN norm 45500). The TDA 2010 provides high output current (up to 3.5 A) and has very low harmonic and cross-over distortion. Further, the device incorporates an original (and patented) short circuit protection system, comprising an arrangement for automatically limiting the dissipated power so as to keep to working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included. The TDA 2010 is pin to pin equivalent to TDA 2020.

## ABSOLUTE MAXIMUM RATINGS

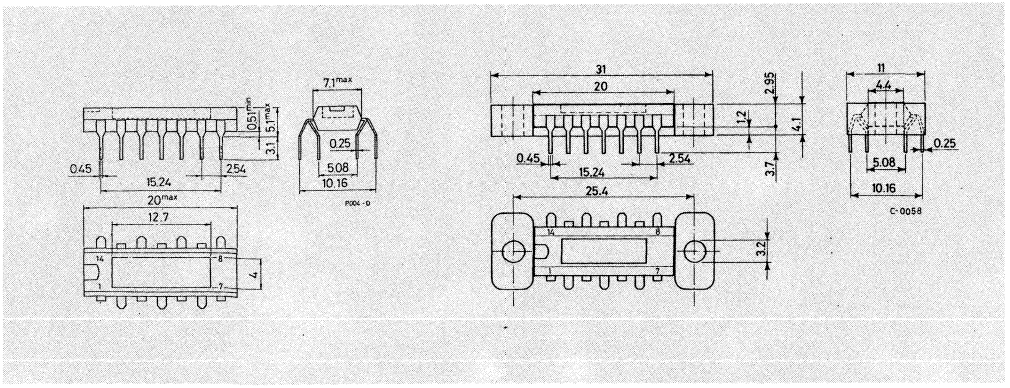
| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | ± 18 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential input voltage | ± 15 | V |
| $I_o$ | Output peak current (internally limited) | 3.5 | A |
| $P_{tot}$ | Power dissipation at $T_{case} \leqslant 95°C$ | 18 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMERS:**

| | |
|---|---|
| TDA 2010 B82 | dual in-line plastic package |
| TDA 2010 B92 | quad in-line plastic package |
| TDA 2010 BC2 | dual in-line plastic package with spacer |
| TDA 2010 BD2 | quad in-line plastic package with spacer |

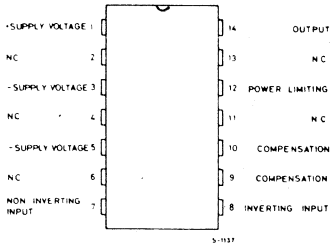
## MECHANICAL DATA

Dimensions in mm

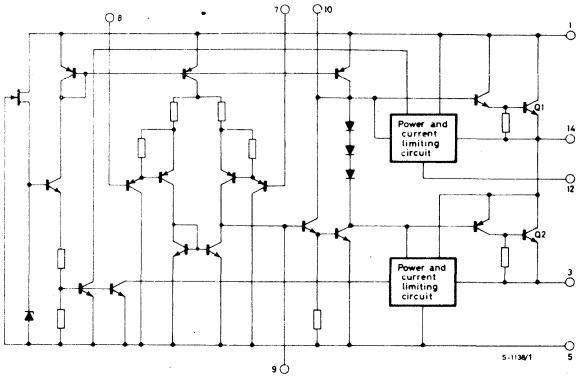


## CONNECTION AND SCHEMATIC DIAGRAMS

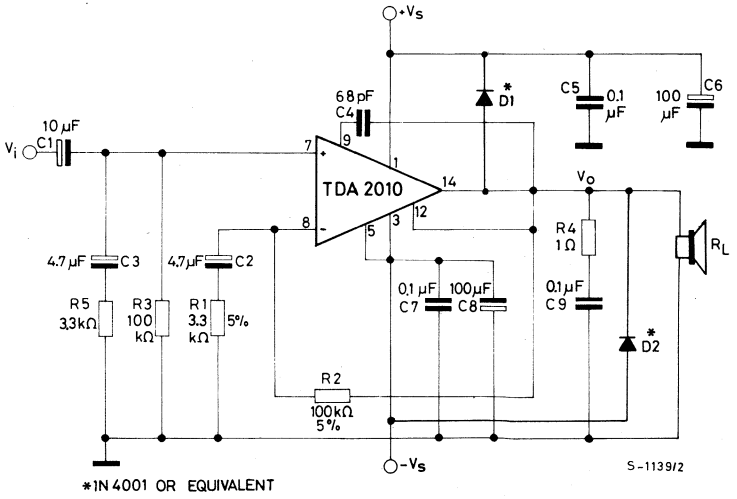
(top view)




The copper slug is electrically connected to pin 5 (substrate)




## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

## ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, $V_s = \pm 14V$, $T_{amb} = 25°C$ unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | ± 5 | | ± 18 | V |
| $I_d$ | Quiescent drain current | $V_s = \pm 18V$ | | 45 | | mA |
| $I_b$ | Input bias current | $V_s = \pm 17V$ | | 0.15 | | μA |
| $V_{os}$ | Input offset voltage | | | 5 | | mV |
| $I_{os}$ | Input offset current | | | 0.05 | | μA |
| $V_{os}$ | Output offset voltage | | | 10 | 100 | mV |
| $P_o$ | Output power | d = 1%<br>$T_{case} \leq 70°C$<br>f = 40 to 15 000 Hz<br>$R_L = 4\ \Omega$<br>$R_L = 8\ \Omega$ | <br><br><br>10<br>8 | <br><br><br>12<br>9 | | <br><br><br>W<br>W |
| | | d = 10%<br>$T_{case} \leq 70°C$ f = 1 kHz<br>$R_L = 4\ \Omega$<br>$R_L = 8\ \Omega$ | | <br><br>15<br>12 | | <br><br>W<br>W |
| $V_i$ | Input sensitivity | f = 1 kHz<br>$P_o = 10$ W $R_L = 4\ \Omega$<br>$P_o = 8$ W $R_L = 8\ \Omega$ | | <br>220<br>250 | | <br>mV<br>mV |
| B | Frequency response (-3dB) | $R_L = 4\ \Omega$ C4 = 68 pF | 10 to 160 000 | | | Hz |
| d | Distortion | $P_o = 100$ mW to 10 W<br>$R_L = 4\ \Omega$<br>$T_{case} \leq 70°C$<br>f = 1 kHz<br>f = 40 to 15 000 Hz | | <br><br><br>0.1<br>0.3 | <br><br><br><br>1 | <br><br><br>%<br>% |
| | | $P_o = 100$ mW to 8 W<br>$R_L = 8\ \Omega$<br>$T_{case} \leq 70°C$<br>f = 1 kHz<br>f = 40 to 15 000 Hz | | <br><br><br>0.1<br>0.2 | <br><br><br><br>1 | <br><br><br>%<br>% |
| $R_i$ | Input resistance (pin 7) | | | 5 | | MΩ |
| $G_v$ | Voltage gain (open loop) | $R_L = 4\ \Omega$ f = 1 kHz | | 100 | | dB |
| $G_v$ | Voltage gain (closed loop) | | 29.5 | 30 | 30.5 | dB |
| $e_N$ | Input noise voltage | $R_L = 4\ \Omega$ | | 4 | | μV |
| $i_N$ | Input noise current | B (-3 dB) = 22 Hz to 22 KHz | | 0.1 | | nA |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| SVR | Supply voltage rejection | $R_L = 4\ \Omega$<br>$f_{ripple} = 100$ Hz | | 50 | | dB |
| $I_d$ | Drain current | $P_o = 12$ W $R_L = 4\ \Omega$<br>$P_o = 9$ W $R_L = 8\ \Omega$ | | 0.8<br>0.5 | | A<br>A |
| $T_{sd}$ | Thermal shut-down junction temperature | | | 145 | | °C |
| $T_{sd}$ | (*) Thermal shut-down case temperature | $P_{tot} = 10.5$ W | | 120 | | °C |

(*) See fig. 14.

Fig. 1 - Output power vs. supply voltage

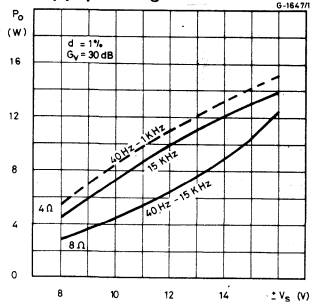



Fig. 2 - Output power vs. supply voltage

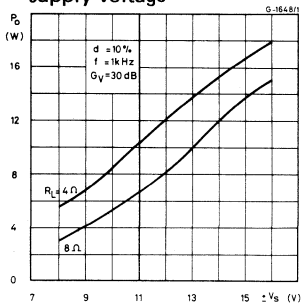



Fig. 3 - Distortion vs. output power

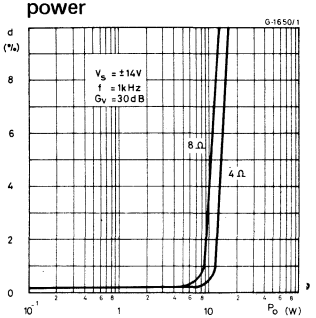



Fig. 4 - Distortion vs. output power ($R_L = 4\ \Omega$)

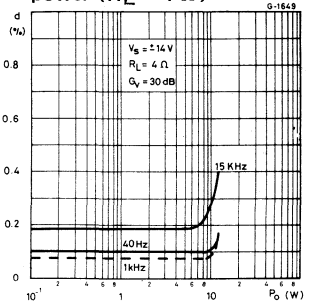



Fig. 5 - Distortion vs. output power ($R_L = 8\ \Omega$)

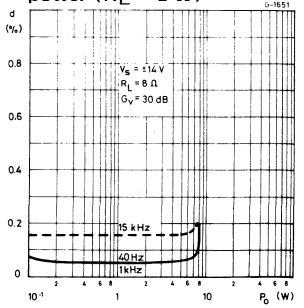



Fig. 6 - Distortion vs. frequency

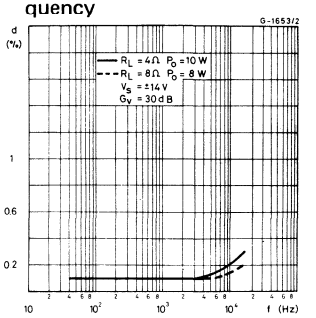


Fig. 7 - Output power vs. frequency

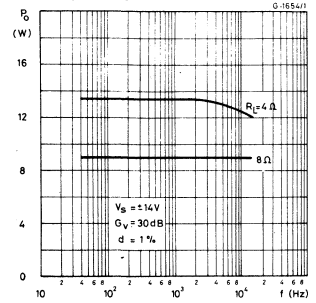



Fig. 8 - Sensitivity vs. output power ($R_L = 4\ \Omega$)

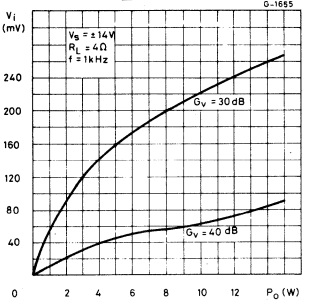



Fig. 9 - Sensitivity vs. output power ($R_L = 8\ \Omega$)

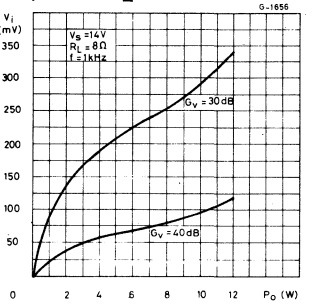



Fig. 10 - Open loop frequency response with different values of the rolloff capacitor C4

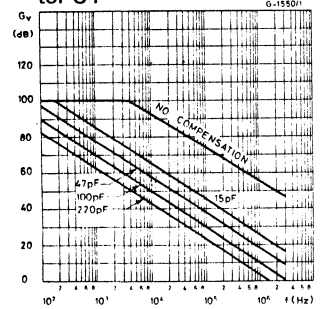



Fig. 11 - Value of C4 vs. voltage gain for different bandwidths

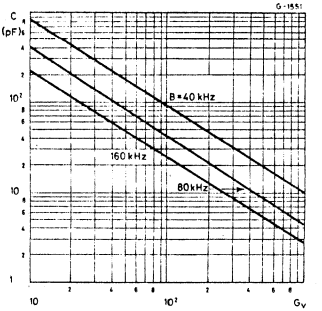



Fig. 12 - Quiescent current vs. supply voltage

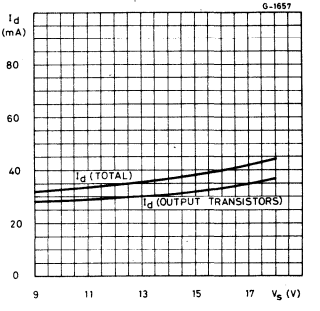



Fig. 13 - Supply voltage rejection vs. voltage gain

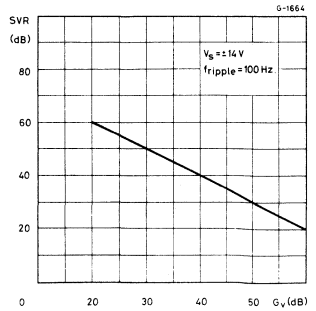



Fig. 14 - Power dissipation and efficiency vs. output power

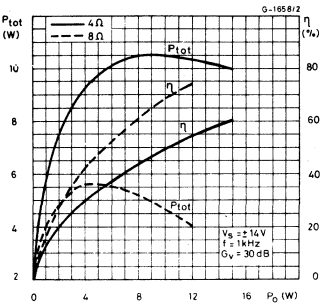
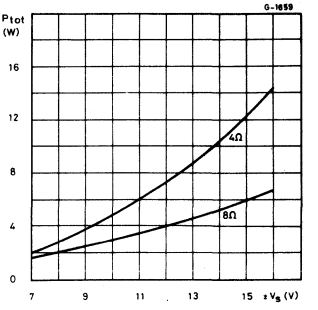



Fig. 15 - Maximum power dissipation vs. supply voltage (sine wave operation)



# LINEAR INTEGRATED CIRCUITS

**TDA2020**

**NOT FOR NEW DESIGN**

## 20W Hi-Fi AUDIO AMPLIFIER

The TDA 2020 is a monolithic integrated **operational amplifier** in a 14-lead quad in-line plastic package, intended for use as a low frequency class B power amplifier. Typically it provides 20W output power (d = 1% ) at ± 18V/4Ω; the guaranteed output power at ± 17V/4Ω is 15W (DIN norm 45500). The TDA 2020 provides high output current (up to 3.5 A) and has very low harmonic and cross-over distortion. Further, the device incorporates an original (and patented) short circuit protection system, comprising an arrangement for automatically limiting the dissipated power so as to keep to working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included.

## ABSOLUTE MAXIMUM RATINGS

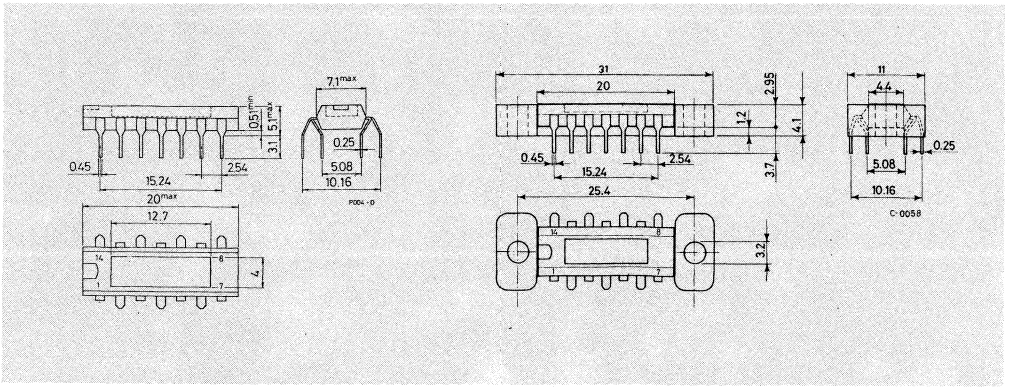
| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | ± 22 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential input voltage | ± 15 | V |
| $I_o$ | Output peak current (internally limited) | 3.5 | A |
| $P_{tot}$ | Power dissipation at $T_{case} \leqslant 75°C$ | 25 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBERS:**

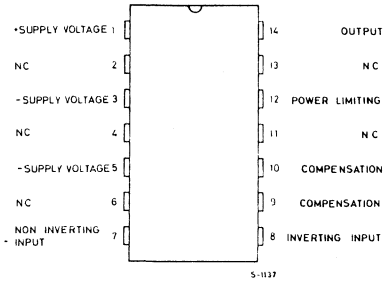
| | |
|---|---|
| TDA 2020 A82 | dual in-line plastic package |
| TDA 2020 A92 | quad in-line plastic package |
| TDA 2020 AC2 | dual in-line plastic package with spacer |
| TDA 2020 AD2 | quad in-line plastic package with spacer |

## MECHANICAL DATA

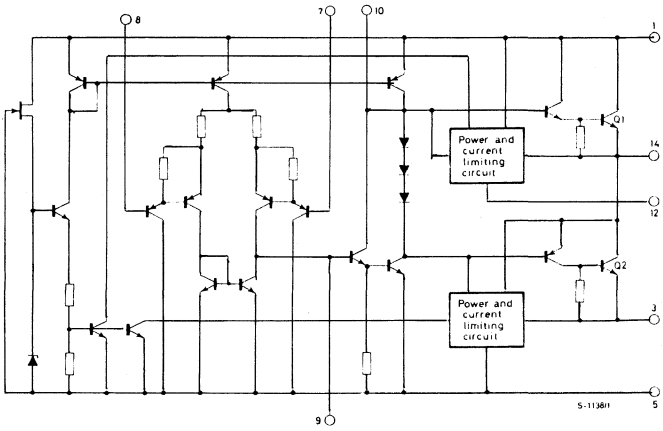
Dimensions in mm



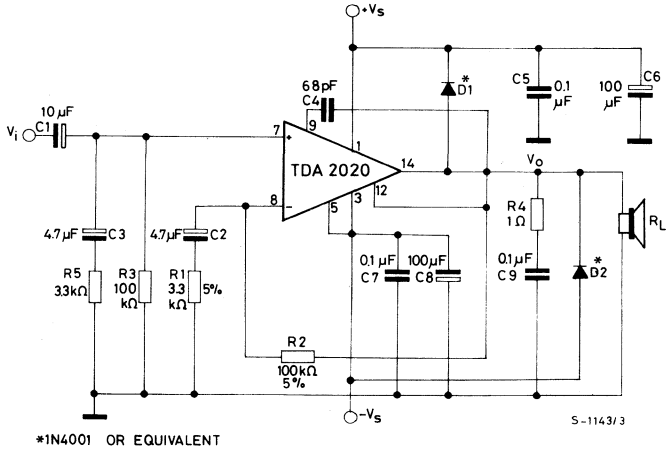
## CONNECTION AND SCHEMATIC DIAGRAMS
(top view)




The copper slug is electrically connected to pin 5 (substrate)




## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

## ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, $V_s = \pm 17V$, $T_{amb} = 25°C$ unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | ± 5 | | ± 22 | V |
| $I_d$ | Quiescent drain current | $V_s$ = ± 22 V | | 60 | | mA |
| $I_b$ | Input bias current | | | 0.15 | | μA |
| $V_{os}$ | Input offset voltage | | | 5 | | mV |
| $I_{os}$ | Input offset current | | | 0.05 | | μA |
| $V_{os}$ | Output offset voltage | | | 10 | 100 | mV |
| $P_o$ | Output power | d = 1% $G_v$ = 30 dB<br>$T_{case} \leq 70°C$<br>f = 40 to 15 000 Hz | | | | |
| | | $V_s$ = ± 17V $R_L$ = 4 Ω | 15 | 18.5 | | W |
| | | $V_s$ = ± 18V $R_L$ = 4 Ω | | 20 | | W |
| | | $V_s$ = ± 18V $R_L$ = 8 Ω | | 16.5 | | W |
| | | d = 10% $G_v$ = 30 dB<br>$T_{case} \leq 70°C$ f = 1 kHz | | | | |
| | | $V_s$ = ± 17V $R_L$ = 4 Ω | | 24 | | W |
| | | $V_s$ = ± 18V $R_L$ = 8 Ω | | 20 | | W |
| $V_i$ | Input sensitivity | $G_v$ = 30 dB f = 1 kHz<br>$P_o$ = 15 W | | | | |
| | | $V_s$ = ± 17V $R_L$ = 4 Ω | | 260 | | mV |
| | | $V_s$ = ± 18V $R_L$ = 8 Ω | | 380 | | mV |
| B | Frequency response (-3 dB) | $R_L$ = 4 Ω C4 = 68 pF | | 10 to 160 000 | | Hz |
| d | Distortion | $P_o$ = 150 mW to 15W<br>$R_L$ = 4 Ω $G_v$ = 30 dB<br>$T_{case} \leq 70°C$ | | | | |
| | | f = 1 kHz | | 0.2 | | % |
| | | f = 40 to 15 000 Hz | | 0.3 | 1 | % |
| | | $P_o$ = 150 mW to 15W<br>$V_s$ = ± 18V $R_L$ = 8 Ω<br>$G_v$ = 30 dB $T_{case} \leq 70°C$ | | | | |
| | | f = 1 kHz | | 0.1 | | % |
| | | f = 40 to 15 000 Hz | | 0.25 | | % |
| $R_i$ | Input resistance (pin 7) | | | 5 | | MΩ |
| $G_v$ | Voltage gain (open loop) | $R_L$ = 4 Ω f = 1 kHz | | 100 | | dB |
| $G_v$ | Voltage gain (closed loop) | | 29.5 | 30 | 30.5 | dB |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $e_N$ | Input noise voltage | $R_L$ = 4 Ω | | 4 | | μV |
| $i_N$ | Input noise current | B(-3 dB) = 10 to 20,000 Hz | | 0.1 | | nA |
| SVR | Supply voltage rejection | $R_L$ = 4 Ω $G_v$ = 30 dB<br>$f_{ripple}$ = 100 Hz | | 50 | | dB |
| $I_d$ | Drain current | $P_o$ = 18.5W $R_L$ = 4 Ω | | 1 | | A |
| | | $P_o$ = 16.5W $V_s$ = ± 18V<br>$R_L$ = 8 Ω | | 0.7 | | A |
| $T_{sd}$ | Thermal shut-down junction temperature | | | 140 | | °C |
| $T_{sd}$ | Thermal shut-down case temperature | $P_{tot}$ = 15.5W | | 105 | | °C |

Fig. 1 - Output power vs. supply voltage

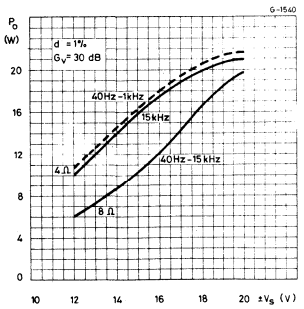



Fig. 2 - Output power vs. supply voltage

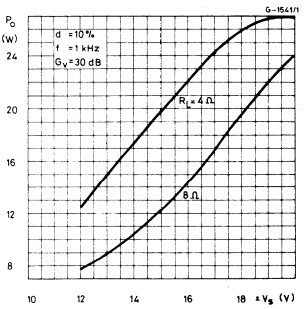



Fig. 3 - Distortion vs. output power

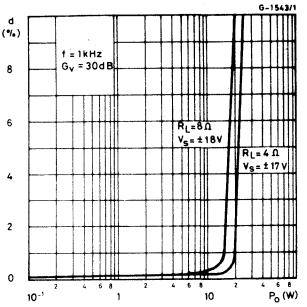


Fig. 4 - Distortion vs. output power ($R_L = 4\ \Omega$)

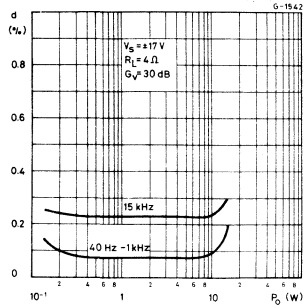



Fig. 5 - Distortion vs. output power ($R_L = 8\ \Omega$)

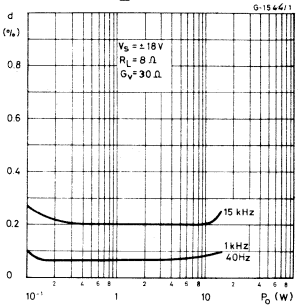



Fig. 6 - Distortion vs. frequency

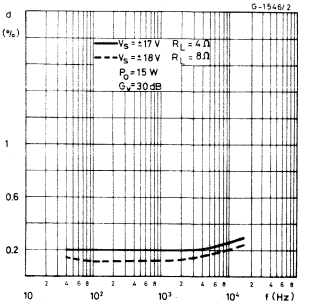



Fig. 7 - Output power vs. frequency

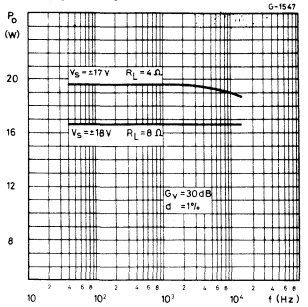



Fig. 8 - Sensitivity vs. output power ($R_L = 4\ \Omega$)

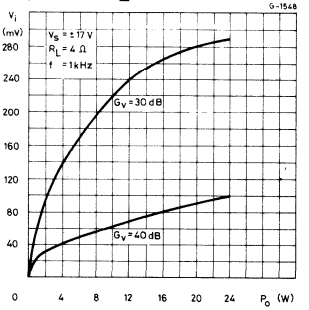



Fig. 9 - Sensitivity vs. output power ($R_L = 8\ \Omega$)

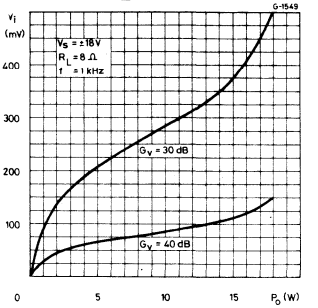



Fig. 10 - Open loop frequency response with different values of the rolloff capacitor C4

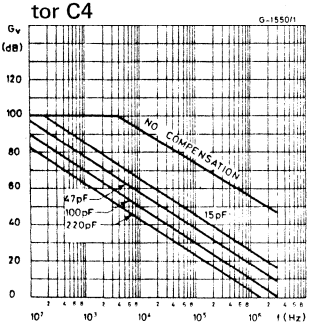



Fig. 11 - Value of C4 vs. voltage gain for different bandwidths

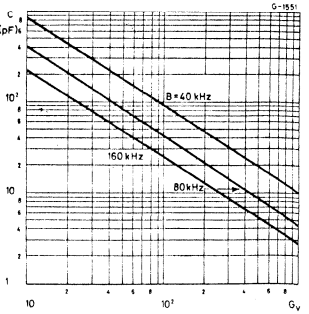



Fig. 12 - Quiescent current vs. supply voltage

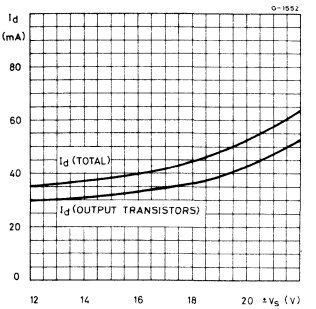


Fig. 13 - Supply voltage rejection vs. voltage gain

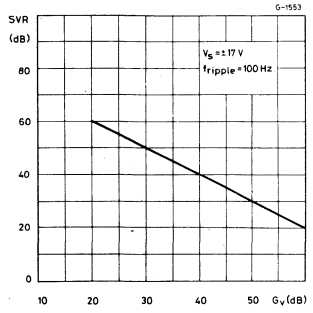



Fig. 14 - Power dissipation and efficiency vs. output power

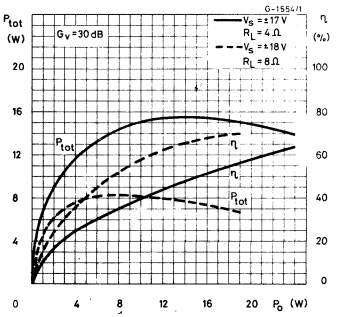
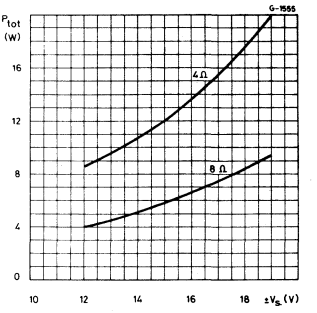



Fig. 15 - Maximum power dissipation vs. supply voltage (sine wave operation)




## APPLICATION INFORMATION

Fig. 16 - Application circuit with split power supply

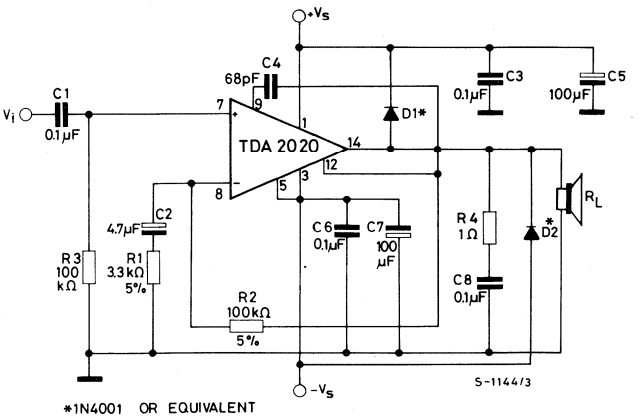


Fig. 17 - P.C. Board and component layout for the circuit of fig. 16 (1:1 scale)

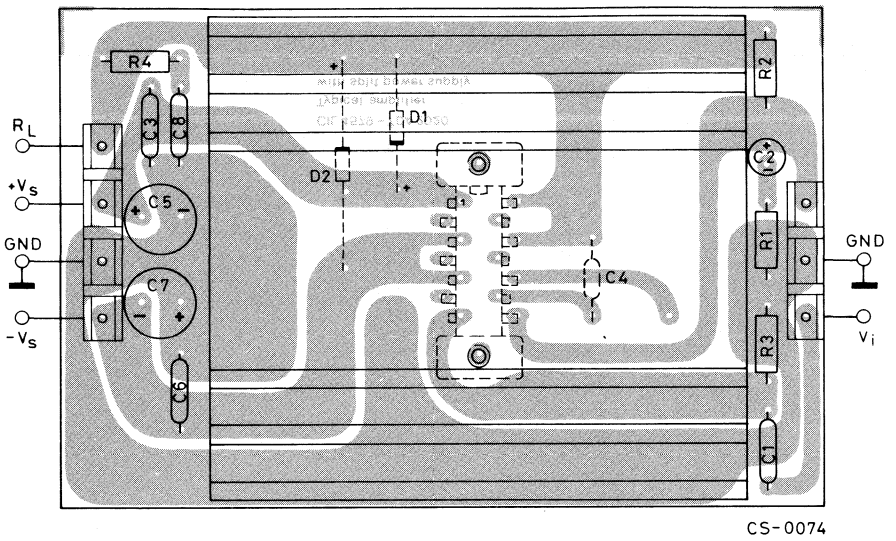
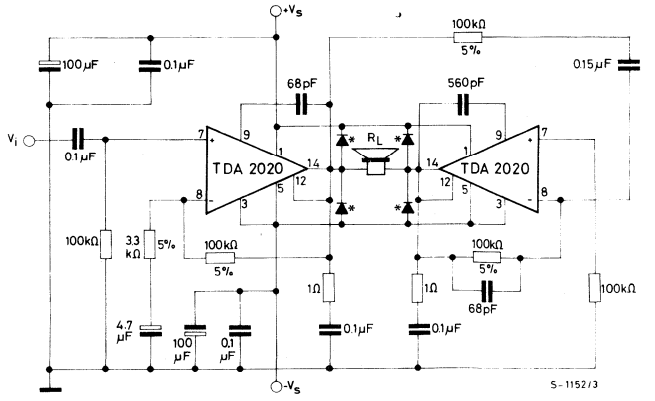



Fig. 18 - 30W bridge amplifier configuration with split power supply ($R_L = 8\ \Omega$ d $\leqslant 1\%$ ; $V_s = \pm 17V$)



# TDA2020D

# LINEAR INTEGRATED CIRCUITS

**NOT FOR NEW DESIGN**

## 40W AUDIO DRIVER

- HIGH SUPPLY VOLTAGE: ± 25V
- HIGH SUPPLY REJECTION: 80 dB
- PROGRAMMABLE SOA PROTECTION
- LOW DISTORTION (0.05% TYP.)
- LOW INPUT NOISE VOLTAGE (4 μV TYP.)

The TDA 2020D is a monolithic integrated **operational amplifier** in a 14 lead quad in-line plastic-package, intended for driving external power transistors in Hi-Fi amplifier (30 to 100W). This device incorporates an original (and patented) short circuit protection system, comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the external transistors within their safe operating area. A thermal shut-down system is also included. This thermal shut-down can also protect the external power transistors.

## ABSOLUTE MAXIMUM RATINGS

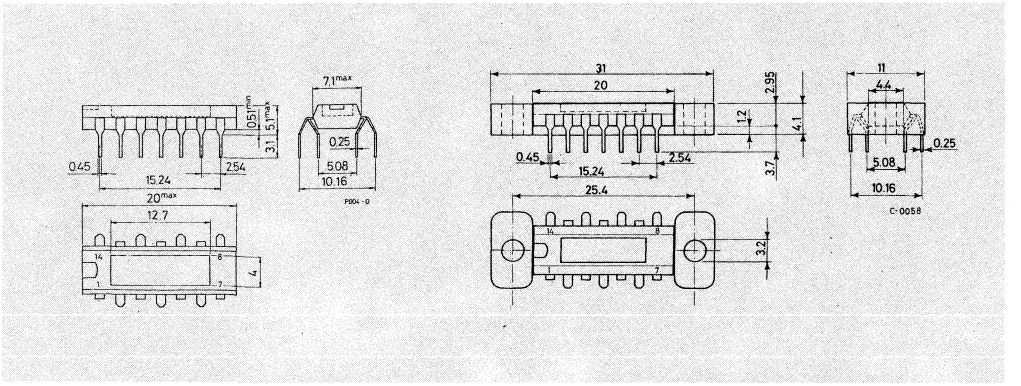
| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | ± 25 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential input voltage | ± 15 | V |
| $I_o$ | Output peak current | 1 | A |
| $P_{tot}$ | Power dissipation at $T_{case} \leqslant 75°C$ | 25 | W |
| $T_{stg}, T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBERS:**

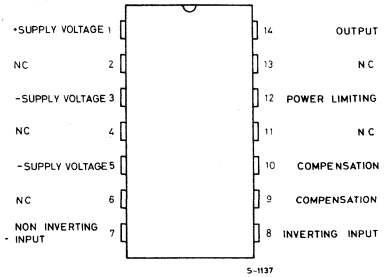
| | | |
|---|---|---|
| TDA 2020D | A82 | dual in-line plastic package |
| TDA 2020D | A92 | quad in-line plastic package |
| TDA 2020D | AC2 | dual in-line plastic package with spacer |
| TDA 2020D | AD2 | quad in-line plastic package with spacer |

## MECHANICAL DATA

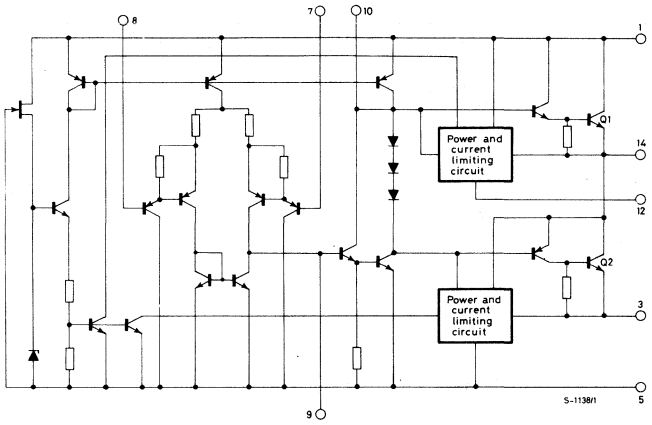
Dimensions in mm



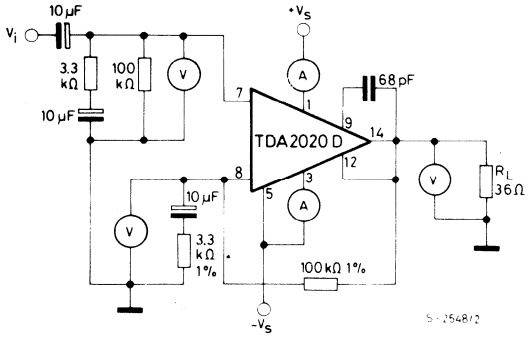
## CONNECTION AND SCHEMATIC DIAGRAMS
(top view)




The copper slug is electrically connected to pin 5 (substrate)




## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

**ELECTRICAL CHARACTERISTICS** (Refer to the test circuit, $V_s$= ±20V, $T_{amb}$= 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | ± 5 | | ± 25 | V |
| $I_d$ | Quiescent drain current | $V_s$ = ±25V | | 40 | 80 | mA |
| $I_b$ | Input bias current | | | 0.15 | | μA |
| $V_{os}$ | Input offset voltage | | | 5 | | mV |
| $I_{os}$ | Input offset current | | | 0.05 | | μA |
| $V_{os}$ | Output offset voltage | | | 10 | 100 | mV |
| $V_{CE(sat)}$ | Output saturation voltage | $I_o$ = 0.5A | | ± 1.7 | ± 2 | V |
| B | Frequency response (-3 dB) | $I_o$ = 0.5A | | 10 to 160 000 | | Hz |
| d | Distortion | $G_v$= 30 dB $I_o$ = 0.5A<br>f = 1 kHz<br>f = 40 to 15 000 Hz | | <br>0.05<br>0.2 | <br><br>0.3 | <br>%<br>% |
| | Intermodulation | DIN 45500 | | 0.2 | | % |
| $R_i$ | Input resistance (pin 7) | | | 5 | | MΩ |
| $G_v$ | Voltage gain (open loop) | f = 1 kHz | | 100 | | dB |
| $G_v$ | Voltage gain (closed loop) | | 29.5 | 30 | 30.5 | dB |
| $e_N$ | Input noise voltage | B (-3 dB) = 10 to 20 000 Hz | | 4 | | μV |
| $i_N$ | Input noise current | | | 0.1 | | nA |
| SVR | Supply voltage rejection | $f_{ripple}$= 100 Hz $G_v$= 30 dB | 35 | 50 | | dB |
| $I_d$ | Drain current | $P_o$ = 4.5W $R_L$= 36Ω<br>$P_o$ = 2W $R_L$= 36Ω | | 160<br>100 | | mA<br>mA |
| $T_{sd}$ | Thermal shut-down junction temperature | | | 145 | | °C |
| $T_{sd}$ | Thermal shut-down case temperature | $P_{tot}$= 5W | | 135 | | °C |

Fig. 1 - Quiescent current vs. supply voltage

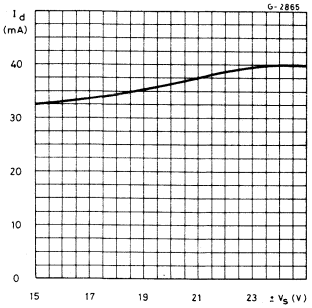



Fig. 2 - Output current vs. $V_{CE(sat)}$

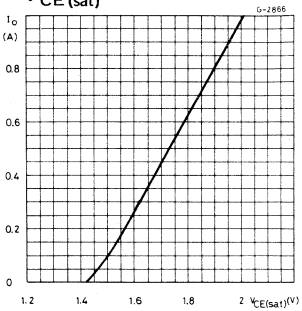



Fig. 3 - Power dissipation vs. supply voltage

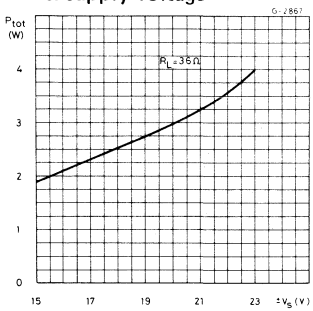



Fig. 4 - Open loop frequency response with different values of the rolloff capacitor

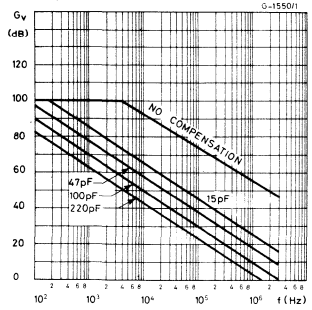



Fig. 5 - Value of rolloff capacitor vs. voltage gain for different bandwidths

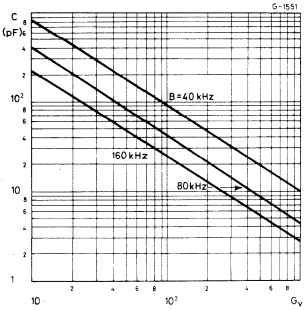



Fig. 6 - Supply voltage rejection vs. voltage gain

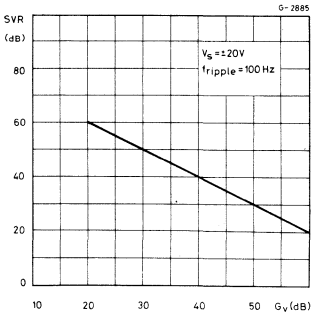



Fig. 7 - Transient response

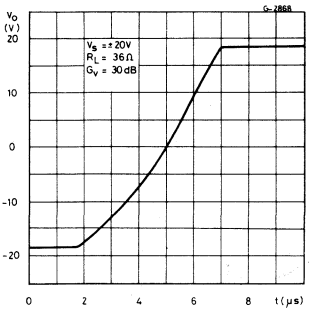
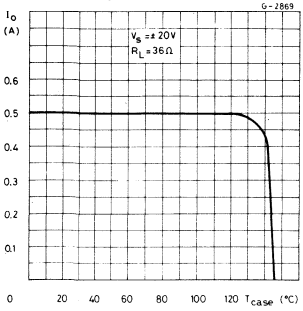
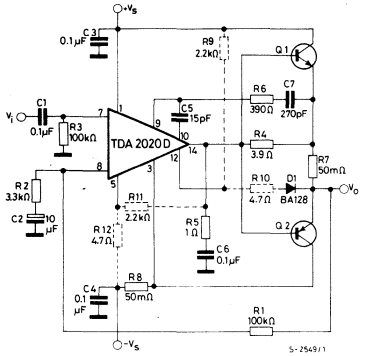



Fig. 8 - Output current vs. case temperature



## APPLICATION INFORMATION

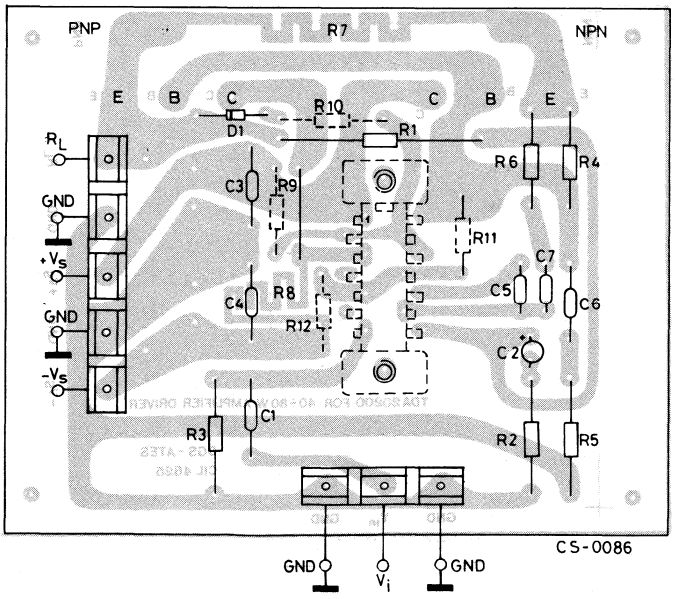
Fig. 9 - Application circuit for $P_o$= 30 to 50W




**Note:**
Resistors R9, R10, R11 and R12 are optional. Their purpose is to change the allowable operating area of the output transistors (see fig. 23).
The designer can choose different values according to working conditions ($V_s$, $R_L$) and to the SOA of the external transistors. When these resistors are not used the application circuit is modified as follows:

a) R7, R8 are changed to 25 mΩ.
b) R10, R12 are substituted by a short circuit.

Fig. 10 - P.C. board and component layout for the circuit of fig. 9 (1:1 scale)




| $P_o$ $R_L$= 4Ω | 30W | 40W |
|---|---|---|
| ± $V_s$ | 18V | 20V |
| R9/R11 | – | 2.2 kΩ |
| R10/R12 | 4.7Ω | 4.7Ω |
| Q1 | BD707 or BDW21A | BD907 or BDW21A |
| Q2 | BD708 or BDW22A | BD908 or BDW22A |

**Note:**
If resistors R9, R10, R11 and R12 are not used, R7 and R8 must be 25 mΩ. The following table shows what length of wire (copper and constantan) is required to obtain a resistor of 25 mΩ for different values of ϕ.

| ϕ (mm) | 1 | 0.8 | 0.7 | 0.5 | 0.4 | 0.3 |
|---|---|---|---|---|---|---|
| l (mm) copper | – | – | 570 | 290 | 180 | 100 |
| l (mm) constantan | 40 | 25 | 20 | 10 | 6.5 | – |

## Application suggestions

The recommended values of the components are those shown in application circuit of fig. 9, although different values can be used. The following table may help the amplifier designers.

| Component | Recomm. value | Purpose | Larger than recommended value | Smaller than recommended value |
|---|---|---|---|---|
| C1 | 0.1 μF | Elimination of DC current on volume control | Reduced lower cutoff frequency | Increased lower cutoff frequency |
| C2 | 10 μF | To obtain DC gain equal to 1 | Reduced lower cutoff frequency | Increased lower cutoff frequency |
| C3 and C4 | 0.1 μF | Frequency stabilization | | Danger of oscillations |
| C5 | 15 pF | Upper frequency cutoff | Reduced upper cutoff frequency | Increased upper cutoff frequency |
| C6 | 0.1 μF | Frequency stabilization | | Danger of oscillation |
| C7 | 270 pF | Compensation | | Danger of oscillations |
| R1 | 100 kΩ | Closed loop gain determination | Larger closed loop gain | Smaller closed loop gain |
| R2 | 3.3 kΩ | Closed loop gain determination | Smaller closed loop gain | Larger closed loop gain |
| R3 | R1 | Input bias | Output DC offset variation | Output DC offset variation |
| R4 | 3.9 Ω | External power transistor driving | Danger of distortion | Increased load for the driver |
| R5 | 1 Ω | Frequency stabilization | Danger of oscillations | Danger of oscillations |
| R6 | 390 Ω | Compensation | | |
| R7 and R8 | 50 mΩ | Current protection sensing | Reduced maximum output current value | Increased maximum output current value |
| R9, R10, R11, R12 | see Fig. 23 | | | |
| Q1 - Q2 | BD 707 – BD 708 or BD 907 – BD 908 or BDW 21A – BDW 22A | | | |
| D1 | BA 128 | Short circuit prot. | | |

Fig. 11 - Output power vs. supply voltage

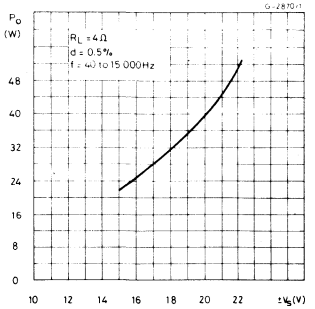



Fig. 12 - Output power vs. supply voltage

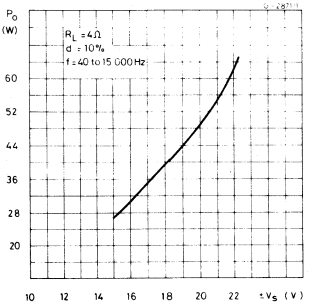



Fig. 13 - Distortion vs. output power

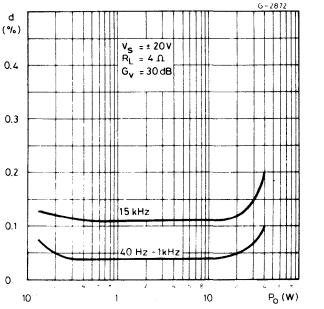



Fig. 14 - Distortion vs. output power

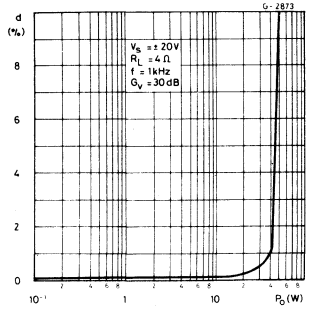



Fig. 15 - Distortion vs. frequency

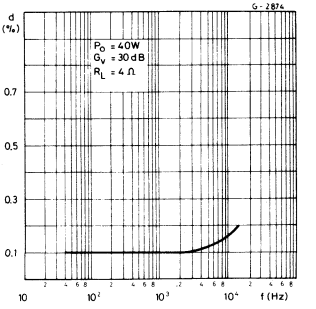



Fig. 16 - Input sensitivity vs. output power

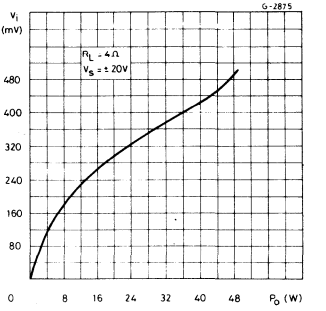



Fig. 17 - Maximum power dissipation vs. supply voltage (sine wave operation)

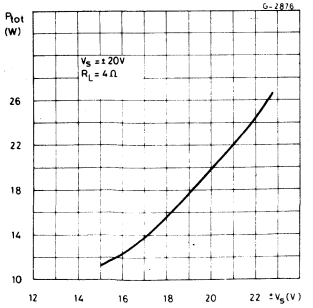
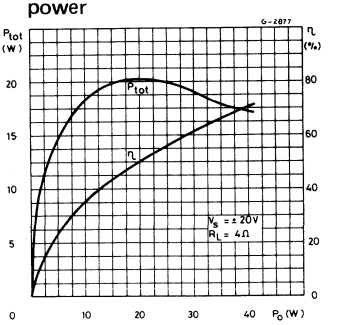



Fig. 18 - Power dissipation and efficiency vs. output power



**TDA2030**

## 14W Hi-Fi AUDIO AMPLIFIER

The TDA 2030 is a monolithic integrated circuit in Pentawatt® package. intended for use as a low frequency class AB amplifier. Typically it provides 14W output power (d = 0.5%) at ± 14V/4Ω; at ± 14V the guaranteed output power is 12W on a 4Ω load and 8W on a 8Ω (DIN 45500). The TDA 2030 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system si also included.

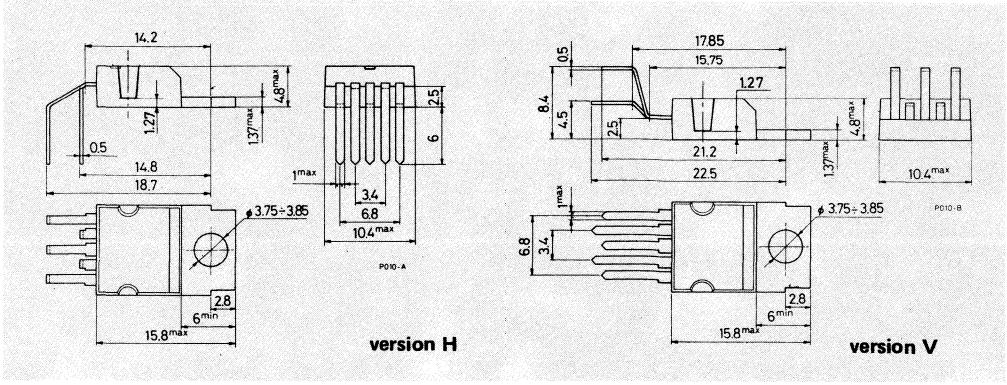
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | ± 18 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential input voltage | ± 15 | V |
| $I_o$ | Output peak current (internally limited) | 3.5 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$ = 90°C | 20 | W |
| $T_{stg}, T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBERS:** TDA 2030 H; TDA 2030 V

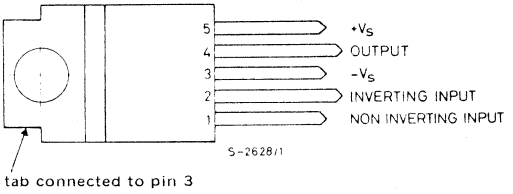
## MECHANICAL DATA

Dimensions in mm

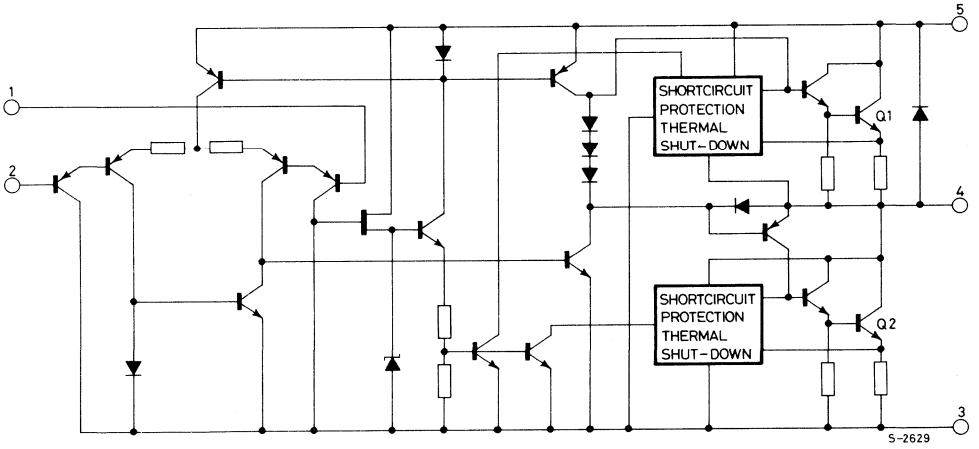


# TDA2030

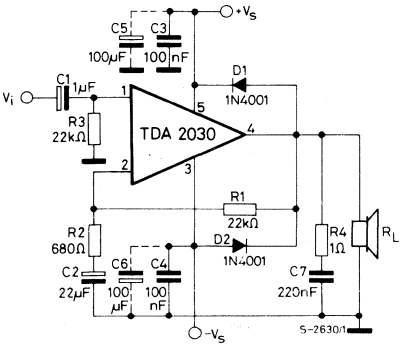
## CONNECTION DIAGRAM
(top view)




## SCHEMATIC DIAGRAM




## TEST CIRCUIT



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = \pm 14V$, $T_{amb} = 25°C$ unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | ± 6 | | ± 18 | V |
| $I_d$ | Quiescent drain current | $V_s = \pm 18V$ | | 40 | 60 | mA |
| $I_b$ | Input bias current | | | 0.2 | 2 | μA |
| $V_{os}$ | Input offset voltage | | | ± 2 | ± 20 | mV |
| $I_{os}$ | Input offset current | | | ± 20 | ± 200 | nA |
| $P_o$ | Output power | d = 0.5% $G_v$ = 30 dB<br>f = 40 to 15 000 Hz<br>$R_L$ = 4Ω<br>$R_L$ = 8Ω | <br><br>12<br>8 | <br><br>14<br>9 | | <br><br>W<br>W |
| | | d = 10% $G_v$ = 30 dB<br>f = 1 kHz<br>$R_L$ = 4Ω<br>$R_L$ = 8Ω | | <br><br>18<br>11 | | <br><br>W<br>W |
| d | Distortion | $P_o$ = 0.1 to 12W<br>$R_L$ = 4Ω $G_v$ = 30 dB<br>f = 40 to 15 000 Hz | | <br><br>0.2 | <br><br>0.5 | <br><br>% |
| | | $P_o$ = 0.1 to 8W<br>$R_L$ = 8Ω $G_v$ = 30 dB<br>f = 40 to 15 000 Hz | | <br><br>0.1 | <br><br>0.5 | <br><br>% |
| B | Power Bandwidth (-3 dB) | $G_v$ = 30 dB<br>$P_o$ = 12W $R_L$ = 4Ω | 10 to 140 000 | | | Hz |
| $R_i$ | Input resistance (pin 1) | | 0.5 | 5 | | MΩ |
| $G_v$ | Voltage gain (open loop) | | | 90 | | dB |
| $G_v$ | Voltage gain (closed loop) | f = 1 kHz | 29.5 | 30 | 30.5 | dB |
| $e_N$ | Input noise voltage | B = 22 Hz to 22 KHz | | 3 | 10 | μV |
| $i_N$ | Input noise current | | | 80 | 200 | pA |
| SVR | Supply voltage rejection | $R_L$ = 4Ω $G_v$ = 30 dB<br>$R_g$ = 22 kΩ<br>$V_{ripple}$ = 0.5 $V_{eff}$<br>$f_{ripple}$ = 100 Hz | 40 | 50 | | dB |
| $I_d$ | Drain current | $P_o$ = 14W $R_L$ = 4Ω<br>$P_o$ = 9W $R_L$ = 8Ω | | 900<br>500 | | mA<br>mA |
| $T_j$ | Thermal shut-down junction temperature | | | 145 | | °C |

Fig. 1 - Output power vs. supply voltage

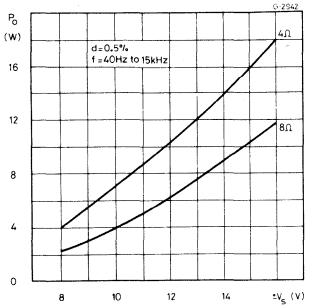



Fig. 2 - Output power vs. supply voltage

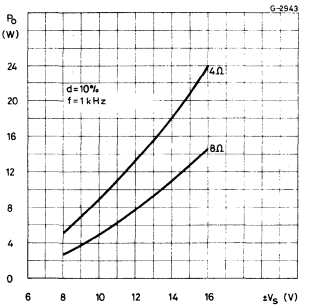



Fig. 3 - Distortion vs. output power

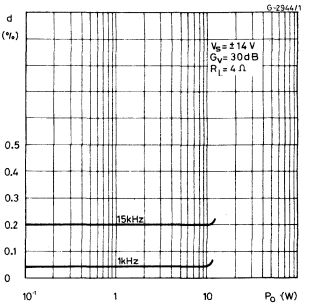



Fig. 4 - Distortion vs. output power

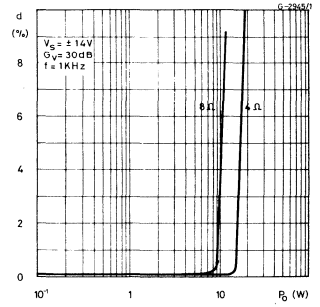



Fig. 5 - Distortion vs. output power

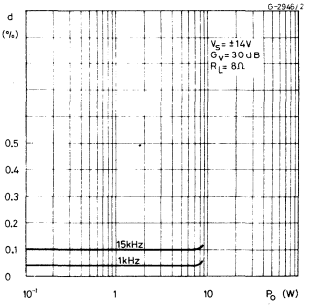



Fig. 6 - Distortion vs. frequency

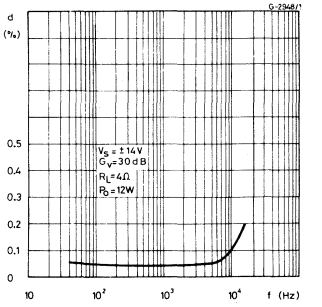



Fig. 7 - Distortion vs. frequency

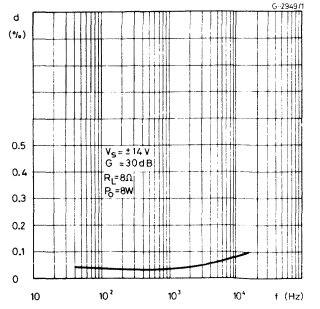



Fig. 8 - Frequency response with different values of the rolloff capacitor C8 (see fig. 13)

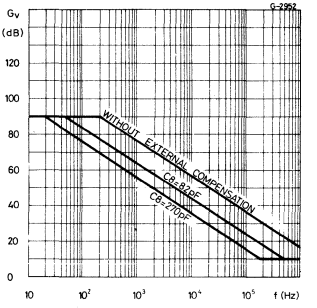



Fig. 9 - Quiescent current vs. supply voltage

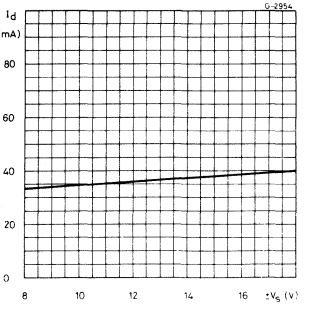


Fig. 10 - Supply voltage rejection vs. voltage gain

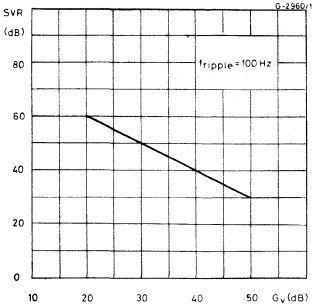



Fig. 11 - Power dissipation and efficiency vs. output power

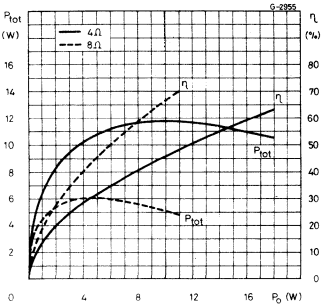
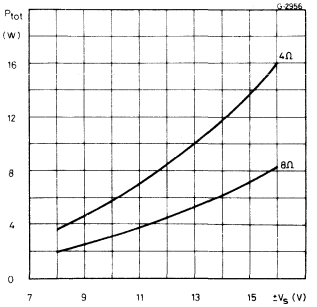



Fig. 12 - Maximum power dissipation vs. supply voltage (sine wave operation)




## APPLICATION INFORMATION

Fig. 13 - Typical amplifier with split power supply

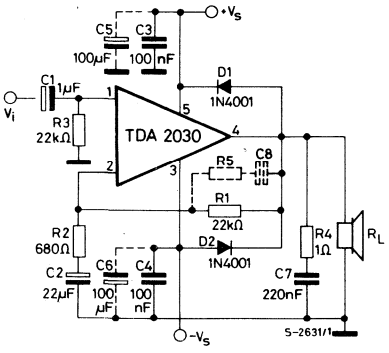
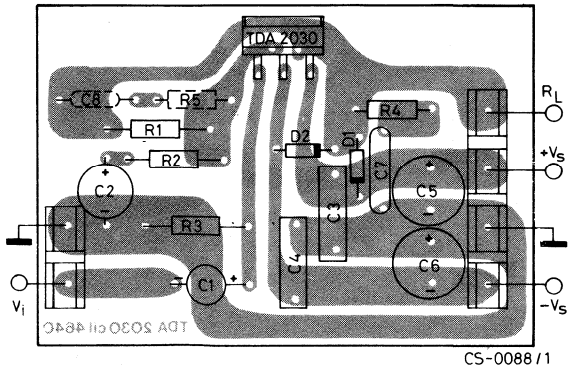



Fig. 14 - P.C. board and component layout for the circuit of fig. 13 (1:1 scale)




CS-0088/1

## APPLICATION INFORMATION (continued)

Fig. 15 - Typical amplifier with single power supply

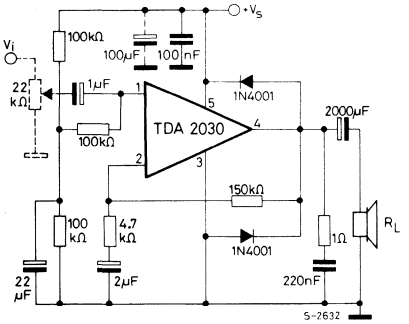



Fig. 16 - P.C. board and component layout for the circuit of fig. 15 (1:1 scale)

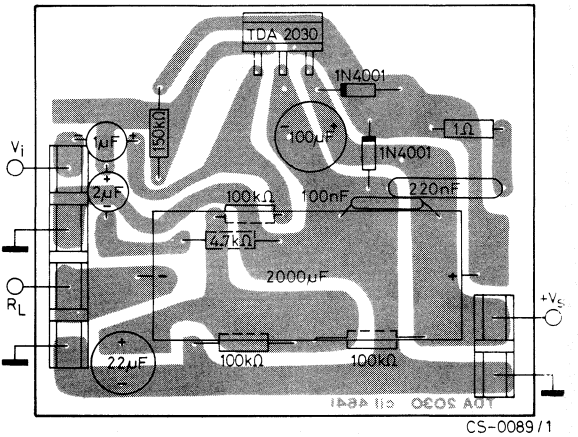
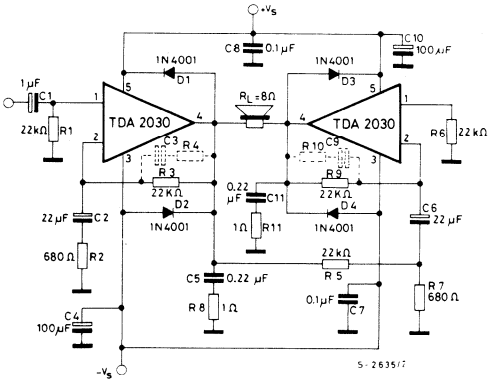



Fig. 17 - Bridge amplifier configuration with split power supply ($P_o$= 28W, $V_s$= ±14V)



## APPLICATION INFORMATION (continued)

Fig. 18 - P.C. board and component layout for the circuit in fig. 17 (1 : 1 scale)

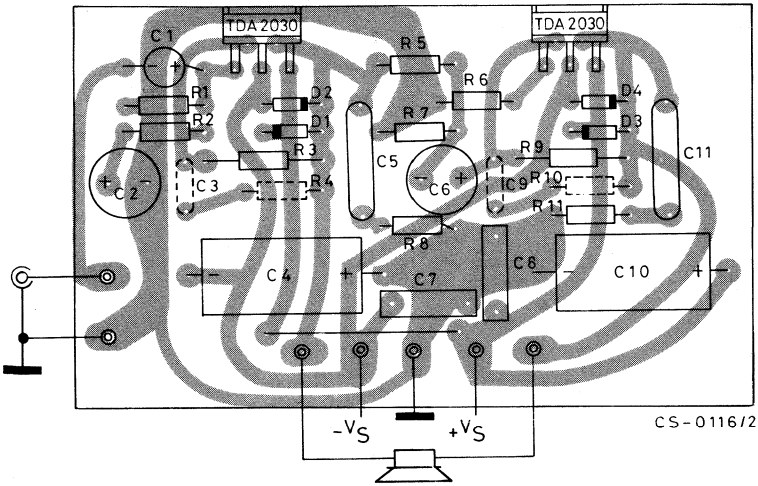
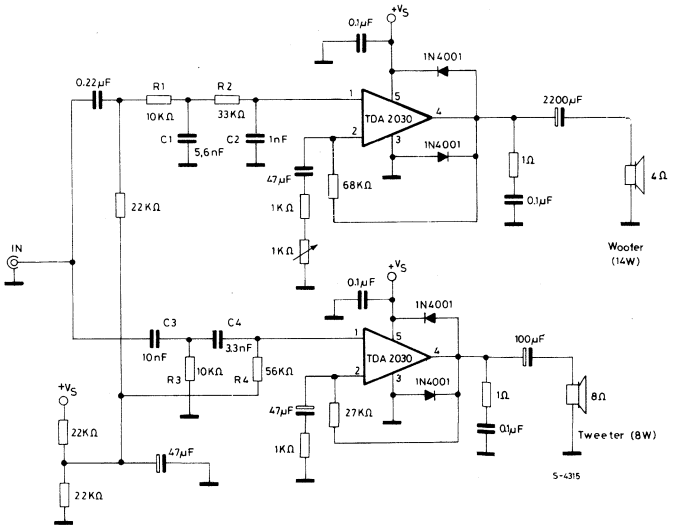



Fig. 19 - Two-way 22W Hi-Fi active-box



## PRACTICAL CONSIDERATIONS

### Printed circuit board

The layout shown in fig. 16 should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

### Assembly suggestion

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

### Application suggestions

The recommended values of the components are those shown on application circuit of fig. 13. Different values can be used. The following table can help the designer.

| Component | Recomm. value | Purpose | Larger than recommended value | Smaller than recommended value |
|---|---|---|---|---|
| R1 | 22 kΩ | Closed loop gain setting | Increase of gain | Decrease of gain |
| R2 | 680 Ω | Closed loop gain setting | Decrease of gain | Increase of gain |
| R3 | 22 kΩ | Non inverting input biasing | Increase of input impedance | Decrease of input impedance |
| R4 | 1 Ω | Frequency stability | Danger of oscillat. at high frequencies with induct. loads | |
| R5 | $\cong$ 3 R2 | Upper frequency cutoff | Poor high frequencies attenuation | Danger of oscillation |
| C1 | 1 μF | Input DC decoupling | | Increase of low frequencies cutoff |
| C2 | 22 μ F | Inverting DC decoupling | | Increase of low frequencies cutoff |
| C3,C4 | 0.1 μF | Supply voltage bypass | | Danger of oscillation |
| C5,C6 | 100 μF | Supply voltage bypass | | Danger of oscillation |
| C7 | 0.22 μF | Frequency stability | | Danger of oscillat. |
| C8 | $\cong \frac{1}{2\pi B R1}$ | Upper frequency cutoff | Smaller bandwidth | Larger bandwidth |
| D1,D2 | 1N4001 | To protect the device against output voltage spikes | | |

## SHORT CIRCUIT PROTECTION

The TDA 2030 has an original circuit which limits the current of the output transistors.Fig. 20 shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area (fig. 21). This function can therefore be considered as being peak power limiting rather than simple current limiting. The TDA 2030 is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time, the thermal shut-down protection keeps the junction temperature within safe limits.

Fig. 20 - Maximum output current vs. voltage [$V_{CEsat}$] across each output transitor

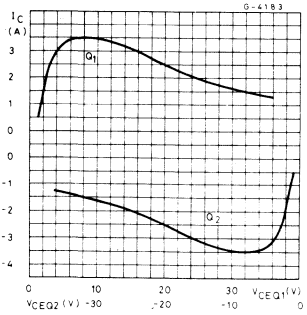
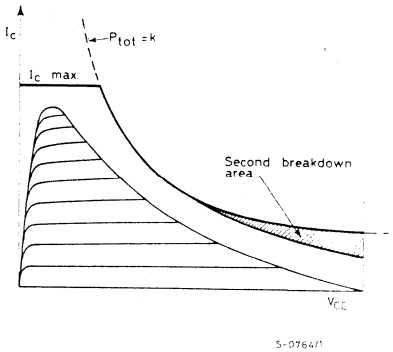



Fig. 21 - Safe operating area and collector characteristics of the protected power transistor




## THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the $T_j$ cannot be higher than 150°C.

2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); fig. 24 shows this dissipable power as a function of ambient temperature for different thermal resistance.

Fig. 22 - Output power and drain current vs. case temperature ($R_L = 4\Omega$)

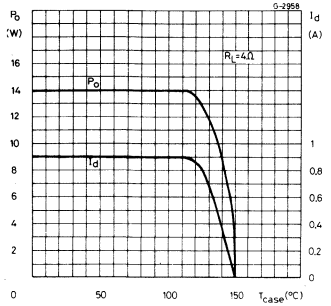



Fig. 23 - Output power and drain current vs. case temperature ($R_L = 8\Omega$)

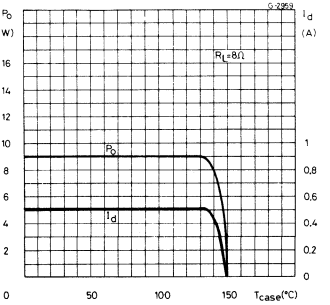



Fig. 24 - Maximum allowable power dissipation vs. ambient temperature

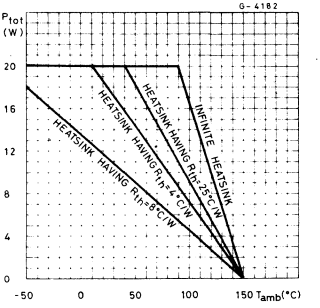
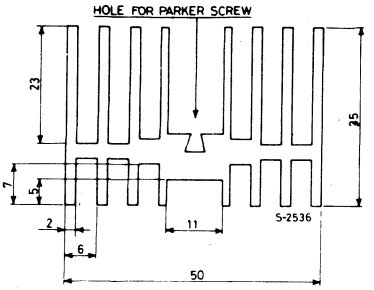



Fig. 25 - Example of heat-sink




Dimension : suggestion.

The following table shows the length that the heatsink in fig. 25 must have for several values of $P_{tot}$ and $R_{th}$.

| $P_{tot}$(W) | 12 | 8 | 6 |
|---|---|---|---|
| Length of heatsink (mm) | 60 | 40 | 30 |
| $R_{th}$ of heatsink (°C/W) | 4.2 | 6.2 | 8.3 |

# LINEAR INTEGRATED CIRCUITS

**TDA2030A**

**PRELIMINARY DATA**

## 18W Hi-Fi AMPLIFIER AND 30W DRIVER

The TDA 2030A is a monolithic IC in Pentawatt® package intended for use as low frequency class AB amplifier.
With $V_{s\ max}$= 44V it is particularly suited for more reliable applications without regulated supply and for 30W driver circuits using low-cost complementary pairs.
The TDA 2030A provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates a short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shut-down system is also included.

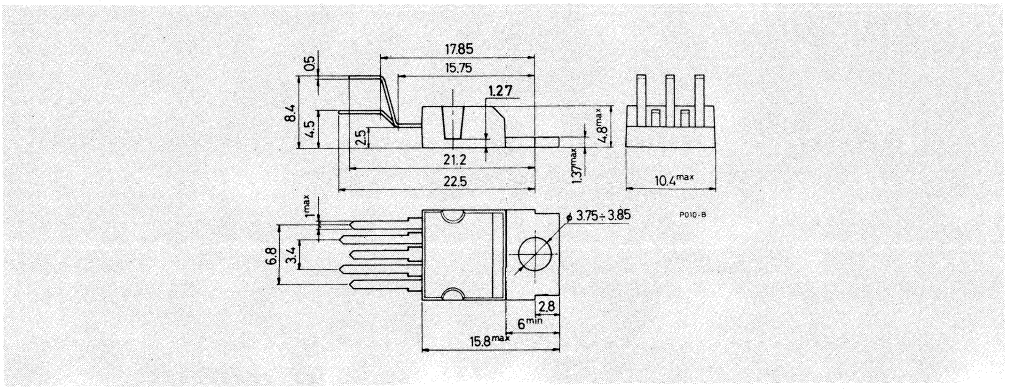
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | ± 22 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential input voltage | ± 15 | V |
| $I_o$ | Peak output current | 3.5 | A |
| $P_{tot}$ | Total power dissipation at $T_{case}$= 90°C | 20 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

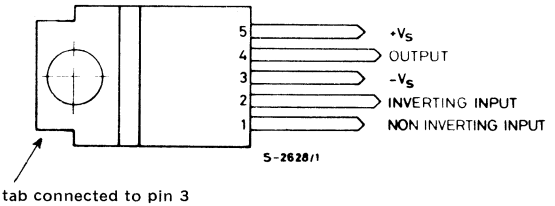
**ORDERING NUMBER:** TDA 2030AV

## MECHANICAL DATA

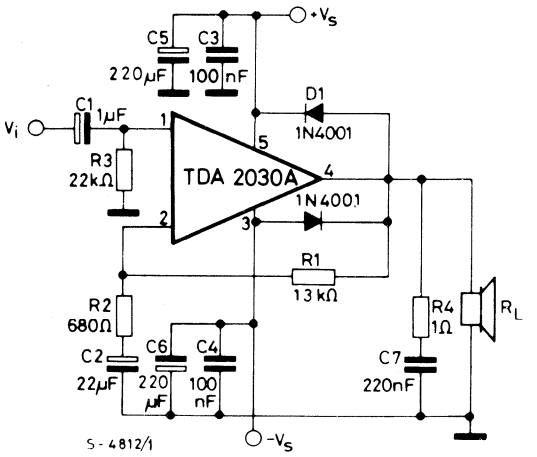
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s$= ±16V, $T_{amb}$= 25°C unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | ± 6 | | ± 22 | V |
| $I_d$ | Quiescent drain current | | | | 50 | 80 | mA |
| $I_b$ | Input bias current | $V_s$ = ± 22V | | | 0.2 | 2 | μA |
| $V_{os}$ | Input offset voltage | | | | ± 2 | ± 20 | mV |
| $I_{os}$ | Input offset current | | | | ± 20 | ± 200 | nA |
| $P_o$ | Output power | d = 0.5% $G_v$ = 26 dB<br>f = 40 to 15000 Hz<br>$R_L$= 4 Ω<br>$R_L$= 8 Ω | | 15<br>10 | 18<br>12 | | W |
| | | $V_s$ = ± 19V | $R_L$= 8Ω | 13 | 16 | | |
| BW | Power bandwidth | $P_o$= 15W | $R_L$= 4 Ω | | 100 | | KHz |
| SR | Slew Rate | | | | 8 | | V/μsec |
| $G_v$ | Open loop voltage gain | f = 1 KHz | | | 80 | | dB |
| $G_v$ | Closed loop voltage gain | | | 25.5 | 26 | 26.5 | dB |
| d | Total harmonic distortion | $P_o$= 0.1 to 14W<br>$R_L$= 4 Ω<br>f = 40 to 15000 Hz<br>f = 1 KHz | | | 0.08<br>0.03 | | % |
| | | $P_o$ = 0.1 to 9W<br>$R_L$= 8 Ω<br>f = 40 to 15000 Hz | | | 0.05 | | % |
| $d_2$ | Second order CCIF intermodulation distortion | $P_o$= 4W<br>$R_L$= 4Ω | $f_2$-$f_1$ = 1 KHz | | 0.03 | | % |
| $d_3$ | Third order CCIF intermodulation distortion | $f_1$= 14 KHz<br>$f_2$= 15 KHz | 2 $f_1$-$f_2$= 13KHz | | 0.08 | | % |
| $e_N$ | Input noise voltage | B = curve A | | | 2 | | μV |
| | | B = 22 Hz to 22 KHz | | | 3 | 10 | |
| $i_N$ | Input noise current | B = curve A | | | 50 | | pA |
| | | B = 22 Hz to 22 KHz | | | 80 | 200 | |
| S/N | Signal to noise ratio | $R_L$= 4Ω<br>$R_g$= 10 KΩ<br>B = curve A | $P_o$ = 15W | | 106 | | dB |
| | | | $P_o$ = 1W | | 94 | | |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $R_i$ | Input resistance (pin 1) | (open loop) | f = 1 KHz | 0.5 | 5 | | MΩ |
| SVR | Supply voltage rejection | $R_L$= 4 Ω<br>$R_g$= 22 KΩ | $G_V$= 26 dB<br>f = 100 Hz | | 54 | | dB |
| $T_j$ | Thermal shut-down junction temperature | | | | 145 | | °C |

Fig. 1 - Single supply amplifier

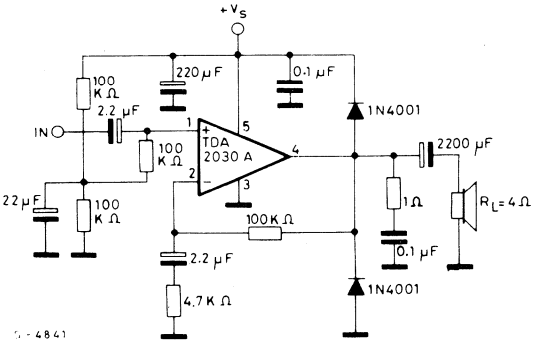



Fig. 2 - Open loop-frequency response

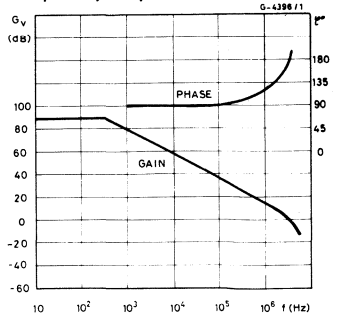



Fig. 3 - Output power vs. supply voltage

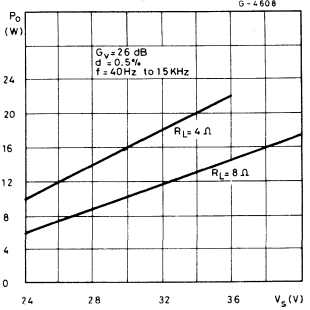
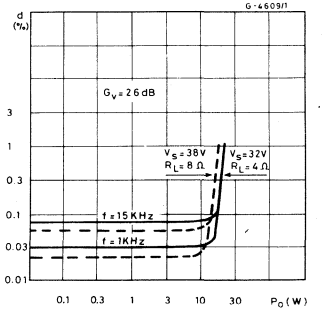



Fig. 4 - Total harmonic distortion vs. output power(*)




*) Test using noise filters.

Fig. 5 - Two tone CCIF intermodulation distortion

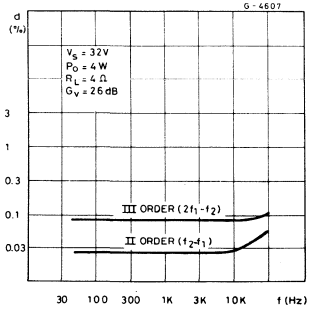



Fig. 6 - Large signal frequency response

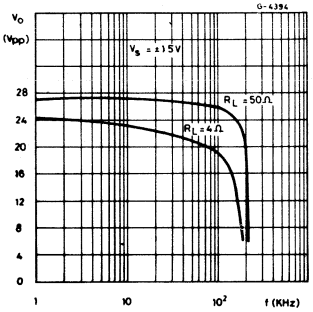



Fig. 7 - Maximum allowable power dissipation vs. ambient temperature

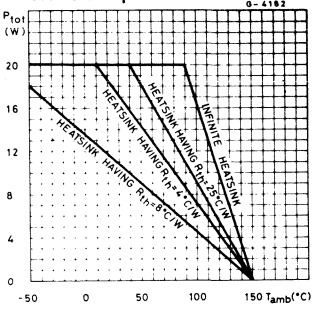



Fig. 8 - Single supply high power amplifier (TDA 2030A + BD907/BD908)

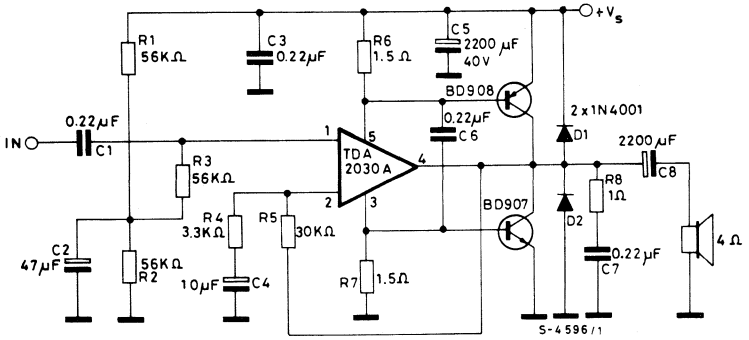
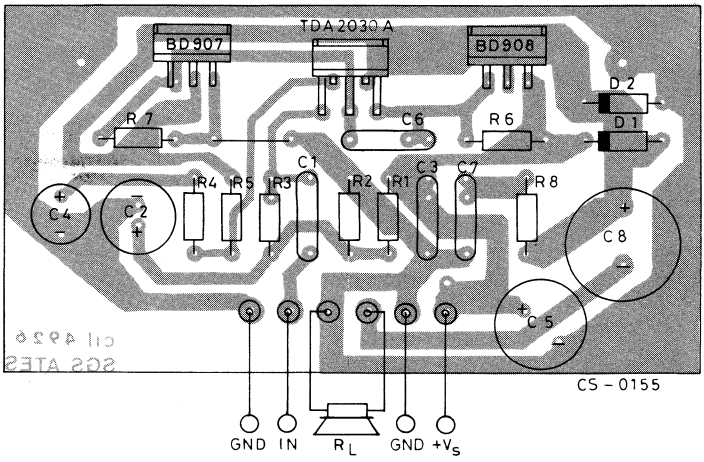


Fig. 9 - P.C. board and component layout for the circuit of fig. 8 (1:1 scale)




## Typical performance of the circuit of fig. 8

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | | 36 | 44 | V |
| $I_d$ | Quiescent drain current | $V_s$ = 36V | | | 50 | | mA |
| $P_o$ | Output power | d = 0.5%<br>$R_L$ = 4Ω<br>f = 40Hz to 15KHz | $V_s$ = 39V | | 35 | | W |
| | | | $V_s$ = 36V | | 28 | | |
| | | d = 10%; f = 1KHz | $V_s$ = 39V | | 44 | | W |
| | | $R_L$ = 4Ω | $V_s$ = 36V | | 35 | | |
| $G_v$ | Voltage gain | f = 1 KHz | | 19.5 | 20 | 20.5 | dB |
| SR | Slew Rate | | | | 8 | | V/μsec |
| d | Total harmonic distortion | | f = 1KHz | | 0.02 | | % |
| | | $P_o$ = 20W | f = 40 Hz to 15 KHz | | 0.05 | | |
| $V_i$ | Input sensitivity | $G_v$ = 20 dB<br>$P_o$ = 20W | f = 1 KHz<br>$R_L$ = 4Ω | | 890 | | mV |
| S/N | Signal to noise ratio | $R_L$ = 4Ω<br>$R_g$ = 10 KΩ<br>B = curve A | $P_o$ = 25W | | 108 | | dB |
| | | | $P_o$ = 4W | | 100 | | |

Fig. 10 - Output power vs. supply voltage

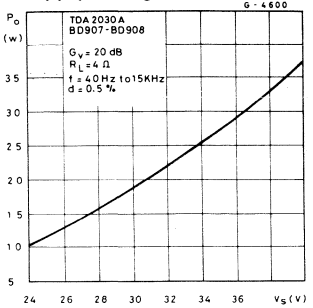



Fig. 11 - Total harmonic distortion vs. output power

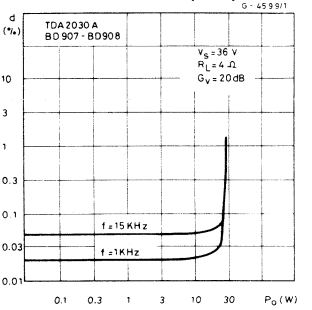



Fig. 12 - Output power vs. input level

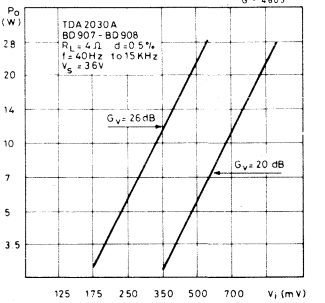



Fig. 13 - Power dissipation vs. output power

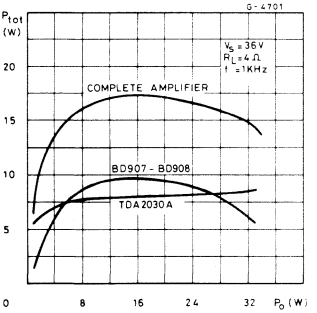



Fig. 14 - Typical amplifier whit split power supply

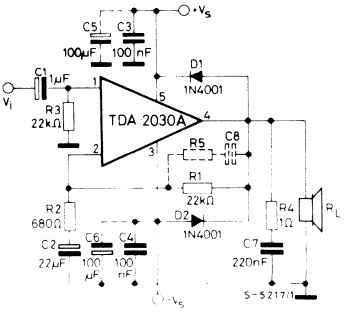



Fig. 15 - P.C. board and component layout for the circuit of fig. 14 (1 : 1 scale)

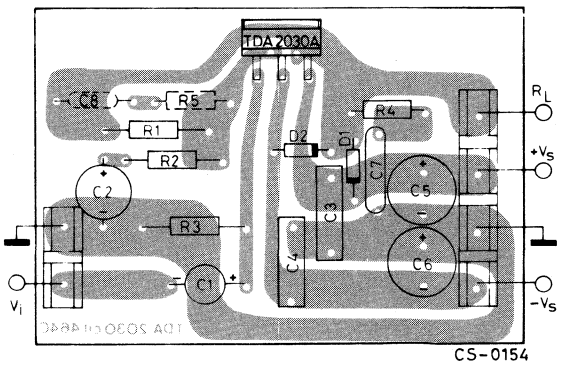


Fig. 16 - Bridge amplifier whit split power supply ($P_o$= 34W, $V_s$= ±16V)

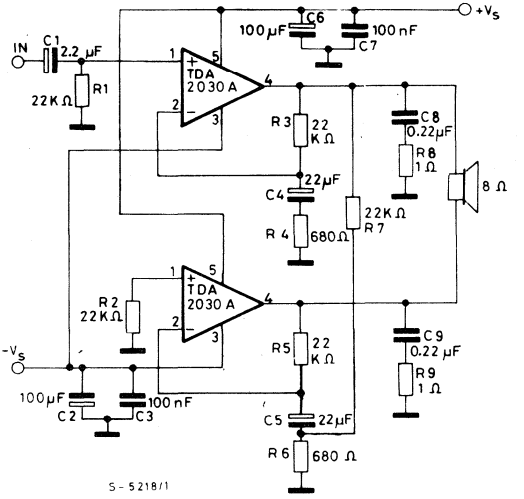
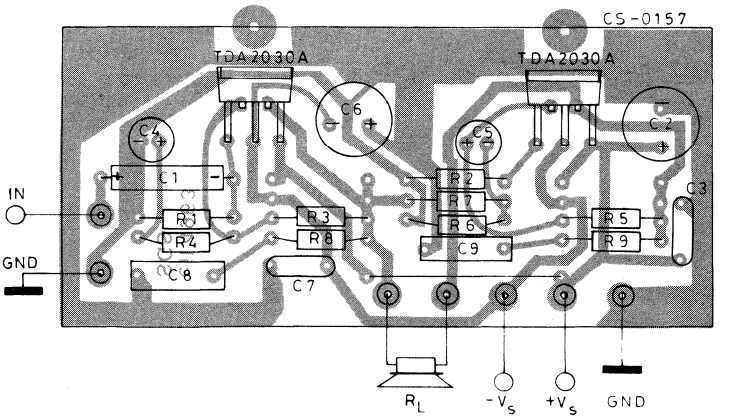



Fig. 17 - P.C. board and component layout for the circuit in fig. 16 (1:1 scale)



## Multiway speaker systems and active boxes

Multiway loudspeaker systems provide the best possible acoustic performance since each loudspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two or three bands.
To maintain a flat frequency response over the Hi-Fi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segment of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum to determine the cutoff frequencies of the crossover filters (see fig. 18). As an example, a 100W three-way system with crossover frequencies of 400 Hz and 3 KHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.
Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters:

- power loss
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance.

Fig. 18 - Power distribution vs. frequency

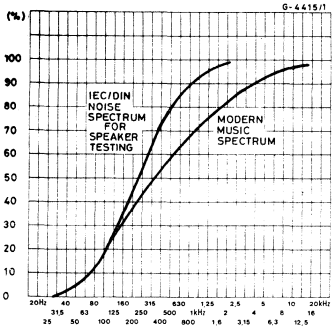
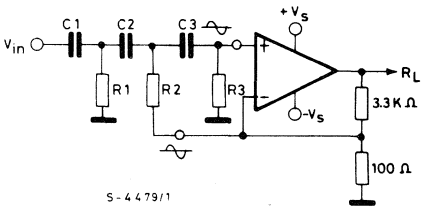



Fig. 19 - Active power filter



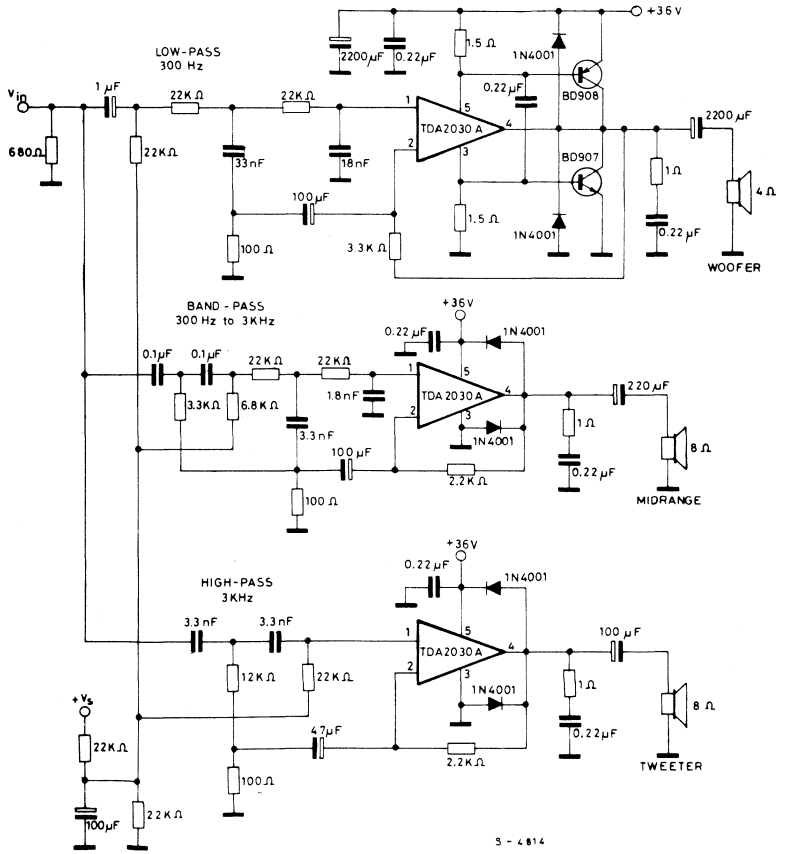

Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit.
This makes it particularly interesting and economically sound to use monolithic power amplifiers.
In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6 dB/octave) can be recommended.
The results obtained are excellent because this is the best type of audio filter and the only one free from phase and transient distortion.
The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.
A more effective solution, named "Active Power Filter" by SGS is shown in fig. 19.
The proposed circuit can realize combined power amplifiers and 12 dB/octave or 18 dB/octave high-pass or low-pass filters.
In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.
The impedance at the pin (−) is of the order of 100Ω, while that of the pin (+) is very high, which is also what was wanted.

The component values calculated for $f_c$ = 900 Hz using a Bessel 3rd order Sallen and Key structure are:

| $C_1 = C_2 = C_3$ | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|
| 22 nF | 8.2 KΩ | 5.6 KΩ | 33 KΩ |

Using this type of crossover filter, a complete 3-way 60W active loudspeaker system is shown in fig. 20. It employs 2nd order Buttherworth filters with the crossover frequencies equal to 300 Hz and 3 KHz. The midrange section consists of two filters, a high pass circuit followed by a low pass network.
With $V_s$ = 36V the output power delivered to the woofer is 25W at d = 0.06% (30W at d = 0.5%). The power delivered to the midrange and the tweeter can be optimized in the design phase taking in account the louspeaker efficiency and impedance ($R_L$ = 4Ω or 8Ω).
It is quite common that midrange and tweeter speakers have an efficiency 3 dB higher than woofers.

Fig. 20 - 3 way 60W active loudspeaker system ($V_s$ = 36V)



## Musical instruments amplifiers

Another important field of application for active systems is music.
In this area the use of several medium power amplifiers is more convenient than a single high power amplifier, and it is also more reliable.
A typical example (see fig. 21) consist of four amplifiers each driving a low-cost, 4Ω, 12 inch loudspeaker. This application can supply 80 to 160W rms.
Similar output power can be obtained by a single amplifier using the "superbridge" circuit of fig. 23 As shown in the diagram of fig. 22 this circuit can supply output power of 120W and more.

Fig. 21 - High power active box for musical instrument

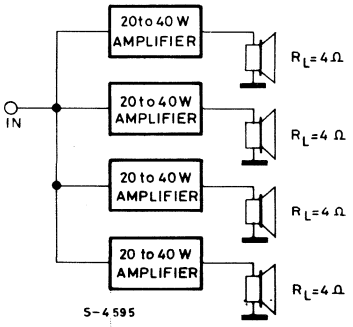



Fig. 22 - Output power vs. supply voltage (application circuit of fig. 23)

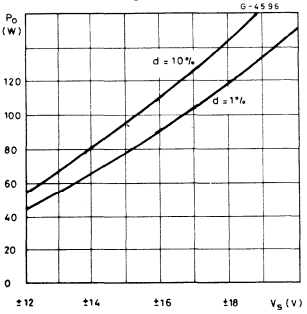
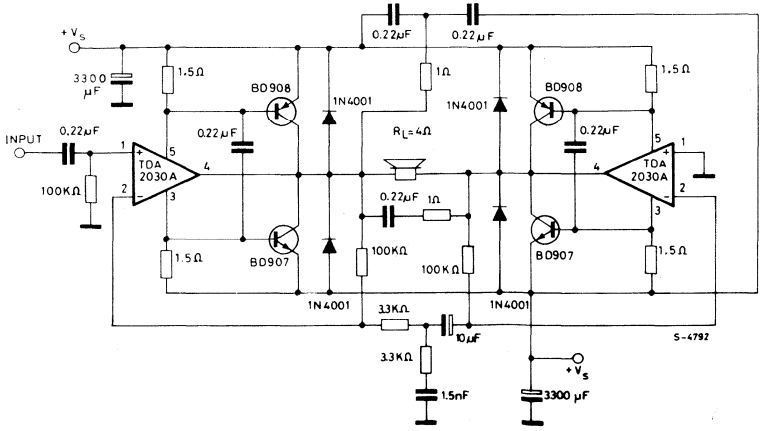



Fig. 23 - 120W "superbridge" power amplifier



## Transient intermodulation distortion (TIM)

Transient intermodulation distortion is an unfortunate phenomen associated with negative-feedback amplifiers. When a feedback amplifier receives an input signal which rises very steeply, i.e. it contains high-frequency components, the feedback can arrive too late so that the amplifiers overloads and a burst of intermodulation distortion will be produced as in fig. 24. Since transients occur frequently in music this is obviously a problem for the designer of audio amplifiers. Unfortunately, heavy negative feedback is frequently used to reduce the total harmonic distortion of an amplifier, which tends to aggravate the transient intermodulation (TIM) situation. The best known method for the measurement of TIM consists of feeding sine waves superimposed onto square waves, into the amplifier under test. The output spectrum is then examined using a spectrum analyser and compared to the input. This method suffers from serious disadvantages: the accuracy is limited, the measurement is a rather delicate operation and an expensive spectrum analyser is essential. A new approach (see Technical Note 143) applied by SGS to monolithic amplifiers measurement is fast cheap-it requires nothing more sophisticated than an oscilloscope — and sensitive — and it can be used down to the values as low as 0.002% in high power amplifiers. The "inverting-sawtooth" method of measurement is based on the response of an amplifier to a 20 KHz sawtooth waveform. The amplifier has no difficulty following the slow ramp but it cannot follow the fast edge. The output will follow the upper line in fig. 25 cutting of the shaded area and thus increasing the mean level. If this output signal is filtered to remove the sawtooth, a direct voltage remains which indicates the amount of TIM distortion, although it is difficult to measure because it is indistinguishable from the d.c. offset of the amplifier. This problem is neatly avoided in the IS-TIM method by periodically inverting the sawtooth waveform at a low audio frequency as shown in fig. 26. In the case of the sawtooth in fig. 25 the mean level was increased by the TIM distortion, for a sawtooth in the other direction the opposite is true.

Fig. 24 - Overshoot phenomenon in feedback amplifiers

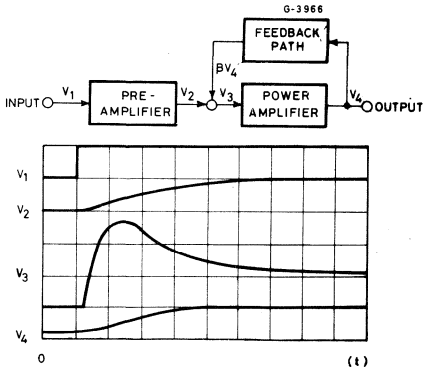
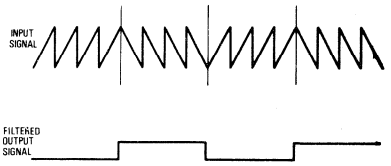



Fig. 25 - 20 KHz sawtooth waveform




Fig. 26 - Inverting sawtooth waveform




The result is an a.c. signal at the output whose peak-to-peak value is the TIM voltage, which can be measured easily with an oscilloscope.
If the peak-to-peak value of the signal and the peak-to-peak of the inverting sawtooth are measured, the TIM can be found very simply from:

$$TIM = \frac{V_{out}}{V_{sawtooth}} \cdot 100$$

In fig. 27 the experimental results are shown for the 30W amplifier using the TDA2030A as a driver and a low-cost complementary pair.
The measured performances are perfectly suitable for Hi-Fi systems.
A simple RC filter on the input of the amplifier to limit the maximum signal slope (SS) is an effective way to reduce TIM.
The diagram of fig. 28 originated by SGS can be used to find the Slew-Rate (SR) required for a given output power or voltage and a TIM design target.
For example if an anti-TIM filter with a cutoff at 30 KHz is used and the max. peak-to-peak output voltage is 20V then, referring to the diagram, a Slew-Rate of 6V/μS is necessary for 0,1% TIM.
As shown Slew-Rates of above 10V/μS do not contribute to a further reduction in TIM.
Slew-Rates of 100V/μS are not only useless but also a disadvantage in Hi-Fi audio amplifiers because they tend to turn the amplifier into a radio receiver.

Fig. 27 - TIM distortion vs. output power

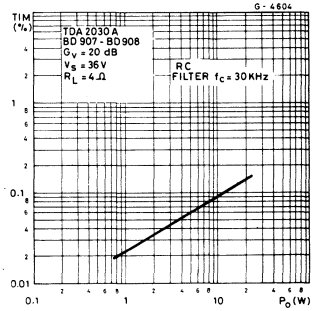
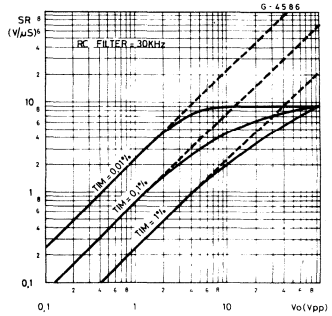



Fig. 28 - TIM design diagram ($f_C$= 30 KHz)

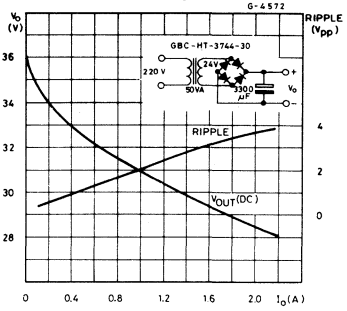



## Power supply

Using monolithic audio amplifier with non-regulated supply voltage it is important to design the power supply correctly. In any working case it must provide a supply voltage less than the maximum value fixed by the IC breakdown voltage.
It is essential to take into account all the working conditions, in particular mains fluctuations and supply voltage variations with and without load.
The TDA 2030A ($V_{s\ max}$= 44V) is particularly suitable for substitution of the standard IC power amplifiers (with $V_{s\ max}$= 36V) for more reliable applications.
An example, using a simple full-wave rectifier followed by a capacitor filter, is shown in the table and in the diagram of fig. 29.
A regulated supply is not usually used for the power output stages because of its dimensioning must be done taking into account the power to supply in the signal peaks. They are only a small percentage of the total music signal, with consequently large overdimensioning of the circuit.
Even if with a regulated supply higher output power can be obtained ($V_s$ is constant in all working conditions), the additional cost and power dissipation do not usually justify its use. Using non-regulated supplies, there are fewer design restriction. In fact, when signal peaks are present, the capacitor filter acts as a flywheel supplying the required energy.
In average conditions, the continuous power supplied is lower. The music power/continuous power ratio is greater in this case than for the case of regulated supplied, with space saving and cost reduction.

| Mains (220V) | Secondary voltage | DC output voltage ($V_o$) | | |
|---|---|---|---|---|
| | | $I_o$= 0 | $I_o$= 0.1A | $I_o$= 1A |
| +20% | 28.8V | 43.2V | 42V | 37.5V |
| +15% | 27.6V | 41.4V | 40.3V | 35.8V |
| +10% | 26.4V | 39.6V | 38.5V | 34.2V |
| – | 24V | 36.2V | 35V | 31V |
| -10% | 21.6V | 32.4V | 31.5V | 27.8V |
| -15% | 20.4V | 30.6V | 29.8V | 26V |
| -20% | 19.2V | 28.8V | 28V | 24.3V |

Fig. 29 - DC characteristics of 50W non-regulated supply




## SHORT CIRCUIT PROTECTION

The TDA 2030A has an original circuit which limits the current of the output transistors. This function can be considered as being peak power limiting rather than simple current limiting. The TDA 2030A is thus protected against temporary overloads or short circuit. Should the short circuit exist for a longer time, the thermal shut-down protection keeps the junction temperature within safe limits.

## THERMAL SHUT-DOWN

The presence of a thermal limiting circuit offers the following advantages:

1) An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the $T_j$ cannot be higher than 150°C.
2) The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases up to 150°C, the thermal shut-down simply reduces the power dissipation and the current consumption.

# LINEAR INTEGRATED CIRCUITS

**TDA2040**

**PRELIMINARY DATA**

## 20W Hi-Fi AUDIO POWER AMPLIFIER

The TDA 2040 is a monolithic integrated circuit in Pentawatt® package, intended for use as an audio class AB amplifier. Typically it provides 22W output power (d = 0.5%) at $V_s$ = 32V/4Ω. The TDA 2040 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates a patented short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A thermal shut-down system is also included.

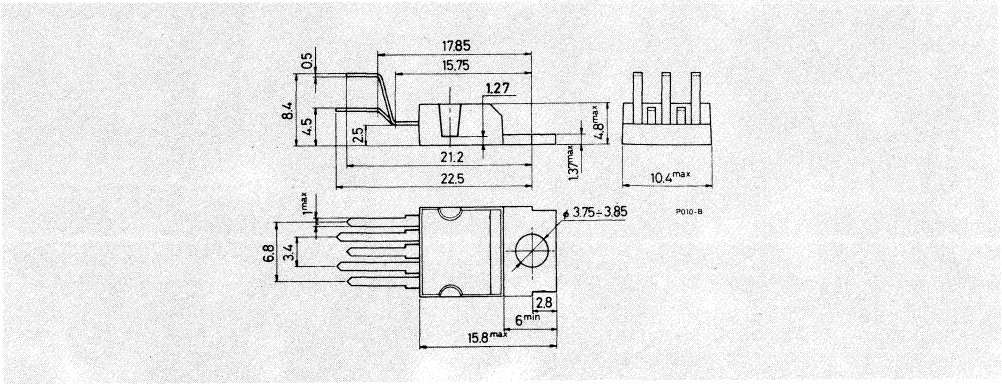
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | ± 20 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential input voltage | ± 15 | V |
| $I_o$. | Output peak current (internally limited) | 4 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$ = 75°C | 25 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

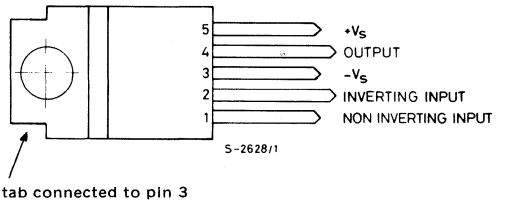
**ORDERING NUMBER:** TDA 2040V

## MECHANICAL DATA

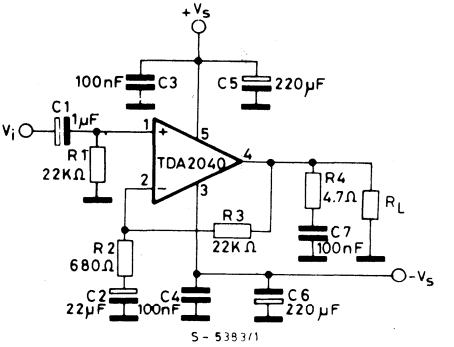
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## TEST CIRCUIT




## THERMAL DATA

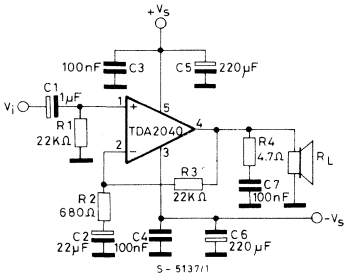
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s = \pm 16V$, $T_{amb} = 25°C$ unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | ± 2.5 | | | V |
| $I_d$ | Quiescent drain current | $V_s = \pm 4.5V$ | | | | 30 | mA |
| | | $V_s = \pm 20V$ | | | 45 | 100 | mA |
| $I_b$ | Input bias current | | | | 0.3 | 1 | μA |
| $V_{os}$ | Input offset voltage | | | | ± 2 | ± 20 | mV |
| $I_{os}$ | Input offset current | | | | | ±200 | nA |
| $P_o$ | Output power | d = 0.5%<br>f = 1 KHz | $T_{case} = 60°C$<br>$R_L = 4\Omega$<br>$R_L = 8\Omega$ | 20 | 22<br>12 | | W |
| | | f = 15 KHz | $R_L = 4\Omega$ | 15 | 18 | | W |
| BW | Power bandwidth | $P_o = 1W$ | $R_L = 4\Omega$ | | 100 | | KHz |
| $G_v$ | Open loop voltage gain | f = 1 KHz | | | 80 | | dB |
| $G_v$ | Closed loop voltage gain | | | 29.5 | 30 | 30.5 | dB |
| d | Total harmonic distortion | $P_o = 0.1$ to 10W | $R_L = 4\Omega$<br>f = 40 to 15000Hz<br>f = 1 KHz | | 0.08<br>0.03 | | % |
| $e_N$ | Input noise voltage | B = curve A | | | 2 | | μV |
| | | B = 22 Hz to 22 KHz | | | 3 | | |
| $i_N$ | Input noise current | B = curve A | | | 50 | | pA |
| | | B = 22 Hz to 22 KHz | | | 80 | | |
| $R_i$ | Input resistance (pin 1) | | | 0.5 | 5 | | MΩ |
| SVR | Supply voltage rejection | $R_L = 4\Omega$<br>$R_g = 22$ KΩ<br>$V_{ripple} = 0.5 V_{rms}$ | $G_v = 30$ dB<br>f = 100 Hz | 40 | 48 | | dB |
| $\eta$ | Efficiency | f = 1 KHz<br>$P_o = 12W$<br>$P_o = 22W$ | <br>$R_L = 8\Omega$<br>$R_L = 4\Omega$ | | <br>66<br>63 | | % |
| $T_j$ | Thermal shut-down junction temperature | | | | 145 | | °C |

## APPLICATION INFORMATION

Fig. 1 - Amplifier with split power supply (*)




$V_s = \pm 16V$
$R_L = 4\Omega$
$P_o \geqslant 15W$ (d = 0.5%)

Fig. 2 - P.C. board and components layout of the circuit of fig. 1.

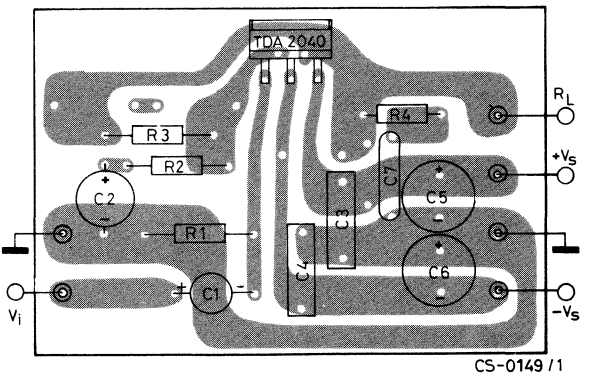
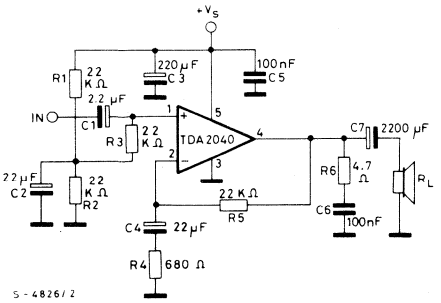
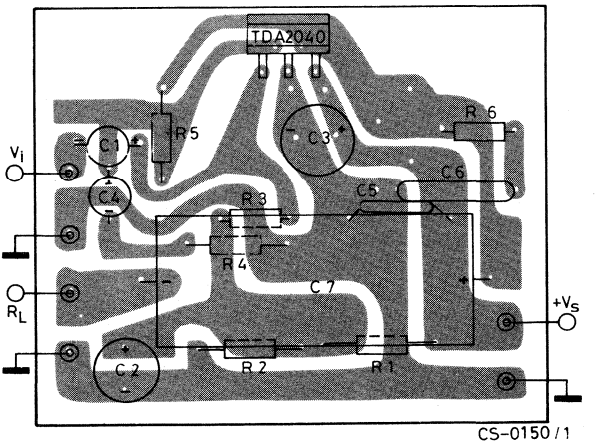



Fig. 3 - Amplifier with single supply (*)



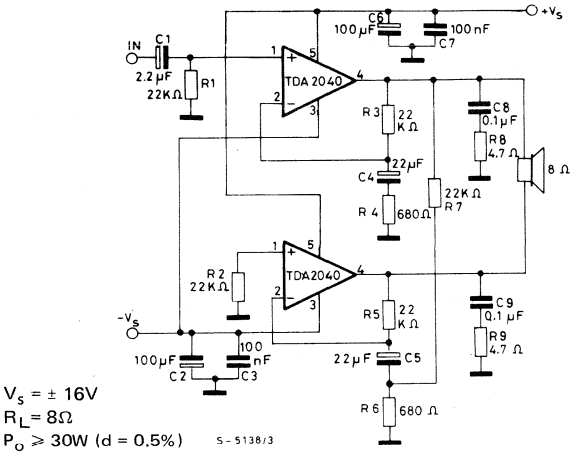

* In the case of highly inductive loads protection diodes may be necessary.

Fig. 4 - P.C. board and components layout of the circuit of fig. 3.



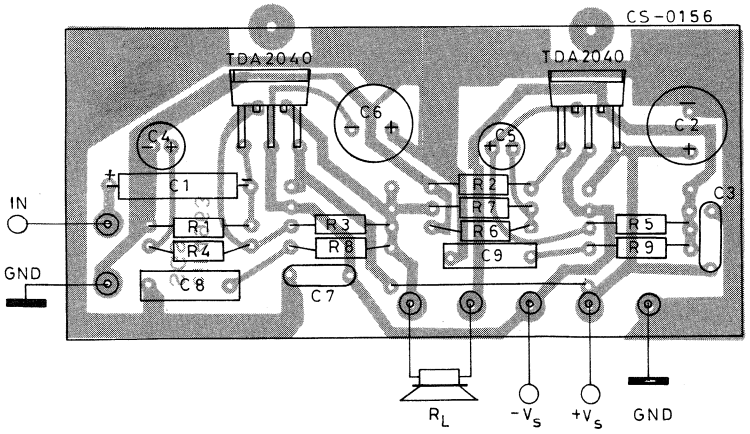
## APPLICATION INFORMATION (continued)

Fig. 5 - 30W Bridge amplifier with split power supply




$V_S$ = ± 16V
$R_L$ = 8Ω
$P_O$ ⩾ 30W (d = 0.5%) S-5138/3

Fig. 6 - P.C. board and components layout for the circuit of fig. 5.



## APPLICATION INFORMATION (continued)

### Multiway speaker systems and active boxes

Multiway loudspeaker systems provide the best possible acoustic performance since each lodspeaker is specially designed and optimized to handle a limited range of frequencies. Commonly, these loudspeaker systems divide the audio spectrum into two, three or four bands.
To maintain a flat frequency response over the HiFi audio range the bands covered by each loudspeaker must overlap slightly. Imbalance between the loudspeakers produces unacceptable results therefore it is important to ensure that each unit generates the correct amount of acoustic energy for its segment of the audio spectrum. In this respect it is also important to know the energy distribution of the music spectrum to determine the cutoff frequencies of the crossover filters (see fig. 7). As an example, a 100 W three-way system with crossover frequencies of 400 Hz and 3KHz would require 50W for the woofer, 35W for the midrange unit and 15W for the tweeter.
Both active and passive filters can be used for crossovers but today active filters cost significantly less than a good passive filter using air-cored inductors and non-electrolytic capacitors. In addition, active filters do not suffer from the typical defects of passive filters:
- power loss
- increased impedance seen by the loudspeaker (lower damping)
- difficulty of precise design due to variable loudspeaker impedance

Fig. 7 - Power distribution vs. frequency

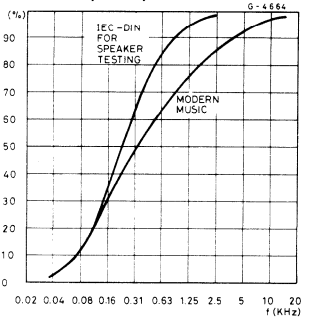
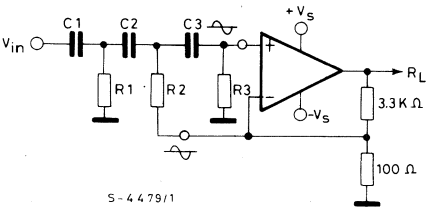



Fig. 8 - Active power filter



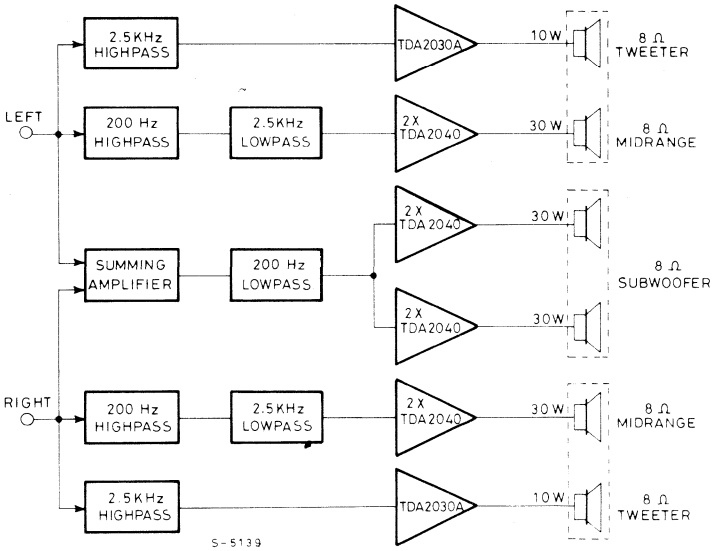

Obviously, active crossovers can only be used if a power amplifier is provided for each drive unit.
This makes it particularly interesting and economically sound to use monolithic power amplifiers.
In some applications, complex filters are not really necessary and simple RC low-pass and high-pass networks (6 dB/octave) can be recommended.
The results obtained are excellent because this is the best type of audio filter and the only one free from phase and transient distortion.
The rather poor out of band attenuation of single RC filters means that the loudspeaker must operate linearly well beyond the crossover frequency to avoid distortion.
A more effective solution, named "Active Power Filter" by SGS is shown in fig. 8.
The proposed circuit can realize combined power amplifiers and 12 dB/octave or 18 dB/octave high-pass or low-pass filters.
In practice, at the input pins of the amplifier two equal and in-phase voltages are available, as required for the active filter operation.
The impedance at the pin (–) is of the order of 100Ω, while that of the pin (+) is very high, which is also what was wanted.

The component values calculated for $f_c$ = 900 Hz using a Bessel 3rd order Sallen and Key structure are:

| C1 = C2 = C3 | R1 | R2 | R3 |
|---|---|---|---|
| 22 nF | 8.2 KΩ | 5.6 KΩ | 33 KΩ |

In the block diagram of fig. 9 is represented an active loudspeaker system completely realized using power integrated circuits, rather than the traditional discrete transistors or hybrids, very high quality is obtained by driving the audio spectrum into three bands using active crossovers (TDA 2320A) and a separate amplifier and loudspeaker for each band.
A modern subwoofer/midrange/tweeter solution is used.

Fig. 9 - High power active loudspeaker system using TDA 2030A and TDA 2040



# TDA2040A

# LINEAR INTEGRATED CIRCUITS

ADVANCE DATA

## 24W Hi-Fi AUDIO POWER AMPLIFIER

- SINGLE OR SPLIT SUPPLY OPERATION
- HIGH OUTPUT POWER
- VERY LOW CROSSOVER DISTORTION
- VERY LOW HARMONIC DISTORTION
- HIGH SLEW-RATE (14V/$\mu$s)
- SHORT CIRCUIT PROTECTION
- SOA PROTECTION
- OVERTEMPERATURE PROTECTION

The TDA 2040A is a monolithic integrated circuit in PENTAWATT package, intended for use as an audio class AB amplifier. Typically is provides 24W output power (d= 0.5%) at $V_s$= 32V/4$\Omega$. The TDA2040A provides high output current and was very low harmonic and cross-over distortion. Further the device incorporates a patented short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A thermal shut-down system is also included.

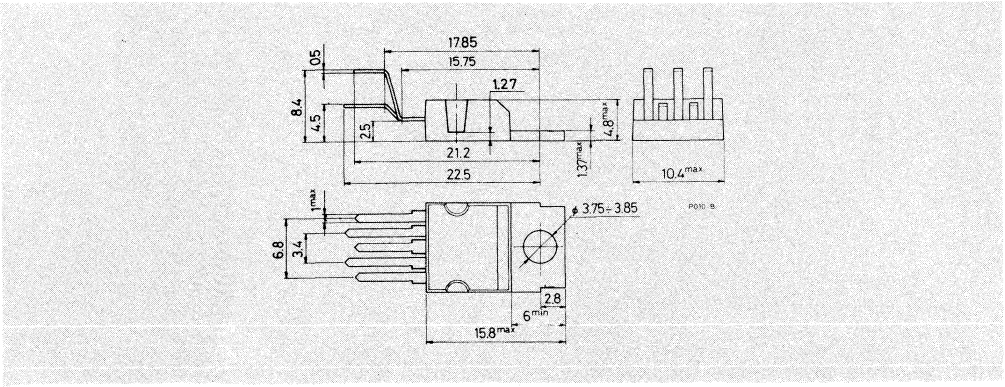
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | ± 20 | V |
| $V_i$ | Input voltage | $V_s$ | |
| $V_i$ | Differential input voltage | ± 15 | V |
| $I_o$. | Output peak current (internally limited) | 4 | A |
| $P_{tot}$ | Power dissipation at $T_{case}$ = 75°C | 25 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

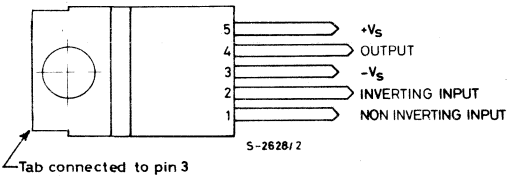
**ORDERING NUMBER:** TDA 2040AV

## MECHANICAL DATA

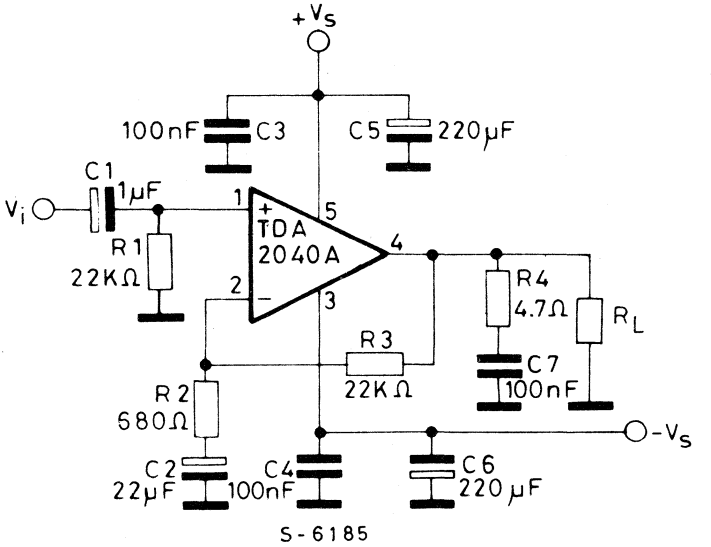
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |

**ELECTRICAL CHARACTERISTICS** (Refer to the test circuit, $V_s = \pm 16V$, $T_{amb} = 25°C$ unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | ±4 | | ±20 | V |
| $I_d$ | Quiescent drain current | | | 40 | | mA |
| | | | | 45 | 100 | mA |
| $I_b$ | Input bias current | $V_s = \pm 20V$ | | 0,3 | 1 | μA |
| $V_{os}$ | Input offset voltage | | | ±2 | ±20 | mV |
| $I_{os}$ | Input offset current | | | | ±200 | nA |
| $P_o$ | Output power | $R_L = 4\Omega$ f = 1KHz; d = 1% | 22 | 24 | | W |
| | | $R_L = 4\Omega$ f = 15KHz; d = 1% | | 22 | | W |
| SR | Slew-Rate | | | 14 | | V/μs |
| $G_v$ | Open loop voltage gain | f = 1 kHz | | 80 | | dB |
| $G_v$ | Closed loop voltage gain | f = 1 kHz | 29.5 | 30 | 30.5 | dB |
| d | Total harmonic distortion | $P_o$=0.1 to 10W $R_L = 4\Omega$ f = 1 KHz | | 0.05 | | % |
| $e_N$ | Input noise voltage | B = curve A | | 2 | | μV |
| | | B = 22Hz to 22KHz | | 3 | 10 | μV |
| $i_N$ | Input noise current | B = curve A | | 50 | | pA |
| | | B = 22 Hz to 22 KHz | | 80 | 200 | pA |
| S/N | Signal to noise ratio | $R_L = 4\Omega$ $R_g = 10K\Omega$ B = curve A; $P_o$ = 20W | | 103 | | dB |
| | | $R_L = 4\Omega$ $R_g = 10K\Omega$ B = curve A; $P_o$ = 2.5W | | 94 | | dB |
| $R_i$ | Input resistance (pin 1) | | 100 | 500 | | KΩ |
| SVR | Supply voltage rejection | $R_g = 22K\Omega$ f = 100Hz $V_{ripple} = 0.5V_{rms}$ | | 50 | | dB |
| $\eta$ | Efficiency | f = 1 KHz $P_o$ = 12W $R_L = 8\Omega$ | | 66 | | % |
| | | f = 1 KHz $P_o$ = 22W $R_L = 4\Omega$ | | 63 | | % |
| $T_j$ | Thermal shut-down juction temperature | | | 145 | | °C |

# LINEAR INTEGRATED CIRCUITS

**TDA2054M**

## PREAMPLIFIER WITH ALC FOR $C_rO_2$ CASSETTE RECORDERS

- EXCELLENT VERSATILITY IN USE ($V_S$ from 4 to 20V)
- HIGH OPEN LOOP GAIN
- LOW DISTORTION
- LOW NOISE
- LARGE AUTOMATIC LEVEL CONTROL RANGE
- STEREO MATCHING BETTER THAN 3 dB (matched pair)

The TDA 2054M is a monolithic integrated circuit in a 16-lead dual in-line plastic package.
The functions incorporated are:

– low noise preamplifier
– automatic level control system (ALC)
– high gain equalization amplifier

It is intended as preamplifier in tape and cassette recorders and players ($C_rO_2$), dictaphones, compressor and expander in telephonic equipments, Hi-Fi preamplifiers and in wire diffusion receivers; for stereo applications the ALC matching is better than 3 dB.

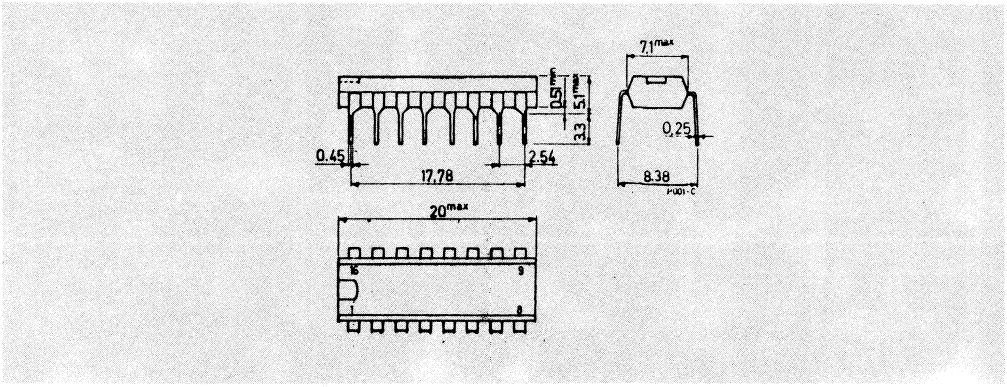
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_S$ | Supply voltage | 20 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb}$= 50°C | 500 | mW |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

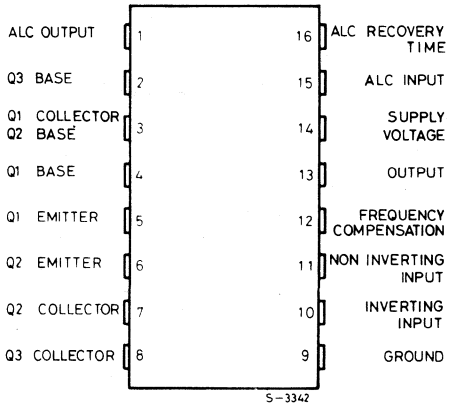
**ORDERING NUMBERS:** TDA 2054M mono applications
2 TDA 2054M stereo applications

## MECHANICAL DATA

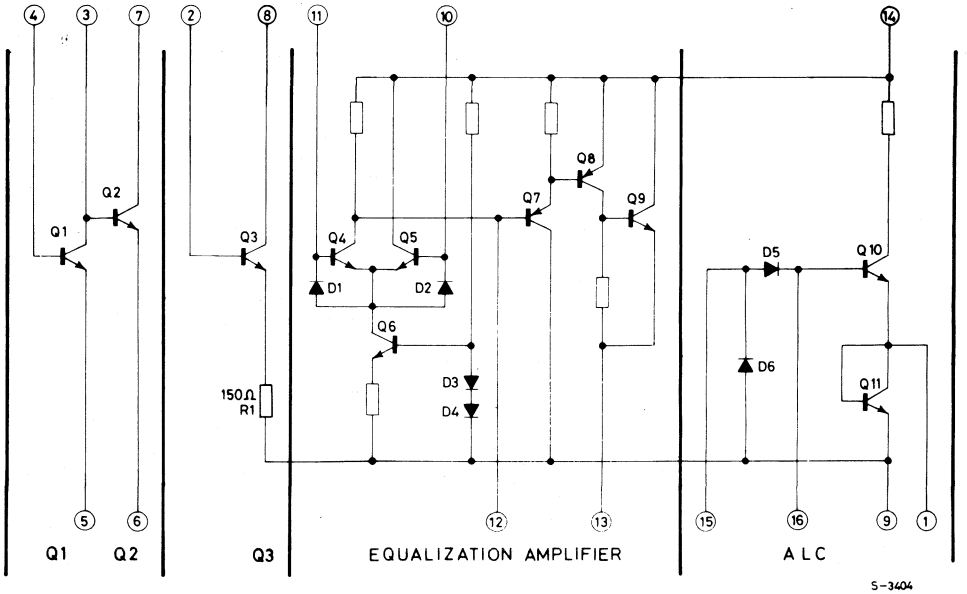
Dimensions in mm



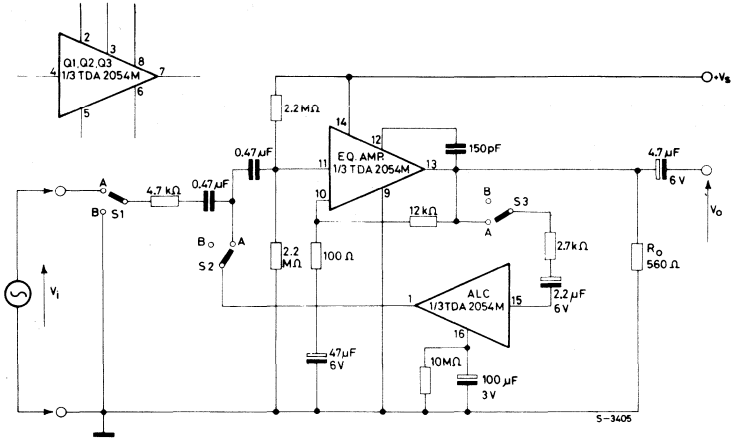
## CONNECTION DIAGRAM




## SCHEMATIC DIAGRAM



## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 200 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb}$= 25°C)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 4 | | 20 | V |
| $I_d$ | Quiescent drain current | $V_s$ = 9V<br>S1 = S2 = S3 = at B | | 10 | | mA |
| $h_{FE}$ | DC current gain (Q1, Q2, Q3) | $I_c$ = 0.1 mA $V_{CE}$= 5V | 300 | 500 | | — |
| $e_N$ | Input noise voltage (Q1, Q2, Q3) | $I_c$ = 0.1 mA $V_{CE}$= 5V<br>f = 1 KHz | | 2 | | $\frac{nV}{\sqrt{Hz}}$ |
| $i_N$ | Input noise current (Q1, Q2, Q3) | | | 0.5 | | $\frac{pA}{\sqrt{Hz}}$ |
| NF | Noise figure (Q1, Q2, Q3) | $I_c$ = 0.1 mA $V_{CE}$= 5V<br>$R_g$ = 4.7 KΩ<br>B (-3 dB)= 20 to 10000 Hz | | 0.5 | 4 | dB |
| $G_v$ | Open loop voltage gain(for equalization amplifier) | $V_s$ = 9V f = 1 KHz | | 60 | | dB |
| $V_o$ | Output voltage with A.L.C. | $V_s$ = 9 V $V_i$ = 100 mV<br>f = 1 KHz S1= S2= S3 at A | | 0.6 | | V |
| $e_N$ | Equivalent input noise voltage (for equalization amplifier pin 11) | $V_s$ = 9V<br>$G_v$ = 40 dB S1 at B<br>B (-3 dB)= 20 to 20000 Hz | | 1.3 | | µV |
| $R_1$ | Q3 emitter resistance | | 105 | 150 | 195 | Ω |

Fig. 1 - Equivalent input spot voltage and noise current vs. bias current (transistors Q1, Q2, Q3)

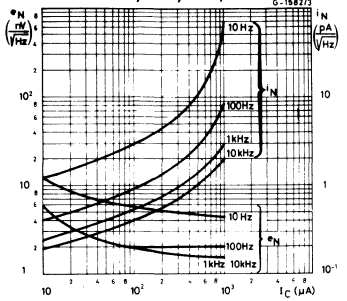



Fig. 2 - Equivalent input noise current vs. frequency (transistors Q1, Q2, Q3)

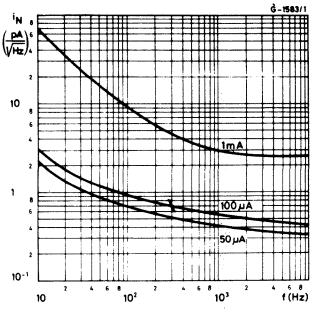



Fig. 3 - Equivalent input noise voltage vs. frequency (transistors Q1, Q2, Q3)

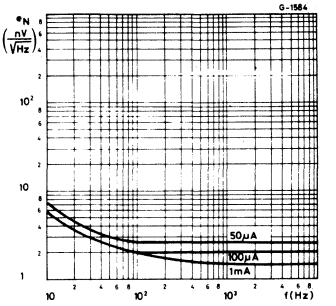



Fig. 4 - Noise figure vs. bias current (transistors Q1, Q2, Q3)

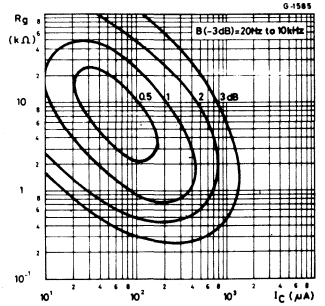



Fig. 5 - Optimum source resistance and minimum NF vs. bias current (transistors Q1, Q2, Q3)

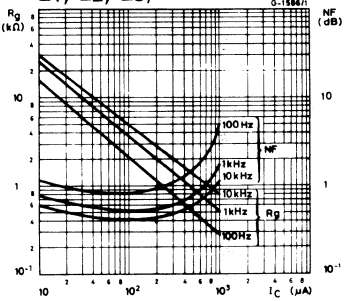



Fig. 6 - Current gain vs. collector current (transistors Q1, Q2, Q3)

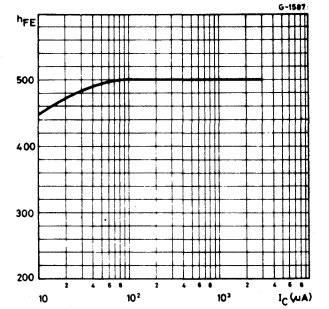



Fig. 7 - Open loop gain vs. frequency (equalization amplifier)

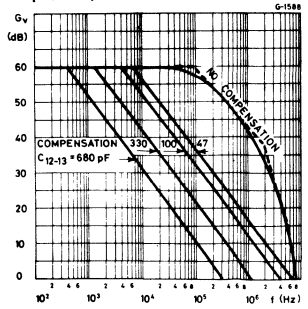



Fig. 8 - Open loop phase response vs. frequency(equalization amplifier)

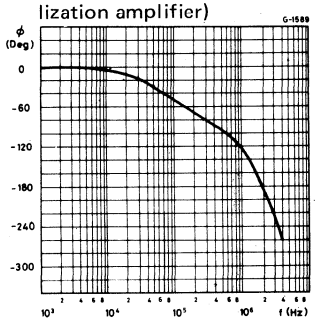
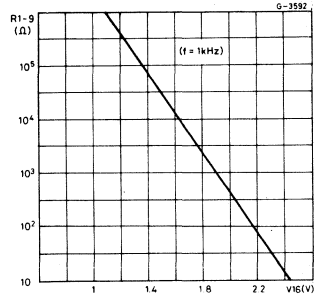



Fig. 9 - Dinamic resistance $R_{1-9}$ vs. ALC voltage $V_{16}$



## APPLICATION INFORMATION

Fig. 9 - Application circuit for $C_rO_2$ cassette player and recorder

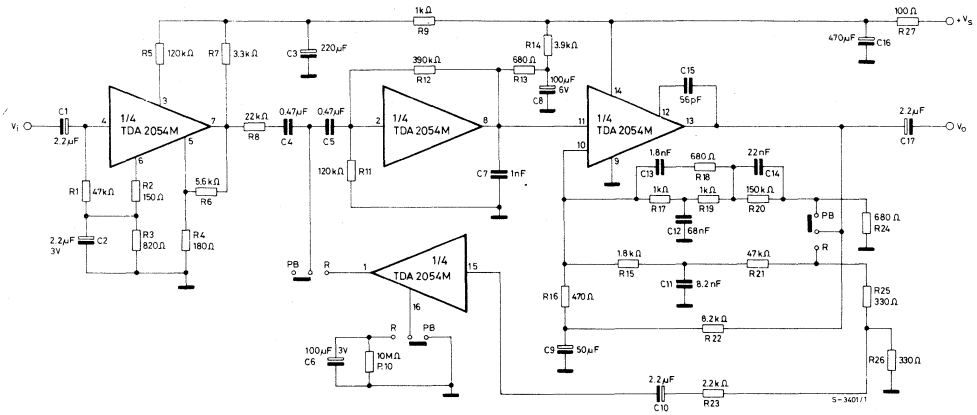
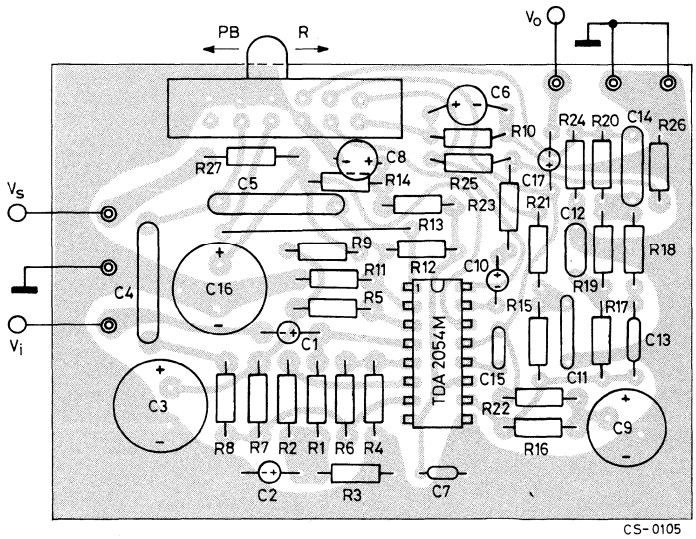



Fig. 10 - P.C. board and component layout for the circuit of Fig. 9 (1:1 scale)



## TYPICAL PERFORMANCE OF CIRCUIT IN FIG. 9 ($T_{amb}$= 25°C, $V_s$ = 9V)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **PLAYBACK** | | | | | | |
| $G_v$ | Voltage gain (open loop) | f = 20 to 20000 Hz | | 134 | | dB |
| $G_v$ | Voltage gain (closed loop) | f = 1 KHz | | 60 | | dB |
| $Z_i$ | Input impedance | f = 100 Hz<br>f = 1 KHz<br>f = 10 KHz | | 10<br>41<br>43 | | KΩ<br>KΩ<br>KΩ |
| $Z_o$ | Output impedance | f = 1 KHz | | 12 | 35 | Ω |
| B | Frequency response | | | see fig. 11 | | |
| d | Distortion | $V_o$ = 1V f = 1 KHz | | 0.2 | | % |
| | Output background noise | $Z_g$ = 300Ω + 120 mH (DIN 45405) | | 1.5 | | mV |
| *** | Output weighted background noise | | | 1 | | mV |
| $\frac{S+N}{N}$ | Signal to noise ratio | $V_o$ = 1.5V<br>$Z_g$ = 300Ω + 120 mH | | 60 | | dB |
| $t_{on}$* | Switch-on time | $V_o$ = 1V | | 500 | | ms |
| **RECORDING** | | | | | | |
| $G_v$ | Voltage gain (open loop) | f = 20 to 20000 Hz | | 134 | | dB |
| $G_v$ | Voltage gain (closed loop) | f = 1 KHz | | 72 | | dB |
| B | Frequency response | | | see fig. 13 | | |
| d | Distortion with ALC | $V_o$ = 1V f = 10 KHz | | 0.5 | | % |
| ALC | Automatic level control range(for 3 dB of output voltage variation) | $V_i \leqslant$ 40 mV f = 10 KHz | | 54 | | dB |
| $V_o$ | Output voltage before clipping without ALC | f = 1 KHz | | 3 | | V |
| $V_o$ | Output voltage with ALC | $V_i$ = 30 mV f = 1 KHz | | 1.1 | | V |
| $t_l$* | Limiting time (see fig. 17) | $\Delta V_i$= +40 dB f = 1 KHz | | 75 | | ms |
| $t_{set}$* | Level setting time (see fig. 17) | | | 300 | | ms |
| $t_{rec}$* | Recovery time (see fig. 17) | $\Delta V_i$= -40 dB f = 1 KHz | | 150 | | sec. |
| $t_{on}$* | Switch-on-time | $V_o$ = 1V | | 500 | | ms |
| $\frac{S+N}{N}$*** | Signal to noise ratio with ALC | $V_o$ = 1V $R_g$ = 470Ω | | 64 | | dB |

* This value depends on external network.

** When the DIN 45511 norm for frequency response is not mandatory the equalization peak at 15 KHz can be avoided - so halving the output noise.

*** Weighted noise measurement (DIN 45405).

Fig. 11 - Frequency response for the circuit in fig. 9 (playback)

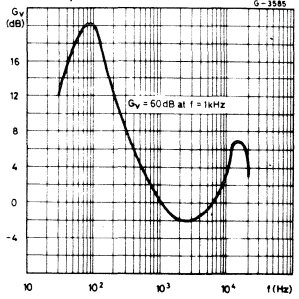



Fig. 12 - Distortion vs. frequency for the circuit in fig. 9 (playback)

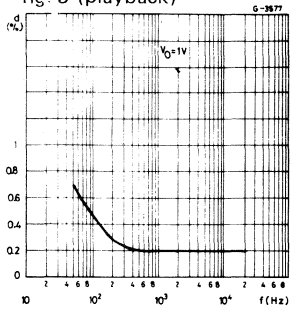



Fig. 13 - Frequency response for the circuit in fig. 9 (recording)

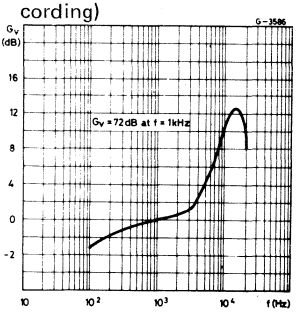



Fig. 14 - Output voltage variation and distortion with ALC vs. input voltage for the circuit in fig. 9 (recording)

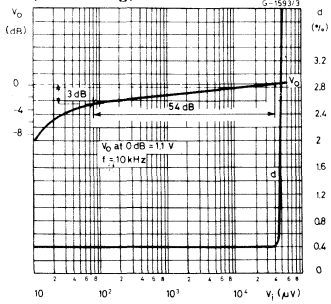



Fig. 15 - Distortion vs. frequency with ALC for the circuit in fig. 9 (recording)

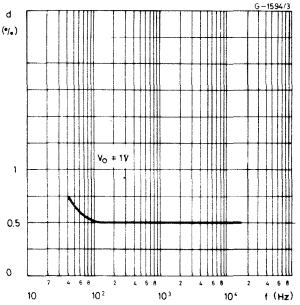



Fig. 16 - Limiting and level setting time vs. input signal variation

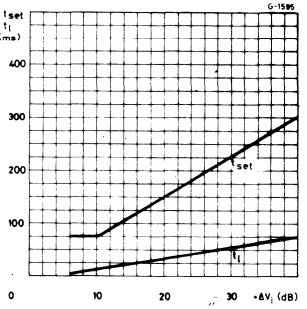
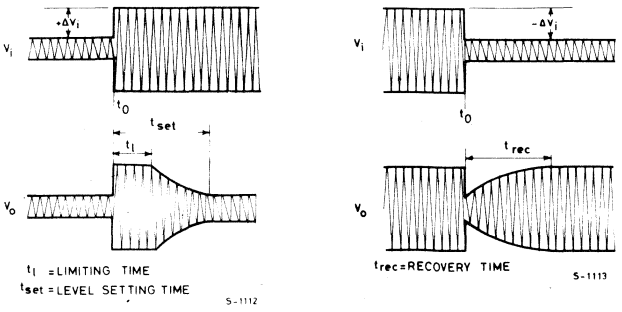



Fig. 17 - Limiting, level setting, recovery time



# TDA2170

# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## TV VERTICAL DEFLECTION OUTPUT CIRCUIT

The TDA 2170 is a monolithic integrated circuit in 11-lead Multiwatt® package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Colour and B & W television receivers as well as in monitors and displays. The functions incorporated are:

- power amplifier
- flyback generator
- reference voltage
- thermal protection

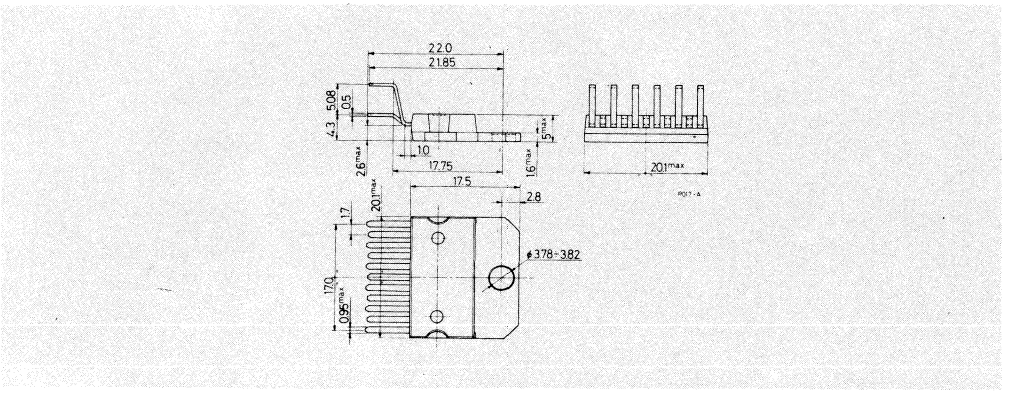
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 4) | 35 | V |
| $V_7$, $V_8$ | Flyback peak voltage | 60 | V |
| $V_5$ | Voltage at pin 5 | $+ V_s$ | |
| $V_2$, $V_3$ | Amplifier input voltage | $+ V_s$ | |
| $I_o$ | Output peak current (non repetitive, t = 2 msec) | -0.5<br>2.5 | V<br>A |
| $I_o$ | Output peak current at f = 50 Hz, $t \leqslant 10$ μsec | 3 | A |
| $I_o$ | Output peak current at f = 50 Hz, $t > 10$ μsec | 2 | A |
| $I_5$ | Pin 5 DC current at $V_7 < V_4$ | 100 | mA |
| $I_5$ | Pin 5 peak to peak flyback current at f = 50 Hz, $t_{fly} \leqslant 1.5$ msec | 3 | A |
| $P_{tot}$ | Total power dissipation at $T_{case} = 60°C$ | 30 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

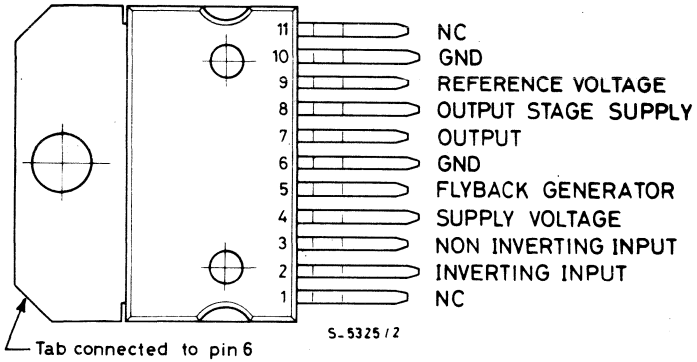
**ORDERING NUMBER:** TDA 2170

## MECHANICAL DATA

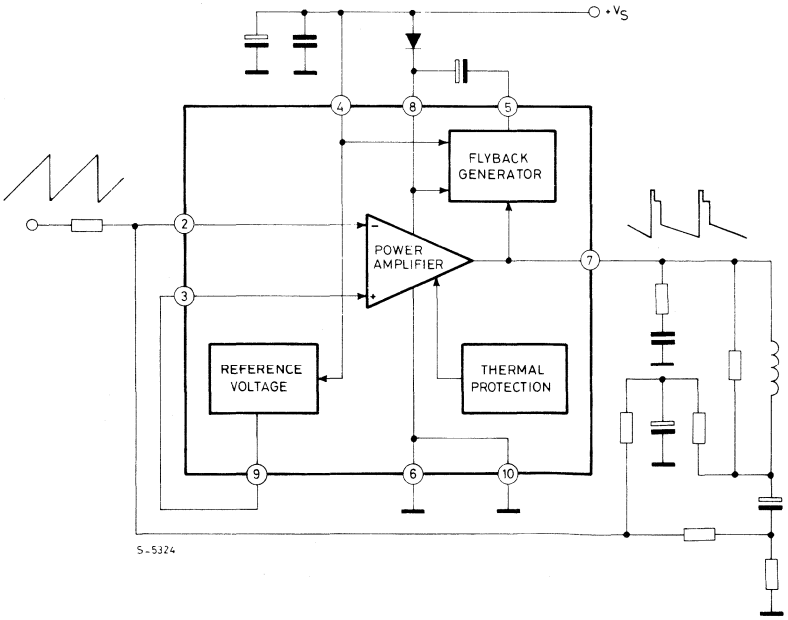
Dimensions in mm



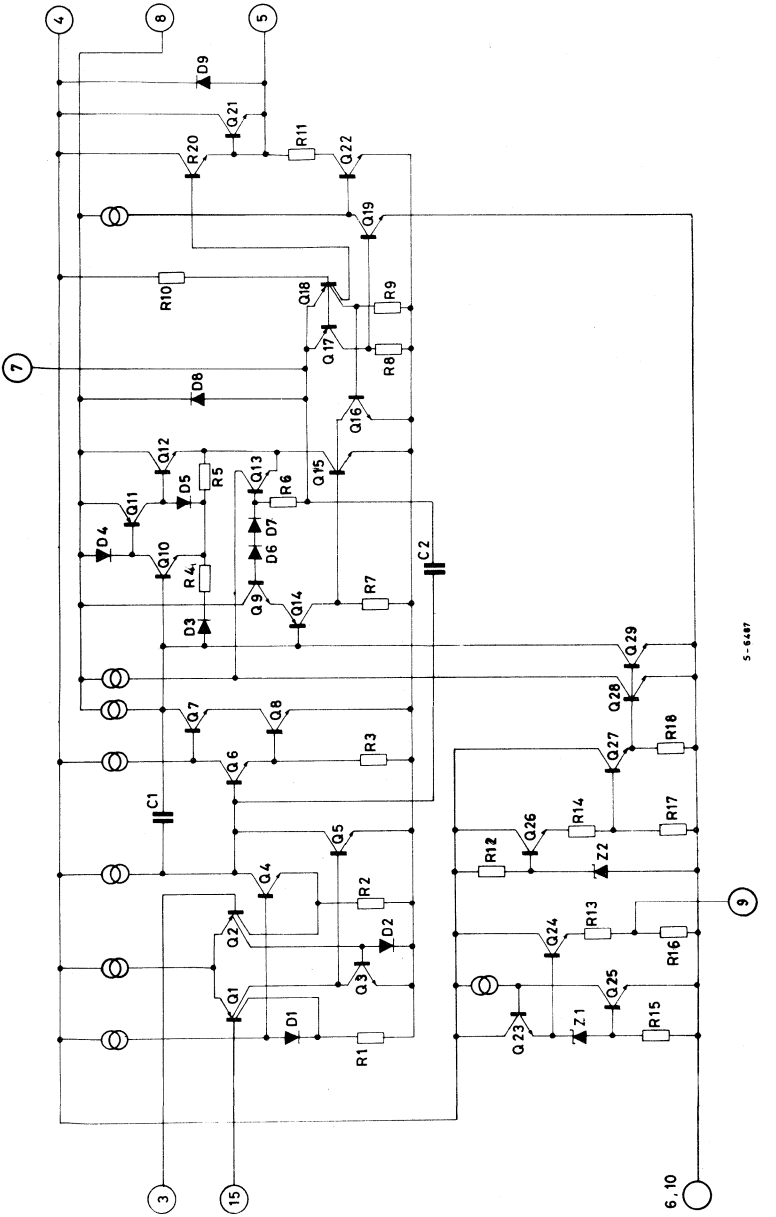
## CONNECTION DIAGRAM
(top view)




## BLOCK DIAGRAM



## SCHEMATIC DIAGRAM



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 3 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 40 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_s$ = 35V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| $I_4$ | Pin 4 quiescent current | $I_5 = 0$; $I_7 = 0$; $V_3 = 3V$ | | 8 | 16 | mA | 1a |
| $I_8$ | Pin 8 quiescent current | $I_5 = 0$; $I_7 = 0$; $V_3 = 3V$ | | 16 | 36 | mA | 1a |
| $I_3$ | Amplifier input bias current | $V_3 = 1V$ | | -0.1 | -1 | μA | 1a |
| $I_2$ | Amplifier input bias current | $V_2 = 1V$ | | -0.1 | -1 | μA | 1a |
| $V_9$ | Reference voltage | $I_9 = 0$ | | 2.2 | | V | 1a |
| $\frac{\Delta V_9}{\Delta V_s}$ | Reference voltage drift vs. supply voltage | $V_s$ = 15 to 30V | | 1 | 2 | mV/V | 1a |
| $V_{5L}$ | Pin 5 saturation voltage to GND | $I_5$ = 20 mA | | 1 | | V | 1c |
| $V_7$ | Quiescent output voltage | $V_s$ = 35V; $R_a$ = 39 KΩ | | 18 | | V | 1d |
| | | $V_s$ = 15V; $R_a$ = 13 KΩ | | 7.5 | | V | 1d |
| $V_{7L}$ | Output saturation voltage to GND | $I_7$ = 1.2A | | 1 | 1.4 | V | 1c |
| | | $I_7$ = 0.7A | | 0.7 | 1 | V | 1c |
| $V_{7H}$ | Output saturation voltage to supply | $-I_7$ = 1.2A | | 1.6 | 2.2 | V | 1b |
| | | $-I_7$ = 0.7A | | 1.3 | 1.8 | V | 1b |
| R9 | Reference voltage output resistance | | | 2.1 | | KΩ | |
| $T_j$ | Junction temperature for thermal shut down | | | 140 | | °C | |

Fig. 1 - DC test circuits

Fig. 1a - Measurement of $I_2$; $I_3$; $I_4$; $I_8$; $V_9$; $\Delta V_9/\Delta V_s$; R9

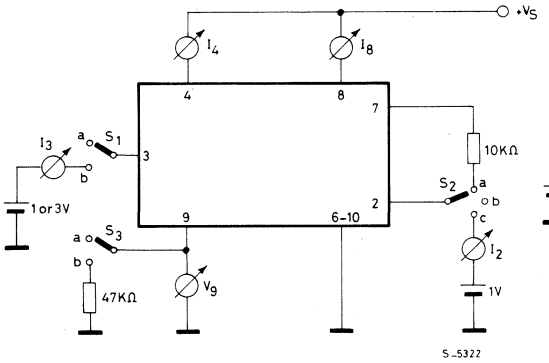
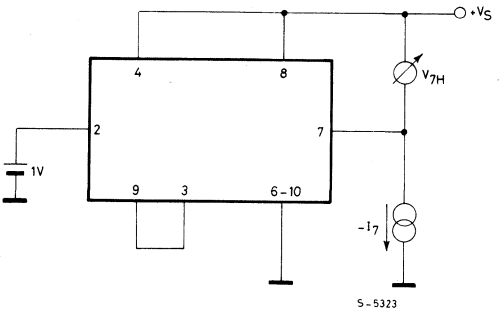



Fig. 1b - Measurement of $V7_H$




$S_1$ : (a) $I_2$; (b) $I_3$, $I_4$ and $I_8$.
$S_2$ : (a) $I_4$ and $I_8$; (b) $I_3$; (c) $I_2$.
$S_3$ : (a) $I_2$, $I_3$, $I_4$, $I_8$, $I_9$ and $V_9$; (b) R9.

Fig. 1c - Measurement of $V_{5L}$; $V_{7L}$

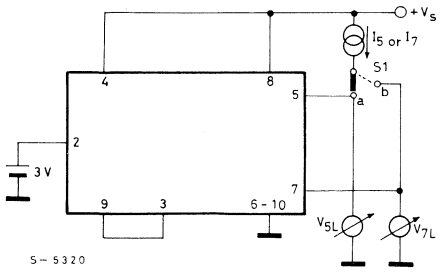
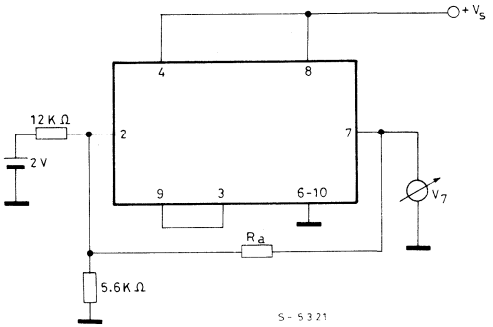



Fig. 1d - Measurement of $V_7$




S1 : (a) $V_{5L}$; (b) $V_{7L}$.

Fig. 2 - Application circuit

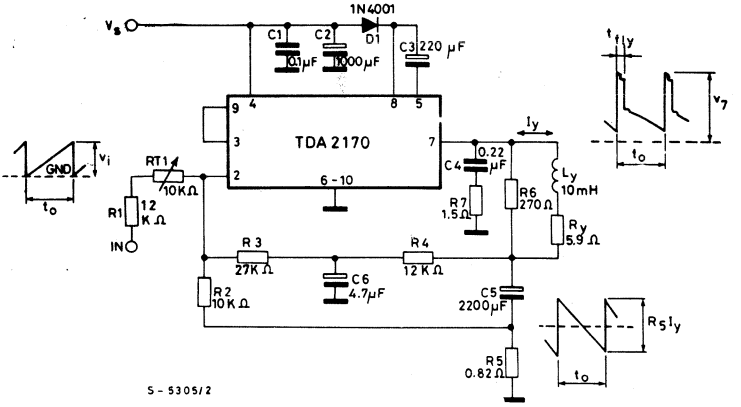
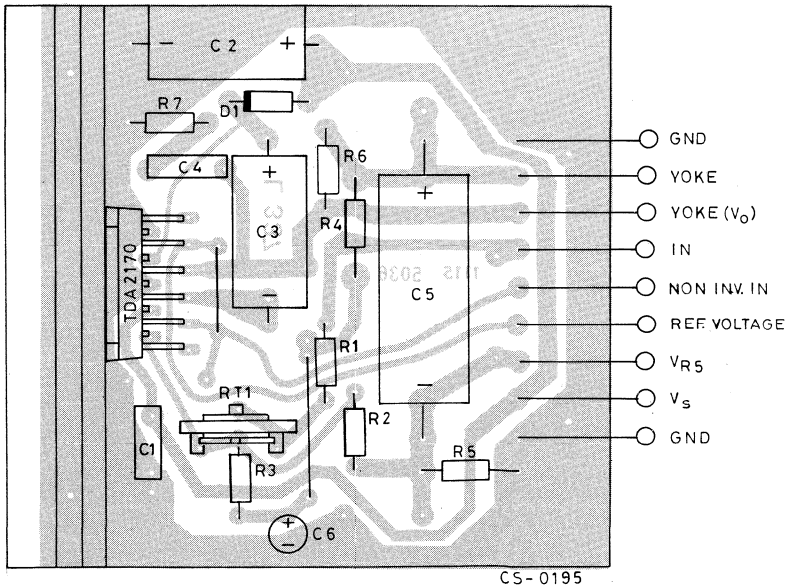



Fig. 3 - PC board and component layout (1:1 scale)



## Components list for typical applications

| Component | 110° TVC 5.9Ω/10 mH 1.95 App | 110° TVC 9.6Ω/24.6 mH 1.2 App | 90° TVC 15Ω/30 mH 0.82 App | Unit |
|---|---|---|---|---|
| RT1 | 10 | 4.7 | 10 | KΩ |
| R1 | 12 | 10 | 12 | KΩ |
| R2 | 10 | 5.6 | 5.6 | KΩ |
| R3 | 27 | 12 | 18 | KΩ |
| R4 | 12 | 8.2 | 5.6 | KΩ |
| R5 | 0.82 | 1 | 1 | Ω |
| R6 | 270 | 330 | 330 | Ω |
| R7 | 1.5 | 1.5 | 1.5 | Ω |
| D1 | 1N 4001 | 1N 4001 | 1N 4001 | – |
| C1 | 0.1 | 0.1 | 0.1 | μF |
| C2 el. | 1000/25V | 470/25V | 470/25V | μF |
| C3 el. | 220/25V | 220/25V | 220/25V | μF |
| C4 | 0.22 | 0.22 | 0.22 | μF |
| C5 el. | 2200/25V | 2200/25V | 1000/16V | μF |
| C6 el. | 4.7/16V | 4.7/16V | 10/16V | μF |

## Typical performances

| Parameter | 110° TVC 5.9Ω/10 mH | 110° TVC 9.6Ω/27 mH | 90° TVC 15Ω/30 mH | Unit |
|---|---|---|---|---|
| $V_s$ – Supply voltage | 24 | 22.5 | 25 | V |
| $I_s$ – Current | 280 | 175 | 125 | mA |
| $t_{fly}$ – Flyback time | 0.6 | 1 | 0.7 | ms |
| * $P_{tot}$ – Power dissip. | 4.2 | 2.5 | 2.05 | W |
| * $R_{th\ c-a}$ – Heatsink | 7 | 13 | 16 | °C/W |
| $T_{amb}$ | 60 | 60 | 60 | °C |
| $T_{j\ max}$ | 110 | 110 | 110 | °C |
| $t_o$ | 20 | 20 | 20 | ms |
| $v_i$ | 2.5 | 2.5 | 2.5 | Vpp |
| $v_7$ | 50 | 47 | 52 | Vp |

* Worst case condition.

## MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the MULTIWATT® package attaching the heatsink is very simple, a screw or a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 4 - Mounting examples

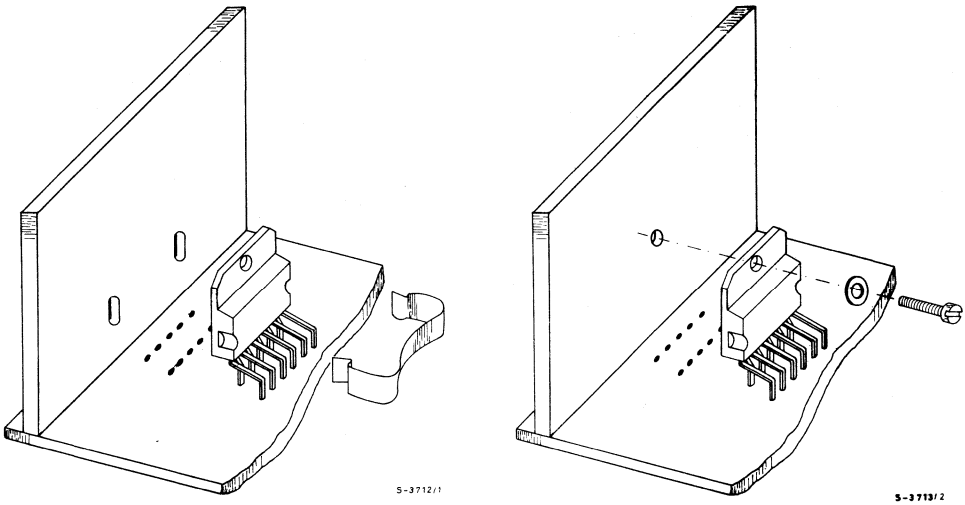
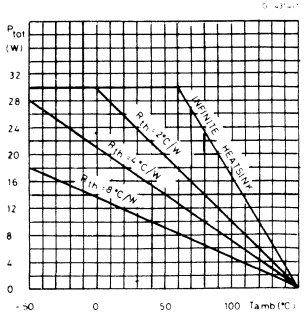



Fig. 5 - Maximum allowable power dissipation vs. ambient temperature



# TDA2220

# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## HIGH PERFORMANCE AM/FM RADIO

- VERY WIDE RANGE OF SUPPLY VOLTAGE 3 to 16V
- HIGH RECOVERED AUDIO SIGNAL (100 mV, $\Delta f = \pm 22.5$ KHz or m = 0.3)
- DESIGNED FOR USE WITH EXTERNAL RATIO DETECTOR; INTERNAL QUADRATURE DETECTOR PROVIDED FOR LOW COST RADIOS
- VERY GOOD AM SIGNAL HANDLING (1V; m = 0.8)
- VERY SIMPLE DC SWITCHING OF AM-FM SECTIONS
- SUITABLE FOR CAPACITANCE, VARICAP AND INDUCTIVE TUNING
- VERY LOW TWEET
- COMMON (AM-FM) FIELD STRENGTH METER OUTPUT PIN
- FIELD STRENGTH METER OUTPUT USEFUL FOR NOISE REDUCTION AND HIGH CUT FUNCTION IN STEREO DECODER
- INDEPENDENT ADJUSTMENT OF FM OUTPUT LEVEL WITH EXTERNAL TRIMMER

The TDA 2220 is a high performance AM/FM radio IC designed for use in a wide range of car radio, portable radio and home radio applications, operating on a supply voltage from 3 to 16V. A special feature of this device is that it may be used with an internal quadrature detector or an external ratio detector. The TDA 2220 is supplied in a 20 pin plastic DIP package.

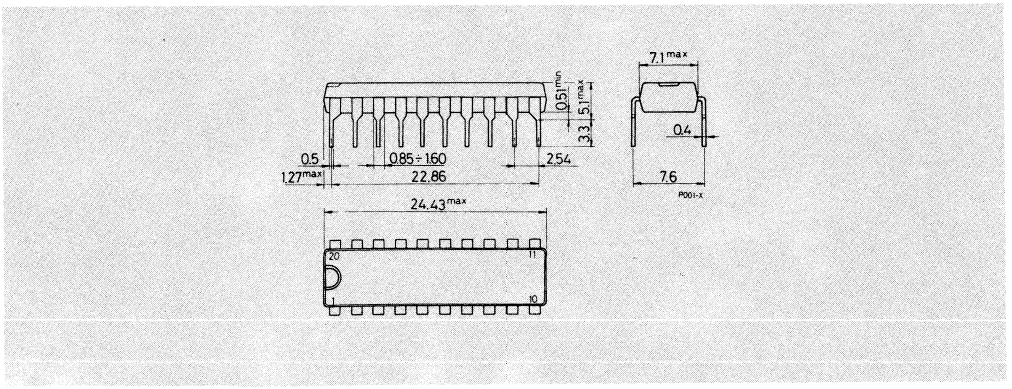
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 16 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 70°C$ | 800 | mW |
| $T_{op}$ | Operating temperature | -40 to 85 | °C |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -55 to 150 | °C |

**ORDERING NUMBER:** TDA 2220

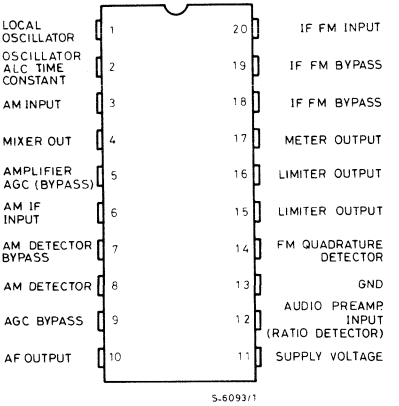
## MECHANICAL DATA

Dimensions in mm

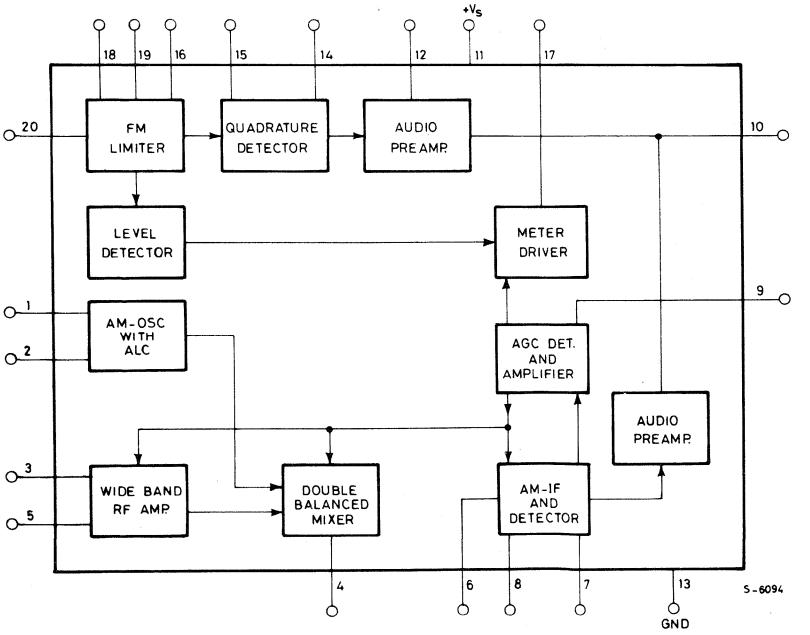


## CONNECTION DIAGRAM

(top view)




## BLOCK DIAGRAM



## THERMAL DATA

| | | |
|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction ambient | max 100 °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $T_{amb}$ = 25°C, $V_s$ = 9V, unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | 3 | 9 | 16 | V |
| $I_d$ | Current drain | AM Section | | 10 | 16 | 21 | mA |
| | | FM Section | | 10 | 14 | 21 | |

**AM SECTION** ($f_o$ = 1MHz; $f_m$ = 1KHz)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_i$ | Input sensitivity | S/N = 26 dB | m = 0.3 | | 12 | 25 | μV |
| $\frac{S+N}{N}$ | Signal to noise ratio | $V_i$ = 10mV | m = 0.3 | 45 | | | dB |
| $V_i$ | AGC range | $\Delta V_{out}$ = 10dB | m = 0.8 | 100 | | | dB |
| $V_o$ | Recovered audio signal (pin 10) | $V_i$ = 1 mV | m = 0.3 | 75 | 120 | 170 | mV |
| d | Distortion | | | | 0.5 | | % |
| d | Distortion | $V_i$ = 1 mV | m = 0.8 | | 2 | 3 | % |
| $V_H$ | Max input signal handling capability | m = 0.8 | d < 10% | 1 | | | V |
| $R_i$ | Input resistance between pins 3 and 5 | m = 0 | | | 7.5 | | KΩ |
| $C_i$ | Input capacitance between pins 3 and 5 | m = 0 | | | 18 | | pF |
| $R_o$ | Output resistance (pin 10) | | | 4.5 | 7 | 9.5 | KΩ |
| | Tweet 2 IF | m = 0.3 | $V_i$ = 1mV | | 38 | | dB |
| | Tweet 3 IF | | | | 55 | | dB |
| $V_m$(*) | Meter output | $V_i$ = 1 mV | m = 0.3 | | 130 | | mV |

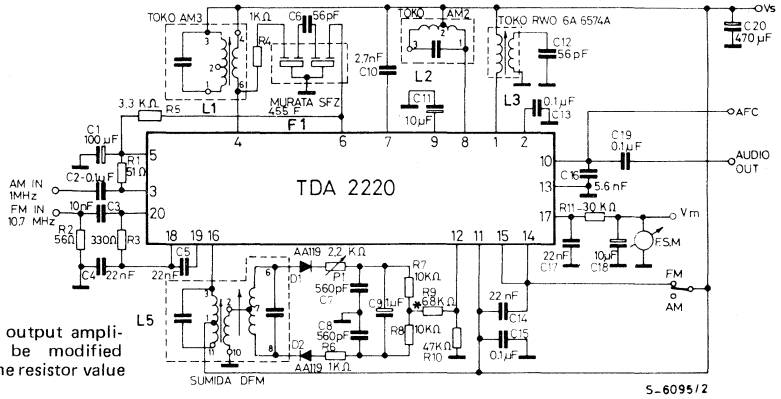
(*) Meter resistance = 1.3 KΩ.

## ELECTRICAL CHARACTERISTICS (Continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **FM SECTION** ($f_o$ = 10.7MHz; $f_m$ = 1KHz) | | | | | | **(RATIO DETECTOR)** |
| $V_i$ | Input limiting voltage | -3 dB limiting point | | 25 | 36 | μV |
| AMR | Amplitude modulation rejection | Δf = ± 22.5KHz m = 0.3<br>$V_i$ = 3mV | 50 | 60 | | dB |
| $\frac{S+N}{N}$ | Signal to noise ratio | Δf = ±22.5KHz $V_i$ = 10mV | 55 | 65 | | dB |
| d | Distortion | Δf = ±75KHz $V_i$ = 1mV | | 0.4 | 0.7 | % |
| d | Distortion | Δf = ±22.5 KHz $V_i$ = 1mV | | 0.2 | | % |
| $V_o$ | Recovered audio signal (pin 10) | Δf = ±22.5KHz $V_i$ = 1mV | 75 | 120 | 170 | mV |
| $R_i$ | Input resistance between pin 20 and ground | Δf = 0 | | 6.5 | | KΩ |
| $C_i$ | Input capacitance between pin 20 and ground | Δf = 0 | | 14 | | pF |
| $R_o$ | Output resistance (pin 10) | | 4.5 | 7 | 9.5 | KΩ |
| $V_m$(*) | Meter output | $V_i$ = 1 mV Δf = ± 22.5 KHz | | 110 | | mV |
| **FM SECTION** ($f_o$ = 10.7MHz, $f_m$ = 1KHz) | | | | | | **(QUADRATURE DETECTOR)** |
| $V_i$ | Input limiting voltage | -3dB limiting point | | 25 | 36 | μV |
| AMR | Amplitude modulation rejection | Δf = ±22.5KHz m = 0.3<br>$V_i$ = 3mV | 35 | 44 | | dB |
| $\frac{S+N}{N}$ | Signal to noise ratio | Δf = ±22.5KHz $V_i$ = 10mV | 55 | 65 | | dB |
| d | Distortion | Δf = ±75KHz $V_i$ = 1mV | | 0.7 | 1.5 | % |
| d | Distortion | Δf = ±22.5KHz $V_i$ = 1mV | | 0.25 | | % |
| d | Distortion (double tuned) | | | 0.1 | | % |
| $V_o$ | Recovered audio signal (pin 10) | Δf = ±22.5KHz $V_i$ = 1mV | 60 | 90 | 130 | mV |
| $R_i$ | Input resistance between pin 20 and ground | Δf = 0 | | 6.5 | | KΩ |
| $C_i$ | Input capacitance between pin 20 and ground | Δf = 0 | | 14 | | pF |
| $R_o$ | Output resistance (pin 10) | | 4.5 | 7 | 9.5 | KΩ |
| $V_m$(*) | Meter output | $V_i$ = 1 mV Δf = ± 22.5 KHz | | 110 | | mV |

(*) Meter resistance = 1.3 KΩ.

Fig. 1 - Test circuit with FM ratio detector




(*) The audio output amplitude can be modified changing the resistor value

Fig. 2 - P.C. board and component layout of the circuit of fig. 1 (1:1 scale)

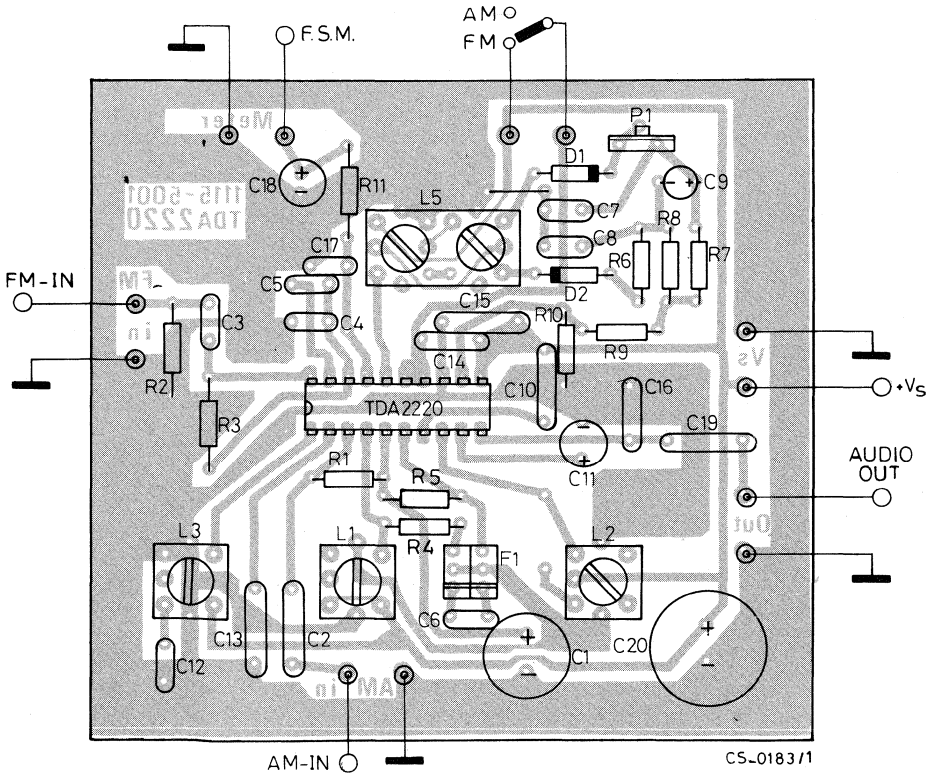


Fig. 3 - Test circuit with FM quadrature detector

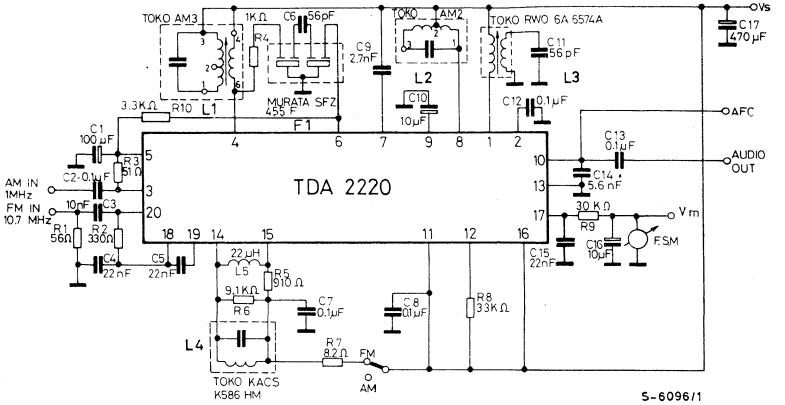
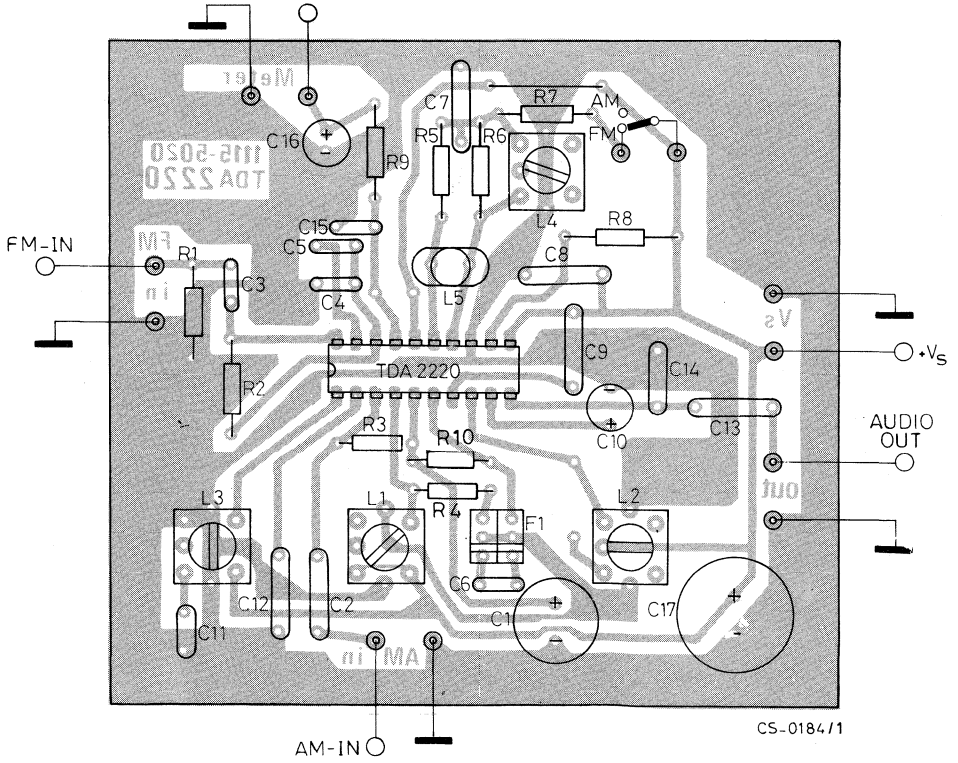
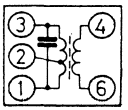



Fig. 4 - P.C. board and component layout of the circuit of fig. 3 (1:1 scale)



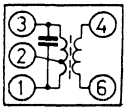
## L1 - 455 kHz IF Coil



| $C_o$(pF) | f (MHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| 1-3 | | 1-3 | 1-2 | 2-3 | 4-6 |
| 180 | 455 | 70 | 57 | 116 | 24 |

TOKO AM3 - 10x10 mm
RLC - 4A7525N

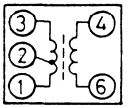
## L2 - AM Detector Coil



| $C_o$(pF) | f (KHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| 1-3 | | 1-3 | 1-2 | 2-3 | 4-6 |
| 180 | 455 | 70 | 173 | 94 | 9 |

TOKO AM2 - 10x10 mm.
RLC - 4A7524EK

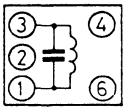
## L3 - AM Oscillator Coil



| f (kHz) | L ($\mu$H) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| | 1-3 | 1-3 | 1-2 | 2-3 | 4-6 |
| 796 | 220 | 80 | 2 | 75 | 8 |

TOKO - 10x10 mm.
RWO - 6A6574N

## L4 - FM Detector Coil

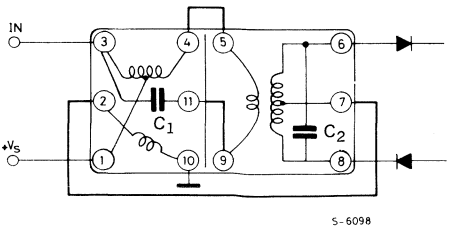


S-6097

| $C_o$(pF) | f (MHz) | $Q_o$ | TURNS | | |
|---|---|---|---|---|---|
| 1-3 | | 1-3 | 1-3 | – | – |
| 82 | 10.7 | 100 | 12 | – | – |

TOKO - 10x10 mm
KACS - K586 HM

## L5 - Ratio Detector




S-6098

| $C_1$(pF) | $C_2$(pF) | f (MHz) | $Q_o$ |
|---|---|---|---|
| 3-11 | 6-8 | | 3-11/4-8 |
| 27 | 47 | 10.7 | 70 |

| TURNS | | | | | |
|---|---|---|---|---|---|
| 1-3 | 1-4 | 2-10 | 5-9 | 6-7 | 7-8 |
| 11 | 6½ | 5½ | ½ | 7 | 7 |

SUMIDA
DFM

## APPLICATION INFORMATION

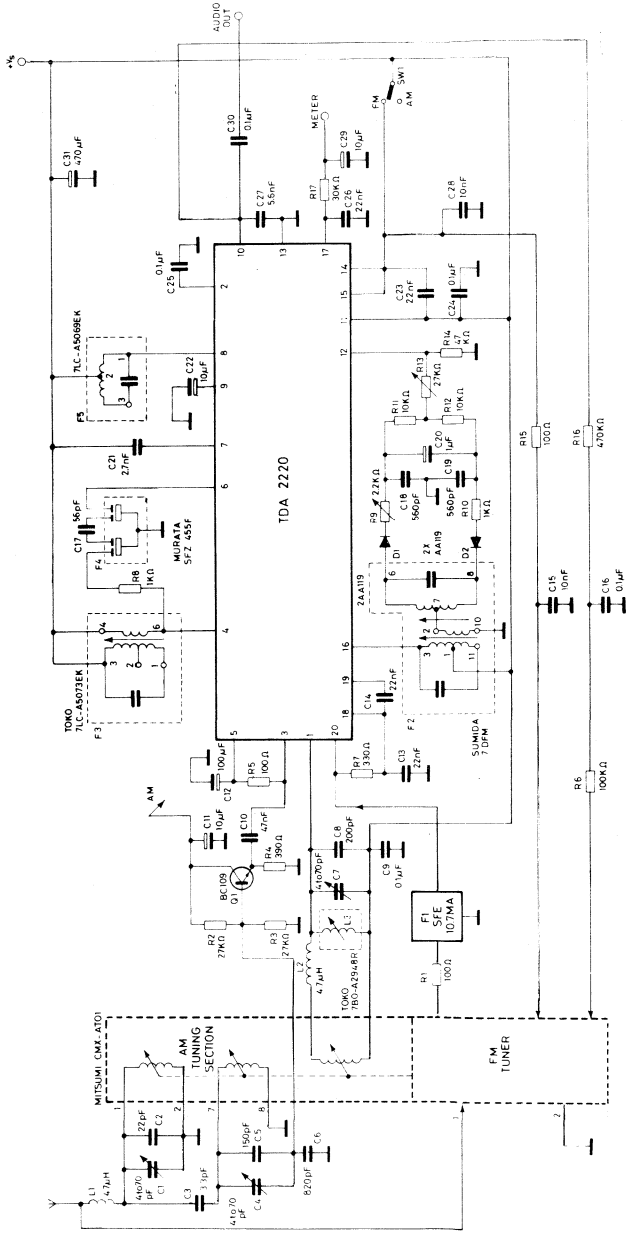



Fig. 5 - AM/FM car radio receiver

Note - The transistor Q1 can be eliminated using the tuner of fig. 7.

Fig. 6 - P.C. board and component layout of the circuit of fig. 5 (1:1 scale)

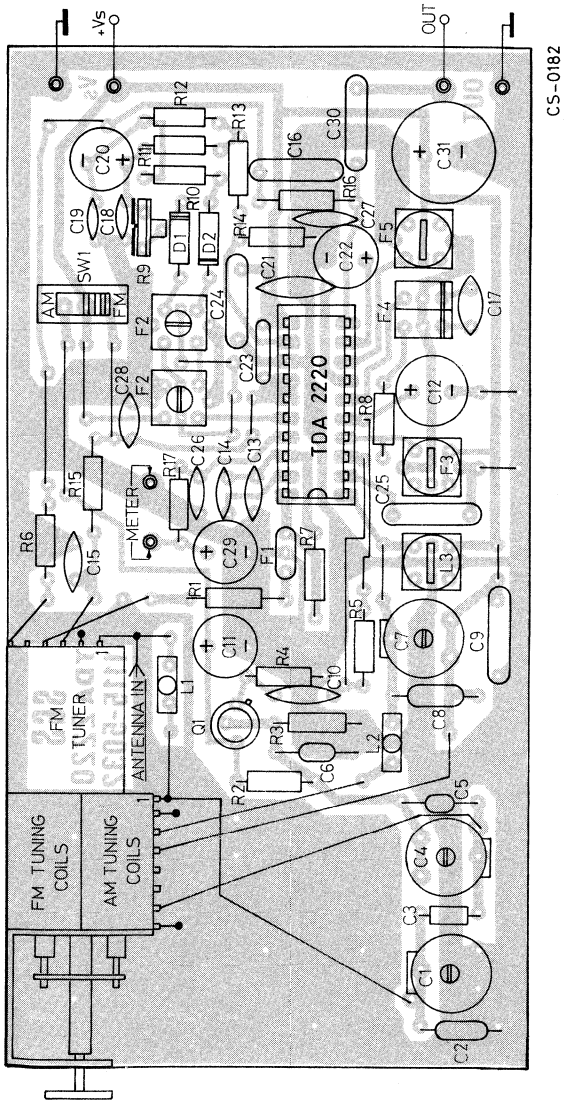
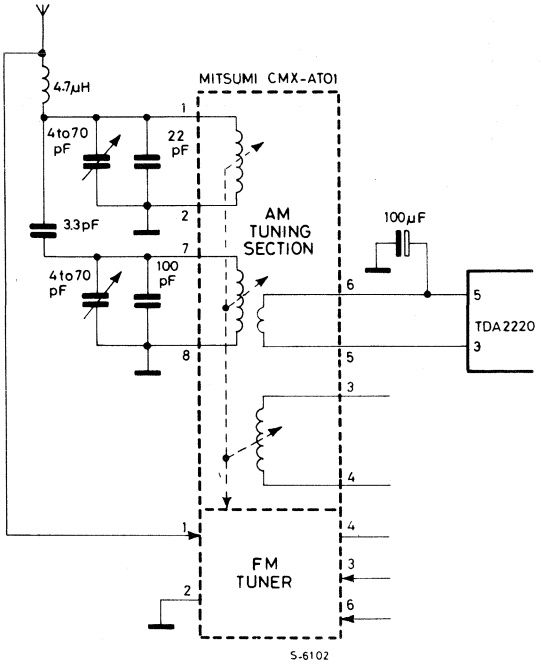
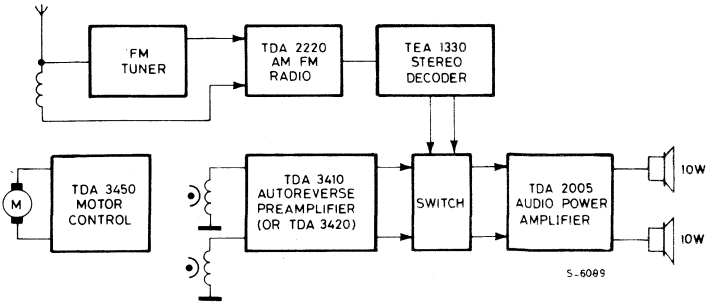


Fig. 7 - Alternative tuner connection for the car radio of fig. 5




## APPLICATION SUGGESTION

Fig. 8 - Car radio with cassette player



# TDA2270

# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## TV VERTICAL DEFLECTION OUTPUT CIRCUIT

- DRIVES VERTICAL DEFLECTION WINDINGS DIRECTLY
- HIGH EFFICIENCY
- INTERNAL FLYBACK GENERATOR
- THERMAL PROTECTION
- ON-CHIP VOLTAGE REFERENCE
- HIGH OUTPUT CURRENT (2.2A PEAK)
- 16-LEAD POWERDIP PLASTIC PACKAGE

The TDA 2270 is a high efficiency monolithic output stage for vertical deflection circuits in TVs and monitors. Driving the vertical windings directly, the device contains a power amplifier, flyback generator, voltage reference and thermal protection circuit.
The TDA 2270 is supplied in a 16-pin DIP with the four center pins connected together and used for heatsinking.

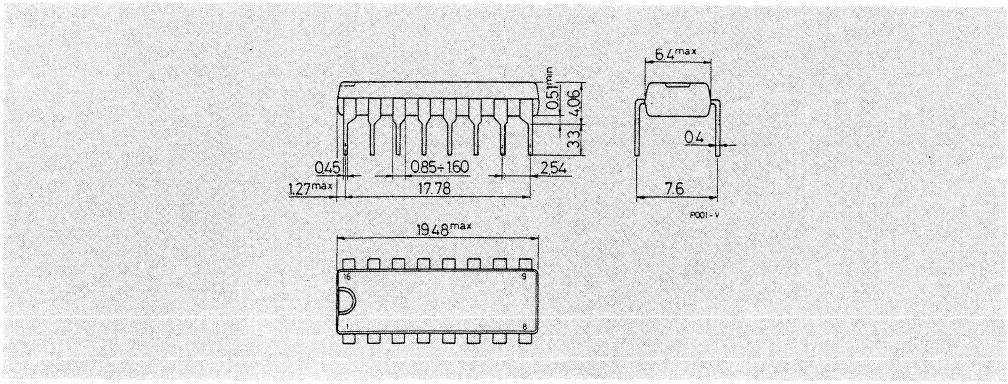
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 1) | 35 | V |
| $V_7$, $V_8$ | Flyback peak voltage | 60 | V |
| $V_2$ | Voltage at pin 2 | $+ V_s$ | |
| $V_{15}$, $V_{16}$ | Amplifier input voltage | $+ V_s$ | |
| | | $- 0.5$ | V |
| $I_o$ | Output peak current (non repetitive, t = 2 ms) | 2 | A |
| $I_o$ | Output peak current at f = 50 Hz, $t \leqslant 10\ \mu s$ | 2.2 | A |
| $I_o$ | Output peak current at f = 50 Hz, $t > 10\ \mu s$ | 1.2 | A |
| $I_2$ | Pin 2 DC current at $V_7 < V_1$ | 50 | mA |
| $I_2$ | Pin 2 peak to peak flyback current at f = 50 Hz, $t_{fly} \leqslant 1.5$ ms | 2 | A |
| $P_{tot}$ | Total power dissipation at $T_{pins} \leqslant 90°C$ | 4.3 | W |
| | $T_{amb} = 70°C$ | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA 2270

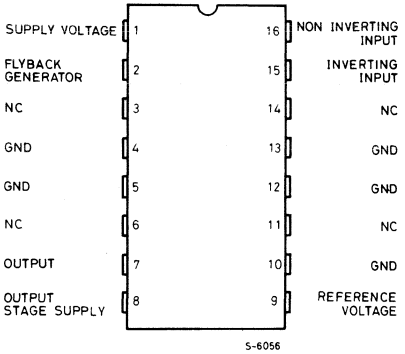
## MECHANICAL DATA

Dimensions in mm

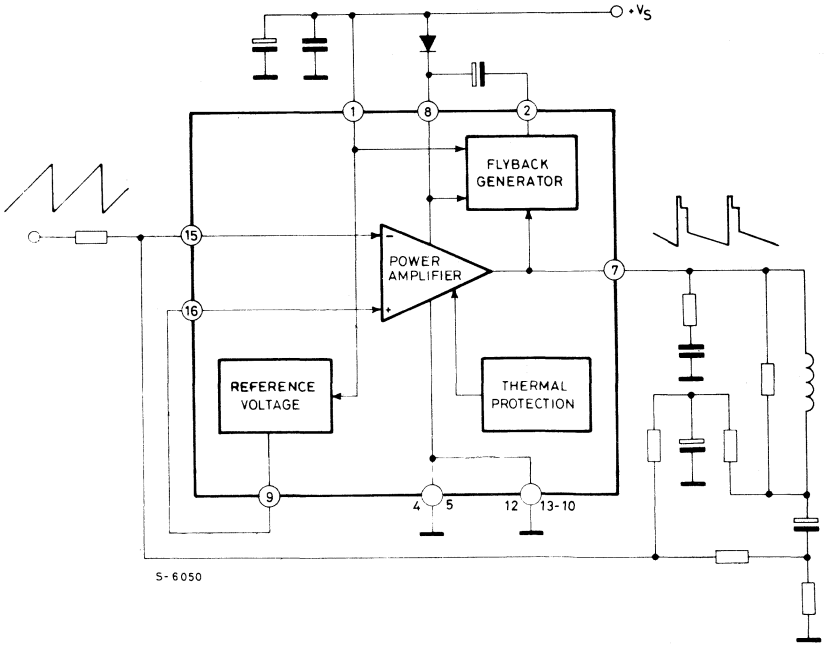


## CONNECTION DIAGRAM

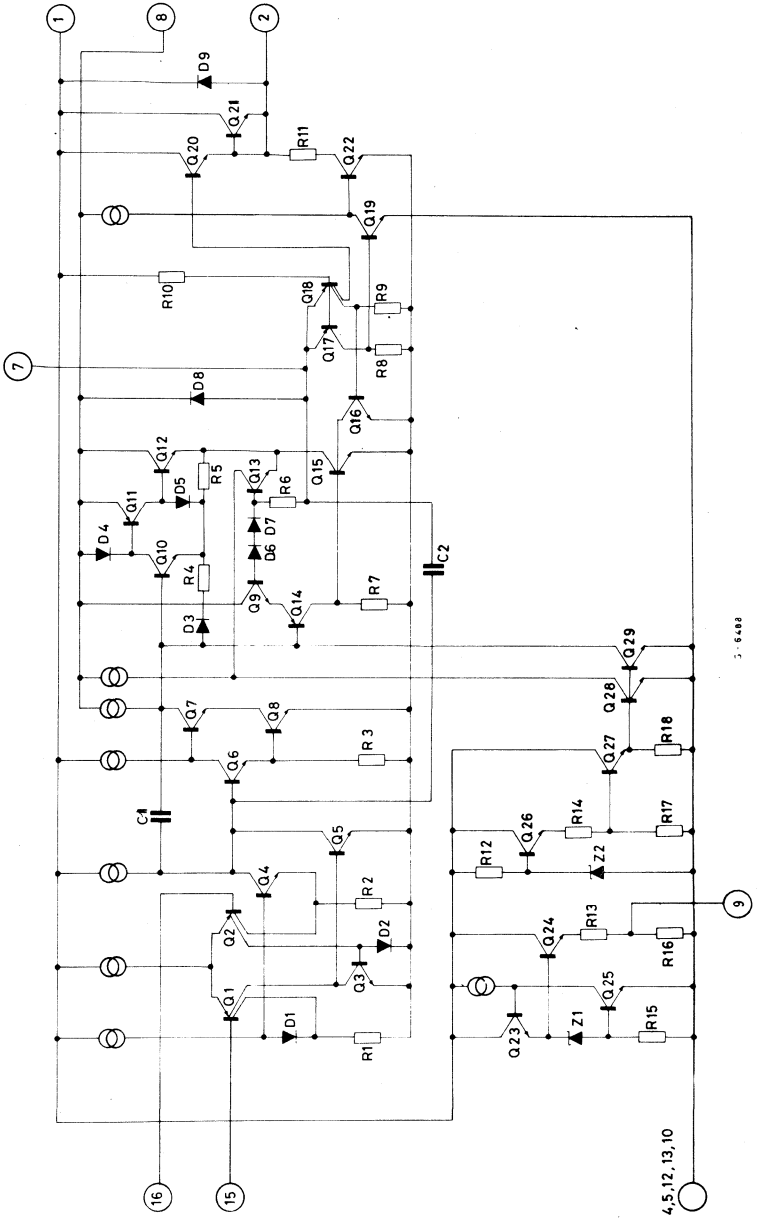
(top view)




## BLOCK DIAGRAM



## SCHEMATIC DIAGRAM



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 14 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 80 | °C/W |

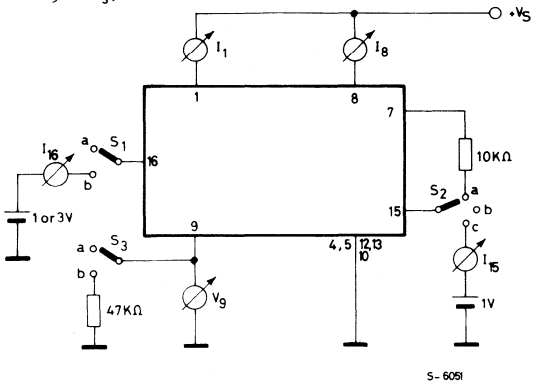
* Obtained with the GND pins soldered to printed circuit with minimized copper area.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_s$ = 35V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| $I_1$ | Pin 1 quiescent current | $I_2 = 0$; $I_7 = 0$; $V_{16} = 3V$ | | 8 | 16 | mA | 1a |
| $I_8$ | Pin 8 quiescent current | $I_2 = 0$; $I_7 = 0$; $V_{16} = 3V$ | | 16 | 36 | mA | 1a |
| $I_{15}$ | Amplifier input bias current | $V_{15} = 1V$ | | -0.1 | -1 | μA | 1a |
| $I_{16}$ | Amplifier input bias current | $V_{16} = 1V$ | | -0.1 | -1 | μA | 1a |
| $V_{2L}$ | Pin 2 saturation voltage to GND | $I_2 = 20$ mA | | 1 | | V | 1c |
| $V_7$ | Quiescent output voltage | $V_s = 35V$; $R_a = 39$ KΩ | | 18 | | V | 1d |
| | | $V_s = 15V$; $R_a = 13$ KΩ | | 7.5 | | V | 1d |
| $V_{7L}$ | Output saturation voltage to GND | $I_7 = 0.7A$ | | 0.7 | 1 | V | 1c |
| $V_{7H}$ | Output saturation voltage to supply | $-I_7 = 0.7A$ | | 1.3 | 1.8 | V | 1b |
| $V_9$ | Reference voltage | $I_9 = 0$ | | 2.2 | | V | 1a |
| $\frac{\Delta V_9}{\Delta V_s}$ | Reference voltage drift vs. supply voltage | $V_s$ = 15 to 30V | | 1 | 2 | mV/V | 1a |
| R9 | Reference voltage output resistance | | | 2.1 | | KΩ | |
| $T_j$ | Junction temperature for thermal shut down | | | 140 | | °C | |

Fig. 1 - DC test circuits

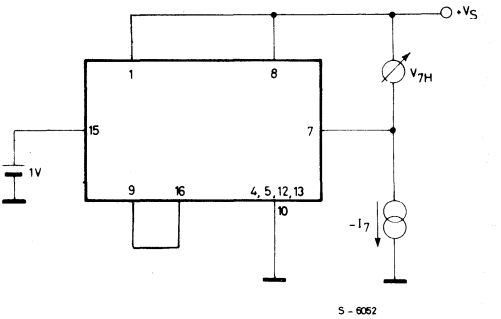
Fig. 1a - Measurement of $I_1$; $I_8$; $I_{15}$; $I_{16}$; $V_9$; $\Delta V_9/\Delta V_s$; R9




S-6051

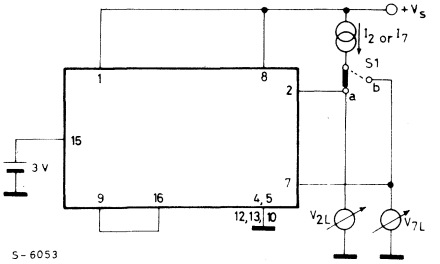
$S_1$ : (a) $I_{15}$; (b) $I_{16}$, $I_7$ and $I_8$.
$S_2$ : (a) $I_7$ and $I_8$; (b) $I_{16}$, (c) $I_{15}$.
$S_3$ : (a) $I_{15}$, $I_{16}$, $I_7$, $I_8$, $I_9$ and $V_9$; (b) R9.

Fig. 1b - Measurement of $V7_H$




S-6052

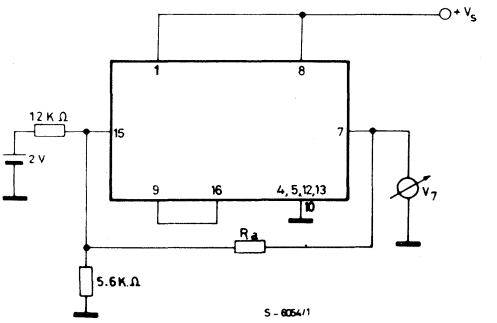
Fig. 1c - Measurement of $V_{2L}$; $V_{7L}$




S-6053

S1 : (a) $V_{2L}$; (b) $V_{7L}$.

Fig. 1d - Measurement of $V_7$




S-6054/1

Fig. 2 - Application circuit

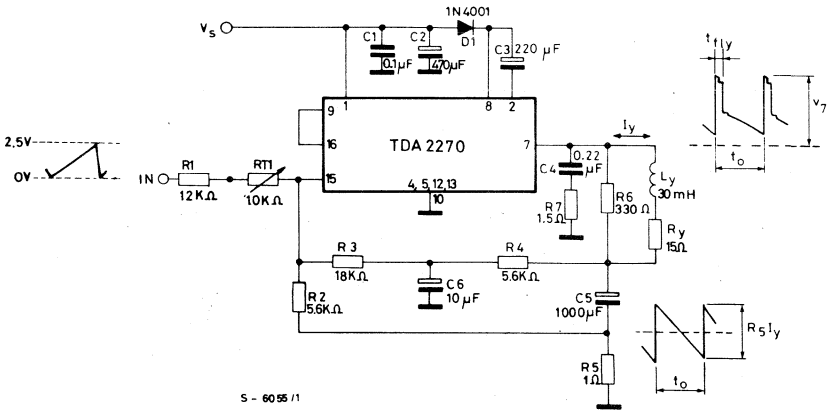
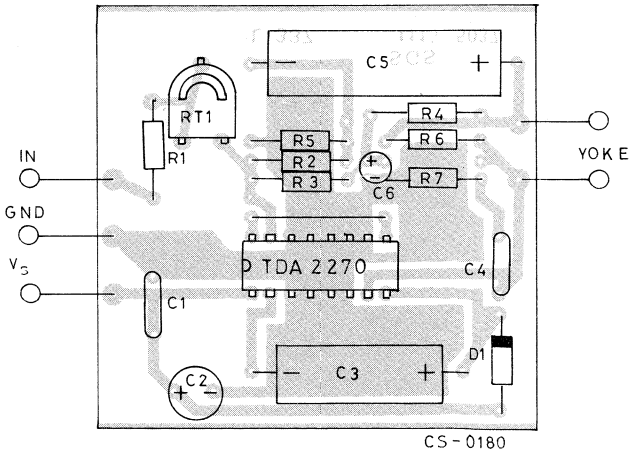



Fig. 3 - PC board and component layout (1:1 scale)



## Components list for typical applications (refer to fig. 2)

| Component | B/W TV 10Ω/20mH/1 App | 90° TVC 15Ω/30 mH 0.82 App | Unit |
|---|---|---|---|
| RT1 | 10 | 10 | KΩ |
| R1 | 10 | 12 | KΩ |
| R2 | 5.6 | 5.6 | KΩ |
| R3 | 15 | 18 | KΩ |
| R4 | 6.8 | 5.6 | KΩ |
| R5 | 1 | 1 | Ω |
| R6 | 330 | 330 | Ω |
| R7 | 1.5 | 1.5 | Ω |
| D1 | 1N 4001 | 1N 4001 | – |
| C1 | 0.1 | 0.1 | μF |
| C2 el. | 470/25V | 470/25V | μF |
| C3 el. | 220/25V | 220/25V | μF |
| C4 | 0.22 | 0.22 | μF |
| C5 el. | 1000/25V | 1000/16V | μF |
| C6 el. | 10/16V | 10/16V | μF |

## Typical performance

| Parameter | B/W TV 10Ω/20mH/1 App | 90° TVC 15Ω/30 mH | Unit |
|---|---|---|---|
| $V_s$ – Supply voltage | 20 | 25 | V |
| $I_s$ – Current | 145 | 125 | mA |
| $t_{fly}$ – Flyback time | 0.75 | 0.7 | ms |
| * $P_{tot}$ – Power dissipation | 1.8 | 2.05 | W |
| * $R_{th\ c-a}$ – Heatsink | 14 | 12 | °C/W |
| $T_{amb}$ | 60 | 60 | °C |
| $T_{j\ max}$ | 130 | 130 | °C |
| $t_o$ | 20 | 20 | ms |
| $v_i$ | 2.5 | 2.5 | Vpp |
| $v_7$ – Flyback voltage | 42 | 52 | Vp |

* Worst case condition.

## MOUNTING INSTRUCTIONS

The $R_{th\ j\text{-}amb}$ of the TDA 2270 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 4) or to an external heatsink (Fig. 5).
The diagram of figure 6 shows the maximum dissipable power $P_{tot}$ and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 4 - Example of P.C. board copper area which is used as heatsink.

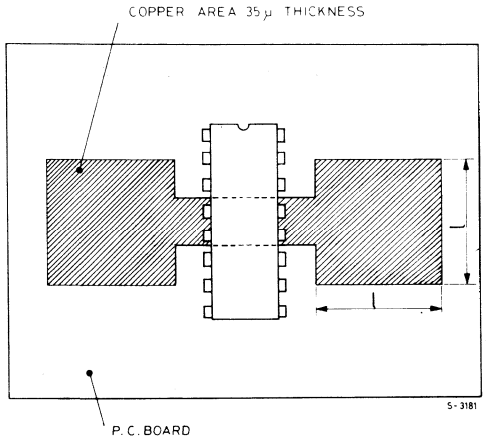



Fig. 5 - External heatsink mounting example

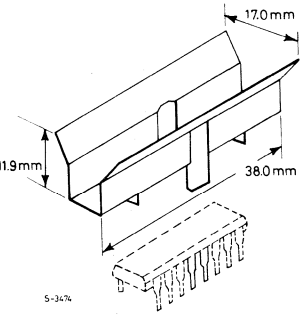



Fig. 6 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

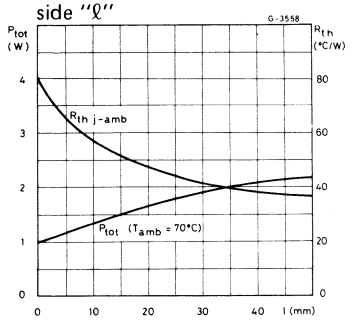
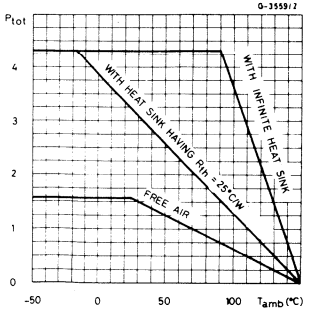



Fig. 7 - Maximum allowable power dissipation vs. ambient temperature



# TDA2320

# LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

## PREAMPLIFIER FOR INFRARED REMOTE CONTROL SYSTEMS

The TDA 2320 is a monolithic integrated circuit in Minidip package specially designed to amplify the IR signal in remote controlled TV or radio sets. It directly interfaces with the digital control circuitry.
The TDA 2320 incorporates a two stages amplifier with excellent sensitivity and high noise immunity. It can work with a single 5V supply voltage and flash or carrier transmission modes as provided for example by the M709/M710C/MOS transmitter.
The TDA 2320 is particularly intended to be used in conjunction with the M104 and M206 + M3870 remote control receivers.

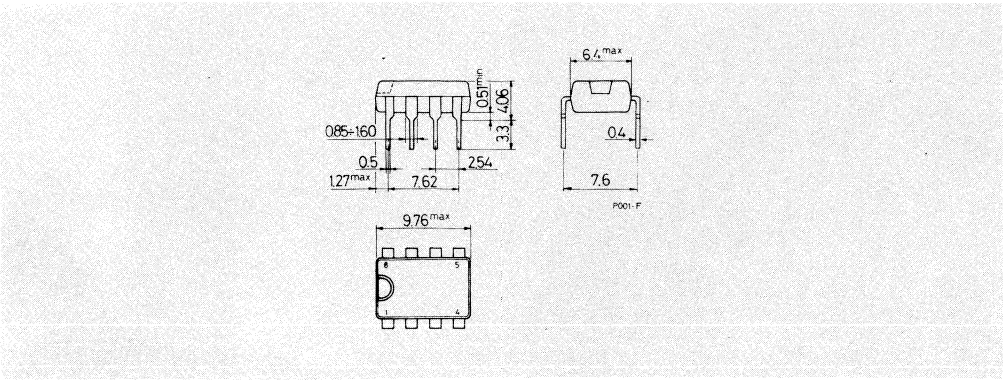
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 20 | V |
| $T_{stg,\ j}$ | Storage and Junction temperature | -40 to 150 | °C |
| $P_{tot}$ | Total power dissipation at $T_{amb}$ = 70°C | 400 | mW |

**ORDERING NUMBER:** TDA 2320

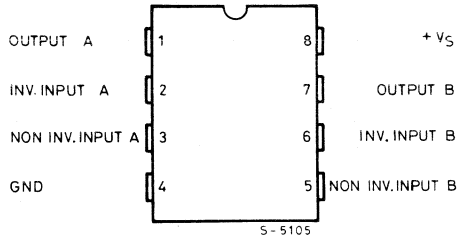
## MECHANICAL DATA

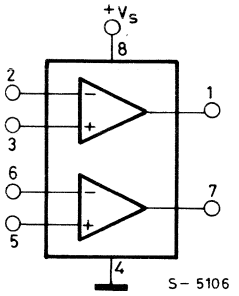
Dimensions in mm



## CONNECTION AND BLOCK DIAGRAM

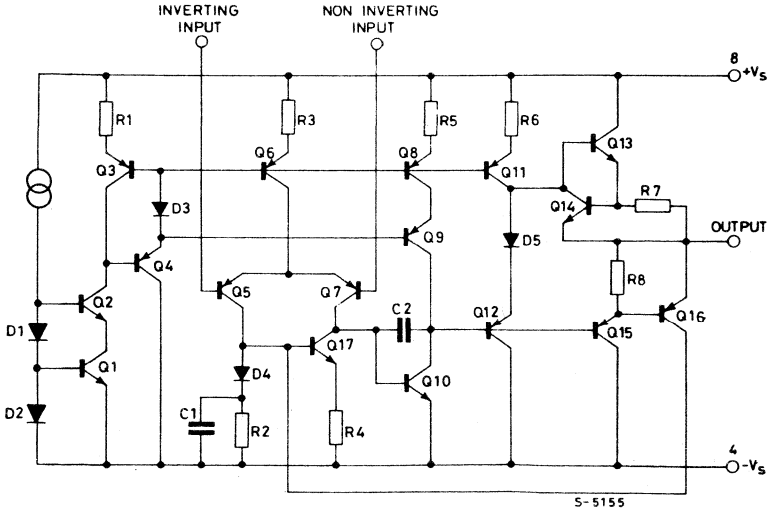
(top view)




## SCHEMATIC DIAGRAM

(one section)




## THERMAL DATA

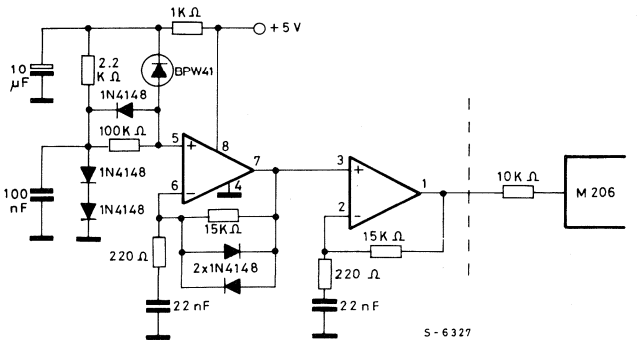
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 200 | °C/W |

## ELECTRICAL CHARACTERISTICS ($V_s$= 5V, $T_{amb}$= 25°C, single amplifier, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 4 | | 20 | V |
| $I_s$ | Total supply current | $V_s$ = 20V | | 0.8 | 2 | mA |
| $I_b$ | Input bias current | | | 100 | 500 | nA |
| $V_{os}$ | Input offset voltage | $R_g$ < 10 KΩ | | 0.5 | | mV |
| $I_{os}$ | Input offset current | | | 15 | | nA |
| $G_v$ | Open loop voltage gain | f = 1 KHz | 64 | 70 | | dB |
| | | f = 100 KHz | | 30 | | dB |
| B | Gain bandwidth product | f = 40 KHz | 1.5 | 3 | | MHz |
| SR | Slew rate | $R_L$= 2 KΩ | | 1.5 | | V/μs |
| $e_N$ | Total input noise voltage | f = 40 KHz<br>Rg= 10KΩ | | 20 | | $nV/\sqrt{Hz}$ |
| $V_o$. | DC output voltage swing | | | 2.5 | | Vpp |
| SVR | Supply voltage rejection | f = 100 Hz | | 80 | | dB |

## APPLICATION INFORMATION

Fig. 1 - Application circuit for carrier transmission mode



## APPLICATION INFORMATION (continued)

Fig. 2 - Flash mode preamplifier

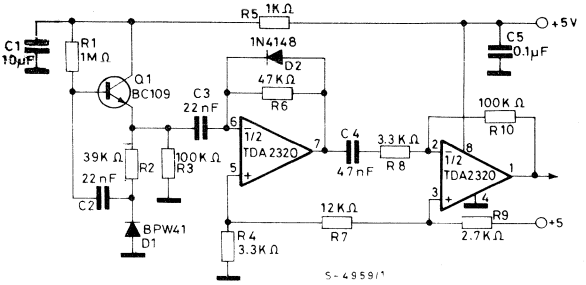



Fig. 3 - P.C. and components layout of the circuit of fig. 2 (1 : 1 scale)

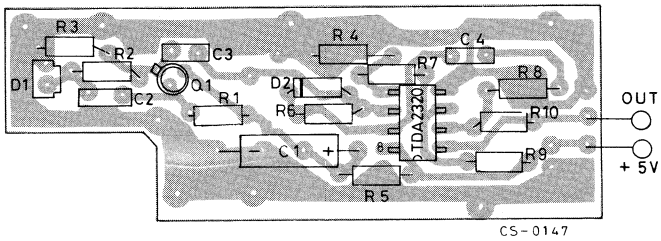



Fig. 4 - IR transmitter using M709 or M710

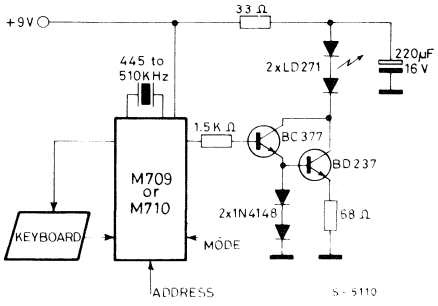
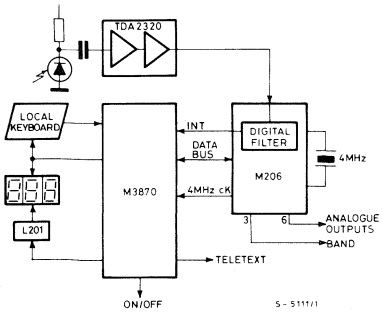
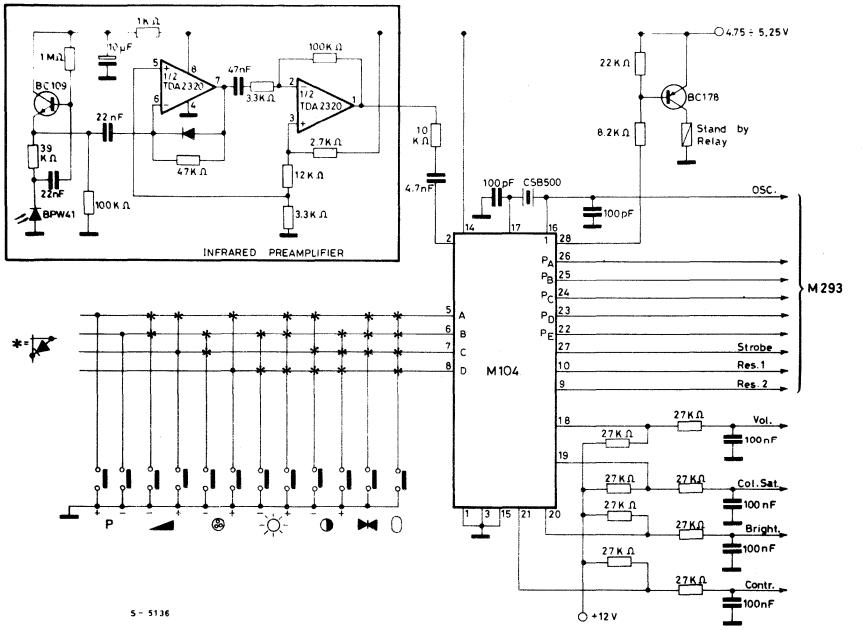



Fig. 5 - MMC II - PLL TV Frequency synthesizer



## APPLICATION INFORMATION (continued)

Fig. 6 - IR Preamplifier and Remote Control receiver for 32 channel voltage synthesizer (EPM - M293)



# LINEAR INTEGRATED CIRCUITS

**TDA2320A**

## MINIDIP STEREO PREAMPLIFIER

The TDA 2320A is a stereo class A preamplifier intended for application in portable cassette players and high quality audio systems.
The TDA 2320A is a monolithic integrated circuit in a 8 lead minidip which features:

- Wide supply voltage range (3 to 36V)
- Single or split supply operation
- Very low current consumption (0.8 mA)
- Very low distortion
- No pop-noise
- Short circuit protection

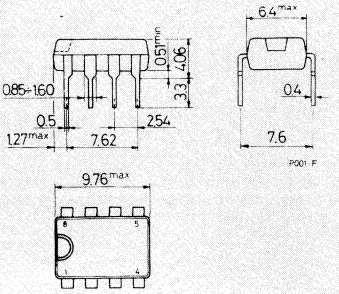
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 36 | V |
| $P_{tot}$. | Total power dissipation at $T_{amb} = 70°C$ | 400 | mW |
| $T_{stg}$, j | Storage and junction temperature | -40 to 150 | °C |

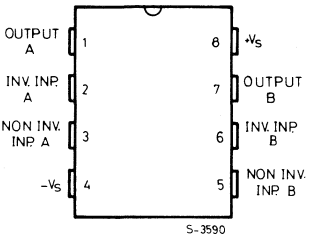
**ORDERING NUMBER:** TDA 2320A

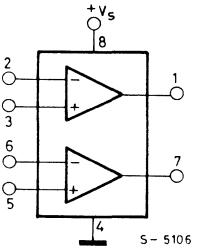
## MECHANICAL DATA

Dimensions in mm

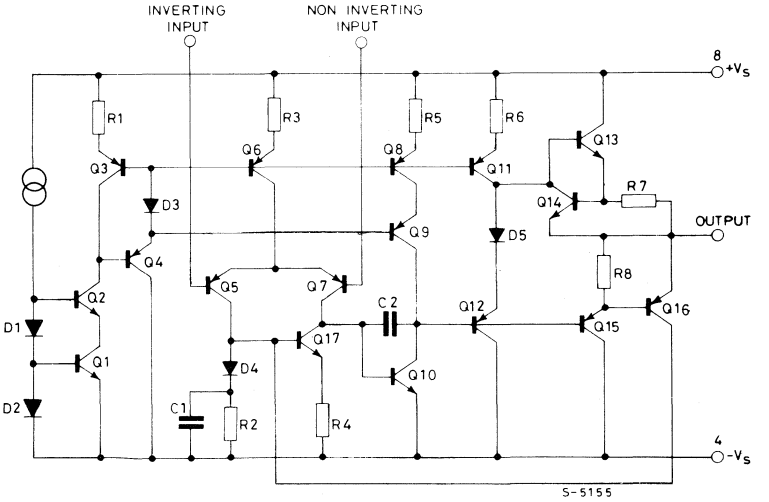


## CONNECTION AND BLOCK DIAGRAM
(top view)




## SCHEMATIC DIAGRAM
(one section)



## TEST CIRCUITS

Fig. 1

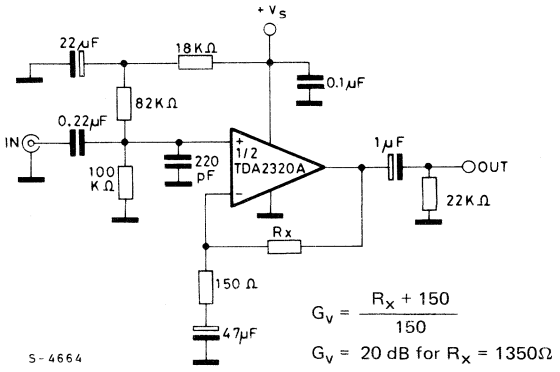
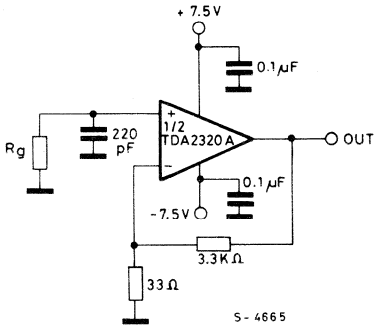



Fig. 2



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 200 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_s$ = 15V, $T_{amb}$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage (*) | | | 3 | | 36 | V |
| $I_s$ | Supply current (*) | | | | 0.8 | 2 | mA |
| $I_b$ | Input bias current | | | | 150 | 500 | nA |
| $V_{os}$ | Input offset voltage | $R_g$ < 10 KΩ | | | 0.5 | 5 | mV |
| $I_{os}$ | Input offset current | | | | 10 | 50 | nA |
| $G_v$ | Open loop voltage gain | $V_s$ = 15V | f = 333 Hz | | 80 | | dB |
| | | | f = 1 KHz | | 70 | | |
| | | | f = 10 KHz | | 50 | | |
| | | $V_s$ = 4.5V | f = 1 KHz | | 70 | | |
| $V_o$ | Output voltage swing (*) | f = 1 KHz | $V_s$= 15V | | 13 | | Vpp |
| | | $R_L$= 600Ω | $V_s$= 4.5V | | 2.5 | | |
| B | Gain-bandwidth product | f = 20 KHz | | 1.5 | 2.5 | | MHz |
| BW | Power bandwidth (*) | $V_o$= 5 Vpp d = 1% | | 40 | 70 | | KHz |
| SR | Slew rate (*) | | | 1 | 1.6 | | V/μS |
| d | Distortion (*) | $V_o$= 2V | f = 1 KHz | | 0.03 | | % |
| | | $G_v$= 20 dB | f = 10 KHz | | 0.08 | | |
| $e_N$ | Total input noise voltage (**) | Curve A | $R_g$= 50Ω | | 1 | | μV |
| | | | $R_g$= 600Ω | | 1.1 | 1.4 | |
| | | | $R_g$= 5 KΩ | | 1.5 | | |
| | | B = 22 Hz to 22 KHz | $R_g$= 50Ω | | 1.3 | | μV |
| | | | $R_g$= 600Ω | | 1.5 | | |
| | | | $R_g$= 5 KΩ | | 2 | | |
| | | f = 1 KHz | $R_g$= 600Ω | | 9 | | nV/√Hz |
| Cs | Channel separation (**) | | f = 1 KHz | | 100 | | dB |
| SVR | Supply voltage (**) rejection | | f = 100 Hz | | 80 | | dB |

(*) Test circuit of fig. 1.
(**) Test circuit of fig. 2.

Fig. 3 - Supply current vs. supply voltage

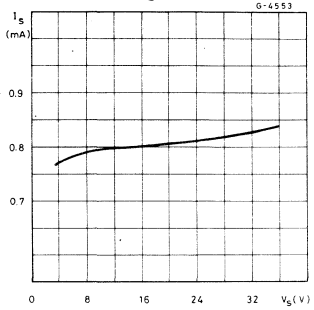



Fig. 4 - Supply current vs. ambient temperature

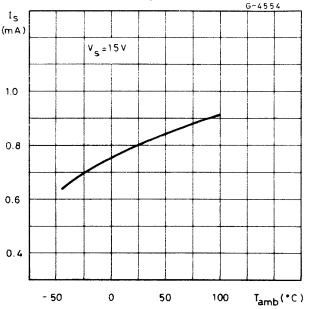



Fig. 5 - Output voltage swing vs. load resistance

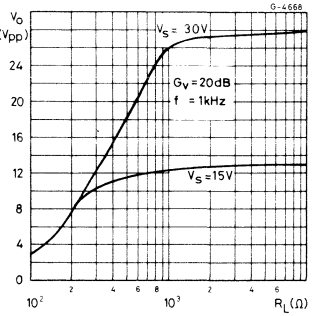



Fig. 6 - Power bandwidth

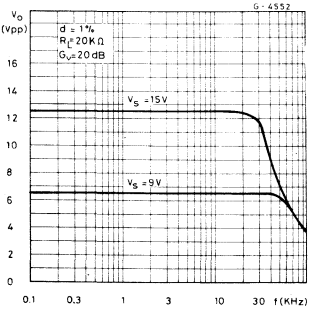



Fig. 7 - Total harmonic distortion vs. output voltage

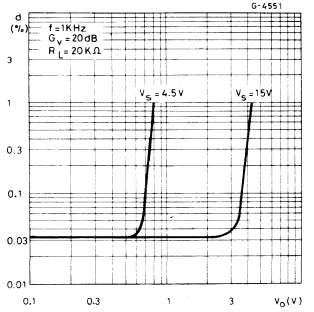



Fig. 8 - Total input noise vs. source resistance

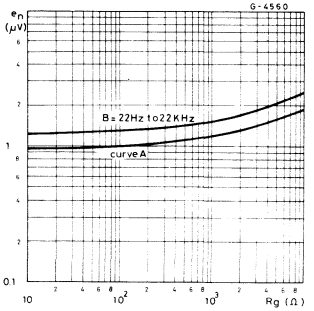



Fig. 9 - Noise density vs. frequency

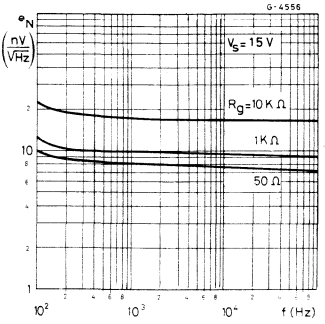



Fig. 10 - RIAA preamplifier response (circuit of fig. 12)

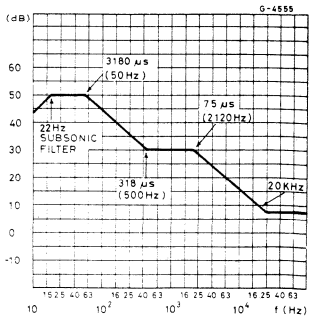
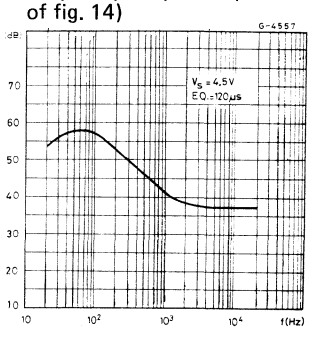



Fig. 11 - Tape preamplifier frequency response (circuit of fig. 14)



## APPLICATION INFORMATION

Fig. 12 - Stereo RIAA preamplifier

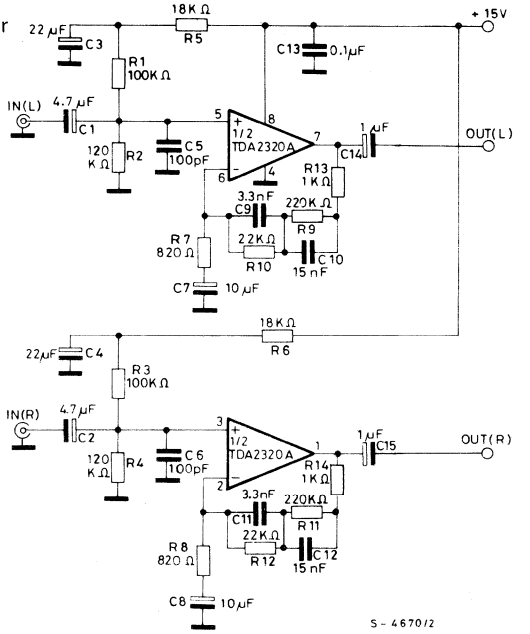
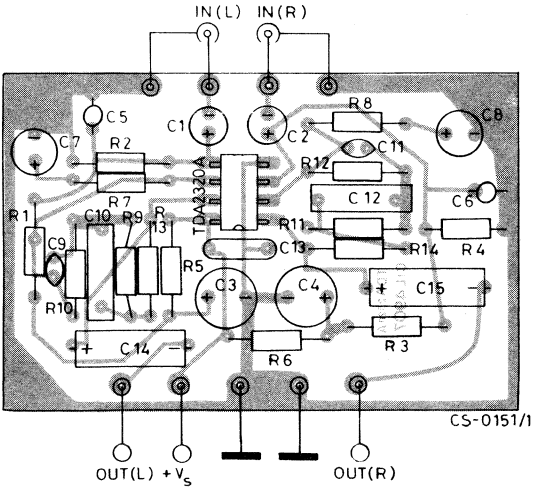



Fig. 13 - P.C. board and components layout of the circuit of fig. 12



## APPLICATION INFORMATION (continued)

Fig. 14 - Stereo preamplifier for Walkman cassette players

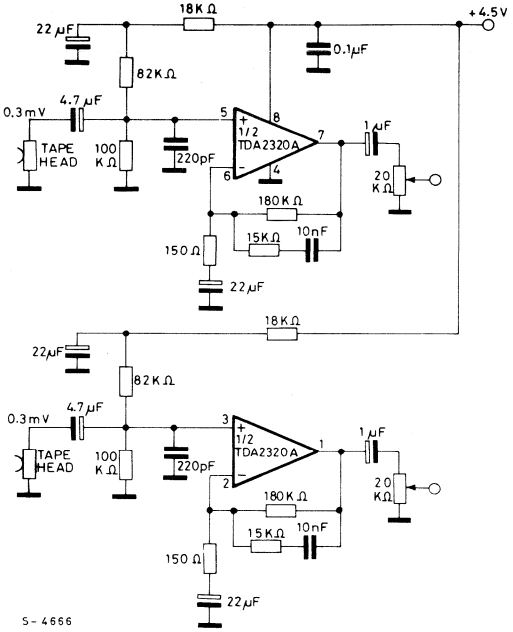



Fig. 15 - Second order 2 KHz Butterworth crossover filter for Hi-Fi active boxes

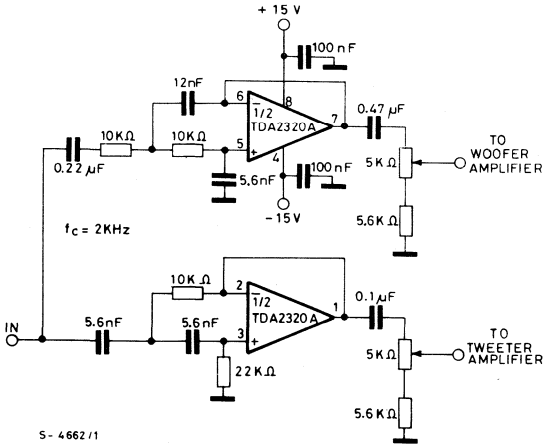
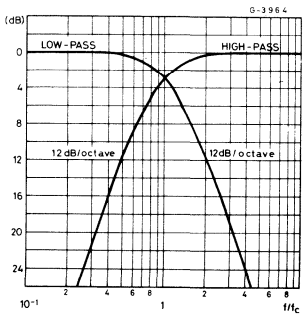



Fig. 16 - Frequency response (circuit of fig. 15)



## APPLICATION INFORMATION (continued)

Fig. 17 - Third order 2.8 KHz Bessel crossover filter for Hi-Fi active boxes

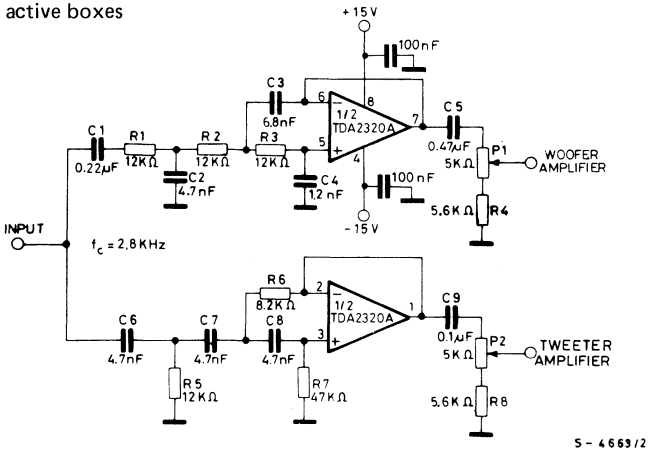



Fig. 18 - Frequency response (circuit of fig. 17)

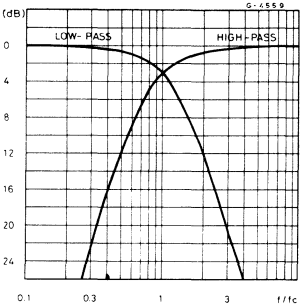



Fig. 19 - 200 Hz to 2 KHz Active Bandpass Filter for midrange speakers

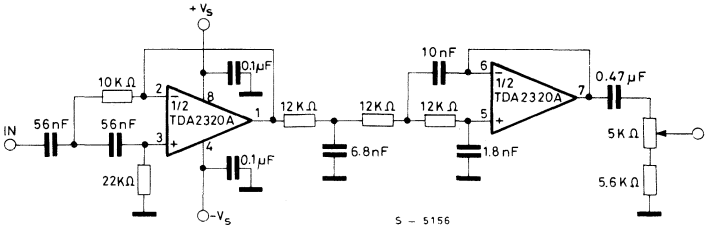
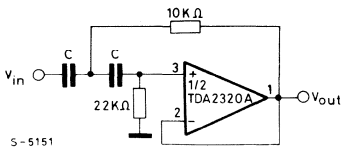
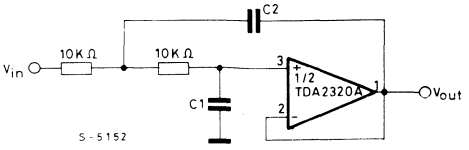



Fig. 20 - Subsonic or rumble filter




| $f_c$ (Hz) | C (μF) |
|---|---|
| 15 | 0.68 |
| 22 | 0.47 |
| 30 | 0.33 |
| 55 | 0.22 |
| 100 | 0.1 |

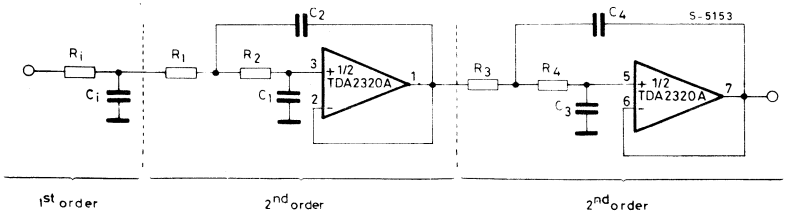
Fig. 21 - High-cut filter




| $f_c$ (KHz) | C1 (nF) | C2 (nF) |
|---|---|---|
| 3 | 3.9 | 6.8 |
| 5 | 2.2 | 4.7 |
| 10 | 1.2 | 2.2 |
| 15 | 0.68 | 1.5 |

## APPLICATION INFORMATION (continued)

Fig. 22 - Fifth order 3.4 KHz low-pass Butterworth filter




For $f_c = 3.4$ KHz and $R_i = R1 = R2 = R3 = R4 = 10$ KΩ, we obtain:

$$C1 = 1.354 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 6.33 \text{ nF}$$

$$C1 = 0.421 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.97 \text{ nF}$$

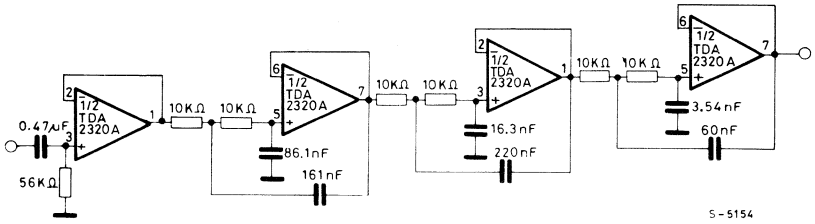
$$C2 = 1.753 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 8.20 \text{ nF}$$

$$C3 = 0.309 \cdot \frac{1}{R} \cdot \frac{1}{2\pi f_c} = 1.45 \text{ nF}$$

$$C4 = 3.325 \cdot \frac{1}{R} \cdot \frac{1}{2,\pi f_c} = 15.14 \text{ nF}$$

The attenuation of the filter is 30 dB at 6.8 KHz and better than 60 dB at 15 KHz.

Fig. 23 - Sixth-pole 355 Hz low-pass filter (Chebychev type)




This is a 6- pole Chebychev type with ± 0.25 dB ripple in the passband. A decoupling stage is used to avoid the influence of the input impedance on the filter's characteristics. The attenuation is about 55 dB at 710 Hz and reaches 80dB at 1065 Hz. The in band attenuation is limited in practice to the ± 0.25 dB ripple and does not exceed 1/2 dB at 0.9 fc.

## APPLICATION INFORMATION (continued)

Fig. 24 - Three band tone control

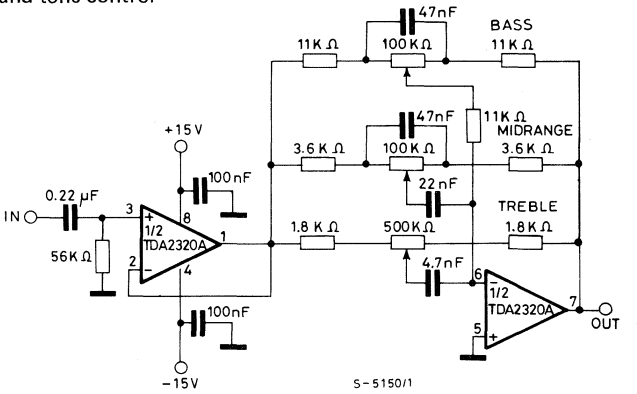
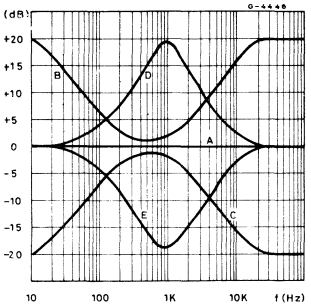



Fig. 25 - Frequency response of the circuit of fig. 24.




A : all controls flat
B : bass & treble boost, mid flat
C : bass & treble cut, mid flat
D : mid boost, bass & treble flat
E : mid cut, bass & treble flat

# LINEAR INTEGRATED CIRCUITS

**TDA2822**

ADVANCE DATA

## DUAL POWER AMPLIFIER

- SUPPLY VOLTAGE DOWN TO 3V
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

The TDA 2822 is a monolithic integrated circuit in 12+2+2 powerdip, intended for use as dual audio power amplifier in portable radios and TV sets.

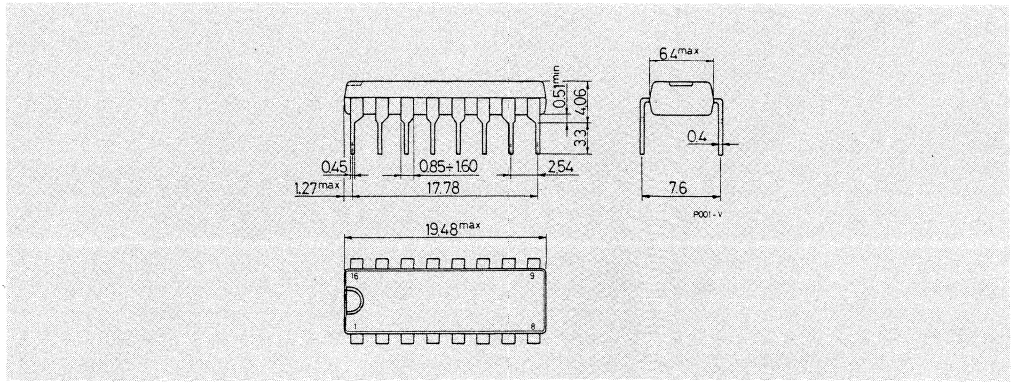
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 15 | V |
| $I_o$ | Output peak current | 1.5 | A |
| $P_{tot}$ | Total power dissipation at $T_{amb}$ = 50°C | 1.25 | W |
| | at $T_{case}$ = 70°C | 4 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | −40 to 150°C | |

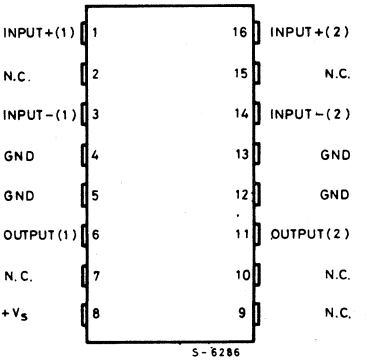
**ORDERING NUMBER:** TDA 2822

## MECHANICAL DATA

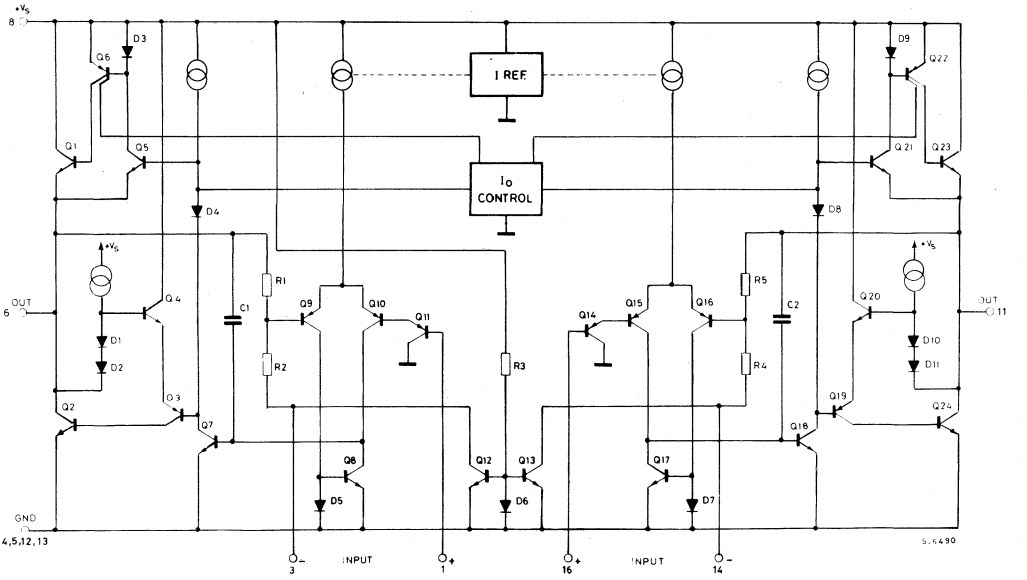
Dimensions in mm



## CONNECTION DIAGRAM
(top view)



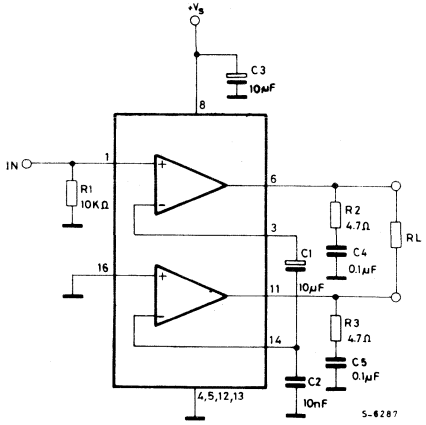

## SCHEMATIC DIAGRAM




## THERMAL DATA

| | | | |
|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max 80 | °C/W |
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-pins | max 20 | °C/W |

Fig. 1 - Test circuit (Bridge)

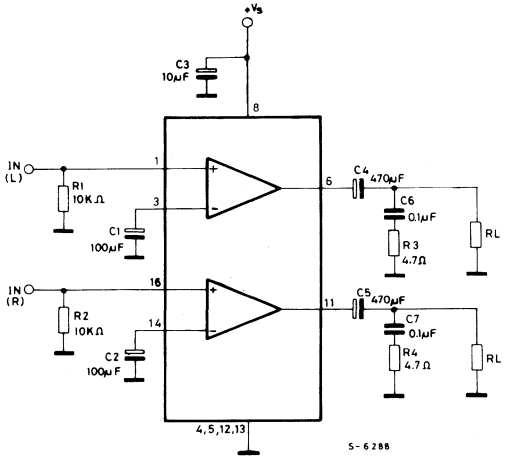



## ELECTRICAL CHARACTERISTICS ($V_s$ = 6V, $T_{amb}$ = 25°C, unless otherwise specified)

**Bridge** (Test circuit of fig. 1)

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 3 | | 15 | V |
| $I_d$ | Quiescent drain current | $R_L = \infty$ | | 6 | 12 | mA |
| $V_{os}$ | Output offset voltage | $R_L$ = 8 ohm | | 10 | 60 | mV |
| $I_b$ | Input bias current | | | 100 | | nA |
| $P_o$ | Output power | d = 10%, f = 1KHz<br>$V_s$ = 9V $R_L$ = 8 ohm<br>$V_s$ = 6V $R_L$ = 8 ohm<br>$V_s$ = 4,5V $R_L$ = 4 ohm | | <br>3.5<br>1.4<br>1.1 | | <br>W<br>W<br>W |
| $G_v$ | Closed loop voltage gain | f = 1KHz | | 40 | | dB |
| $R_i$ | Input resistance | f = 1KHz | | 100 | | Kohm |
| $e_N$ | Total input noise | $R_s$ = 10K ohm, B = 22 Hz to 22 KHz | | 3 | | µV |
| | | $R_s$ = 10K ohm, curve A | | 2 | | µV |
| SVR | Supply voltage rejection | f = 100Hz | | 40 | | dB |

Fig. 2 - Test circuit (Stereo)

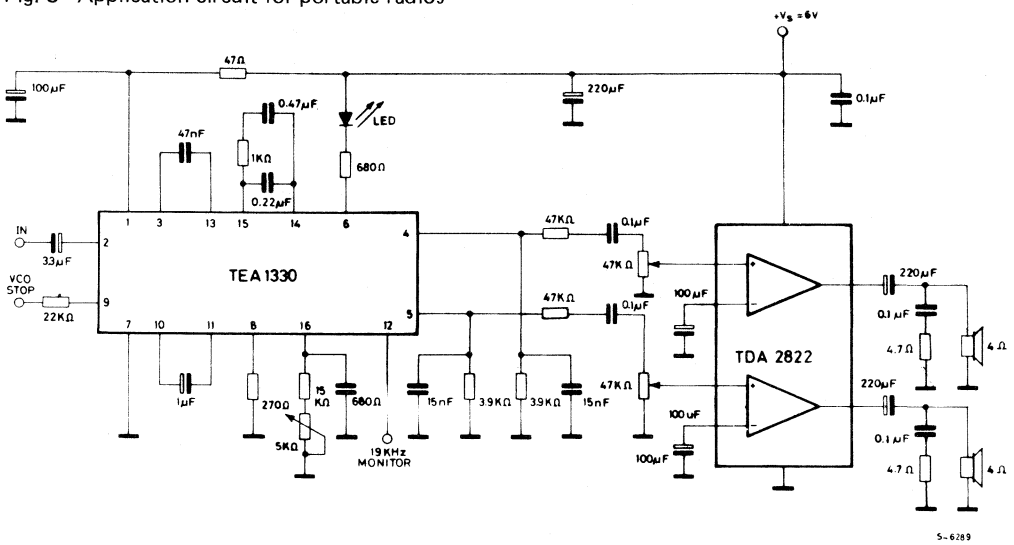



## ELECTRICAL CHARACTERISTICS ($V_s$ = 6V, $T_{amb}$ = 25°C, unless otherwise specified)

**Stereo** (Test circuit of fig. 2)

| Parameter | | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | 3 | | 15 | V |
| $V_c$ | Quiescent output voltage | $V_s$ = 9V<br>$V_s$ = 6V | | | 4.5<br>2.7 | | V<br>V |
| $I_d$ | Quiescent drain current | | | | 6 | 12 | mA |
| $I_b$ | Input bias current | | | | 100 | | nA |
| $P_o$ | Output power (each channel) | d = 10%<br>$V_s$ = 9V<br>$V_s$ = 6V<br>$V_s$ = 4.5V | f = 1KHz<br>$R_L$ = 4 ohm<br>$R_L$ = 4 ohm<br>$R_L$ = 4 ohm | | <br>1.8<br>0.7<br>0.35 | | <br>W<br>W<br>W |
| $G_v$ | Closed loop voltage gain | f = 1KHz | | | 40 | | dB |
| $R_i$ | Input resistance | f = 1KHz | | | 100 | | K ohm |
| $e_N$ | Total input noise | $R_s$ = 10K ohm | B = 22 Hz to 22 KHz | | 3 | | µV |
| | | | Curve A | | 2 | | µV |
| SVR | Supply voltage rejection | f = 100 Hz | | | 30 | | dB |
| CS | Channel separation | $R_g$ = 10 KΩ | f = 1 KHz | | 50 | | dB |

Fig. 3 - Application circuit for portable radios




## MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA 2822 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 4) or to an external heatsink (Fig. 5).

The diagram of figure 6 shows the maximum dissipable power $P_{tot}$ and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35µ (1.4 mils).

During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

## MOUNTING INSTRUCTION (continued)

Fig. 4 - Example of P.C. board copper area which is used as heatsink.

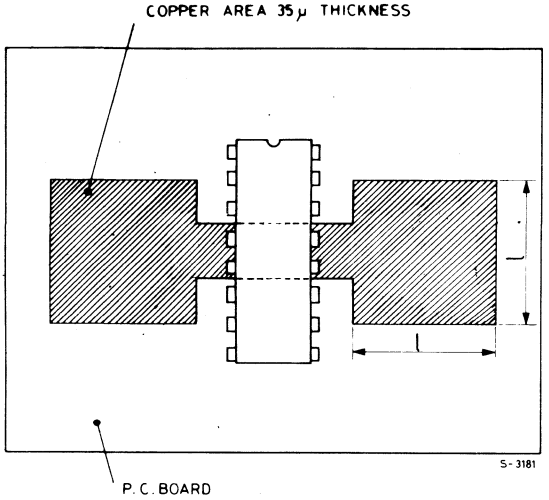



Fig. 5 - External heatsink mounting example

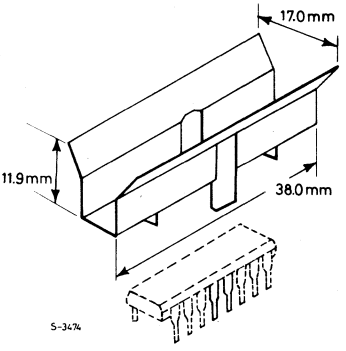



Fig. 6 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

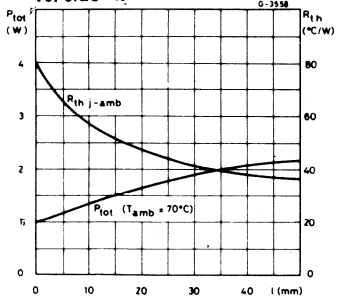
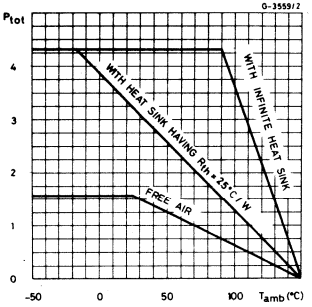



Fig. 7 - Maximum allowable power dissipation vs. ambient temperature



# LINEAR INTEGRATED CIRCUITS

**TDA2822M**

**ADVANCE DATA**

## DUAL LOW-VOLTAGE POWER AMPLIFIER

- SUPPLY VOLTAGE DOWN TO 1.8V
- LOW CROSSOVER DISTORTION
- LOW QUIESCENT CURRENT
- BRIDGE OR STEREO CONFIGURATION

The TDA 2822M is a monolithic integrated circuit in 8 lead Minidip package. It is intended for use as dual audio power amplifier in portable cassette players and radios.

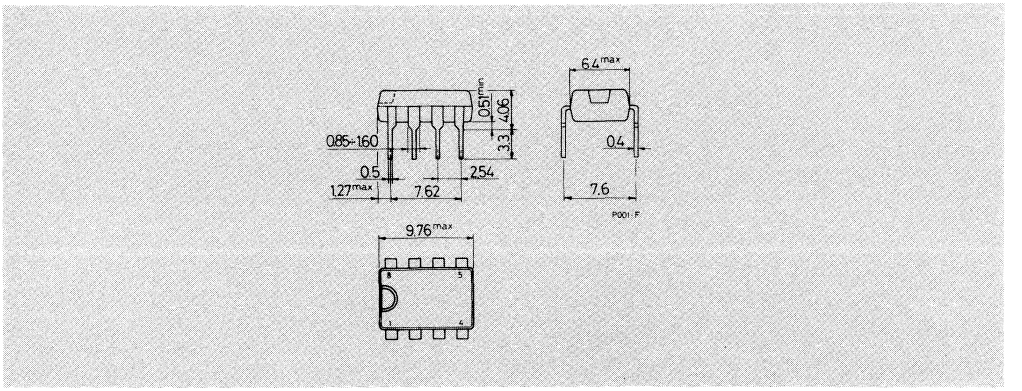
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 15 | V |
| $I_o$ | Peak output current | 1 | A |
| $P_{tot}$ | Total power dissipation at $T_{amb} = 50°C$ | 1 | W |
| | at $T_{case} = 50°C$ | 1.4 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA 2822M

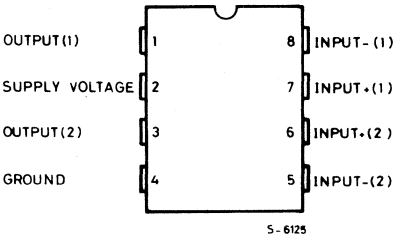
## MECHANICAL DATA

Dimensions in mm

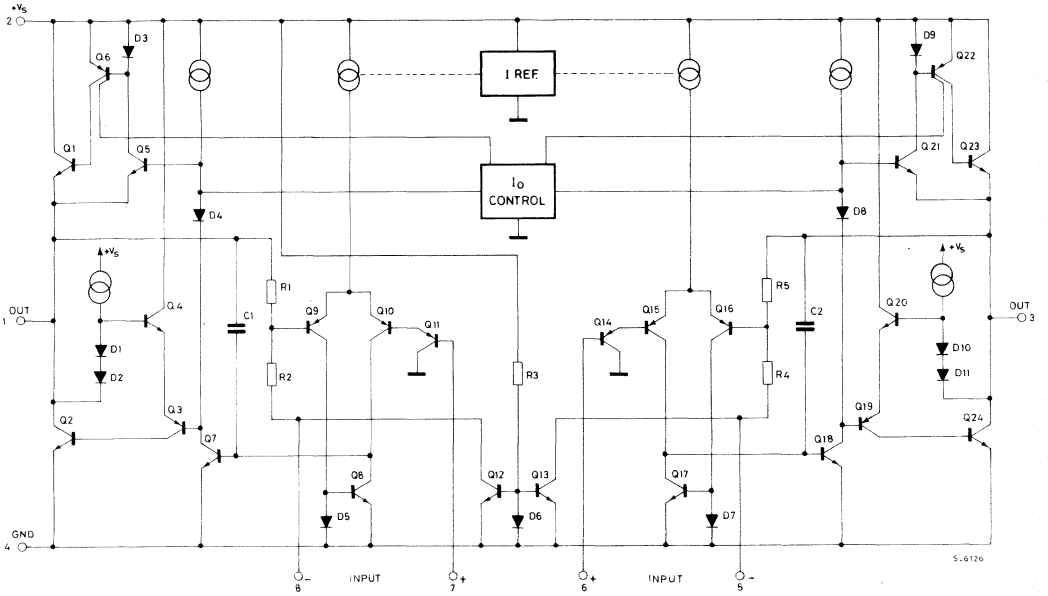


# TDA2822M

## CONNECTION DIAGRAM
(top view)




## SCHEMATIC DIAGRAM




## THERMAL DATA

| | | |
|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max 100 °C/W |
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-pin (4) | max 70 °C/W |

Fig. 1 - Test circuit (stereo)

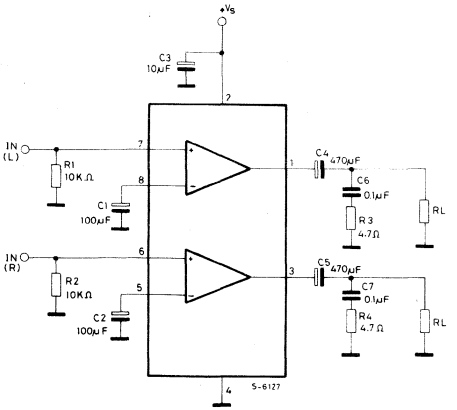
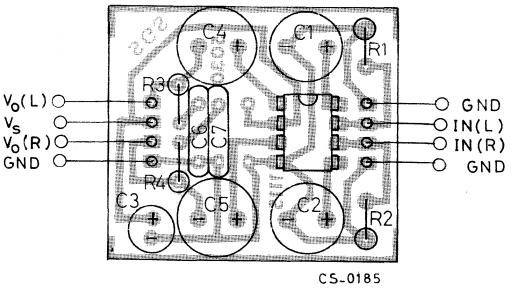



Fig. 2 - PC board and components layout of the circuit of Fig. 1 (1:1 scale)




## ELECTRICAL CHARACTERISTICS ($V_s$ = 6V, $T_{amb}$ = 25°C, unless otherwise specified)

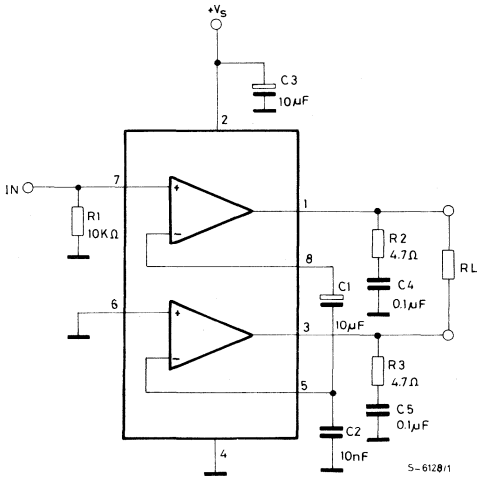
**Stereo** (Test circuit of fig. 1)

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 1.8 | | 15 | V |
| $V_o$ | Quiescent output voltage | | | 2.7 | | V |
| | | $V_s$ = 3V | | 1.2 | | V |
| $I_d$ | Quiescent drain current | | | 6 | 9 | mA |
| $I_b$ | Input bias current | | | 100 | | nA |
| $P_o$ | Output power (each channel) | d = 10% f = 1 KHz<br>$V_s$ = 3V $R_L$ = 4Ω<br>$V_s$ = 3V $R_L$ = 32Ω | | 110<br>20 | | mW |
| | | d = 10% f = 1KHz<br>$V_s$ = 9V $R_L$ = 8Ω<br>$V_s$ = 6V $R_L$ = 4Ω<br>$V_s$ = 4.5V $R_L$ = 4Ω | 0.4 | 1<br>0.65<br>0.32 | | W |

## ELECTRICAL CHARACTERISTICS

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| d | Distortion | $P_O$ = 0.5W $R_L = 8\Omega$<br>f = 1KHz $V_S$ = 9V | | 0.3 | | % |
| $G_v$ | Closed loop voltage gain | f = 1KHz | | 40 | | dB |
| $\Delta G_v$ | Channel balance | | | | ± 1 | dB |
| $R_i$ | Input resistance | f = 1KHz | 100 | | | KΩ |
| $e_N$ | Total input noise | $R_S$ = 10KΩ B = Curve A | | 2 | | μV |
| | | $R_S$ = 10KΩ B = 22 Hz to 22 KHz | | 3 | | |
| SVR | Supply voltage rejection | f = 100Hz C1 = C2 = 100 μF | 24 | 30 | | dB |
| $C_s$ | Channel separation | f = 1KHz | | 50 | | dB |

Fig. 3 - Test circuit (Bridge)



## ELECTRICAL CHARACTERISTICS ($V_s$ = 6V, $T_{amb}$ = 25°C, unless otherwise specified)

**Bridge** (Test circuit of fig. 3)

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 1.8 | | 15 | V |
| $I_d$ | Quiescent drain current | $R_L = \infty$ | | 6 | 9 | mA |
| $V_{os}$ | Output offset voltage (between the outputs) | $R_L = 8\Omega$ | | | ± 50 | mV |
| $I_b$ | Input bias current | | | 100 | | nA |
| $P_o$ | Output power | d = 10% f = 1KHz | | | | |
| | | $V_s$ = 9V $R_L = 16\Omega$ | | 2 | | |
| | | $V_s$ = 6V $R_L = 8\Omega$ | 0.9 | 1.35 | | W |
| | | $V_s$ = 4.5V $R_L = 8\Omega$ | | 0.7 | | |
| | | $V_s$ = 4.5V $R_L = 4\Omega$ | | 1 | | |
| | | $V_s$ = 3V $R_L = 4\Omega$ | 200 | 350 | | mW |
| | | $V_s$ = 2V $R_L = 4\Omega$ | | 80 | | |
| d | Distortion | $P_o$ = 0.5W $R_L = 8\Omega$ f = 1KHz | | 0.2 | | % |
| $G_v$ | Closed loop voltage gain | f = 1KHz | | 40 | | dB |
| $R_i$ | Input resistance | f = 1KHz | 100 | | | KΩ |
| $e_n$ | Total input noise | $R_s$ = 10KΩ B = Curve A | | 2.5 | | μV |
| | | $R_s$ = 10KΩ B = 22Hz to 22KHz | | 3 | | μV |
| SVR | Supply voltage rejection | f = 100Hz | | 40 | | dB |
| B | Power bandwidth (-3dB) | $R_L = 8\Omega$ $P_o$ = 1W | | 120 | | KHz |

Fig. 4 - Quiescent current vs. supply voltage

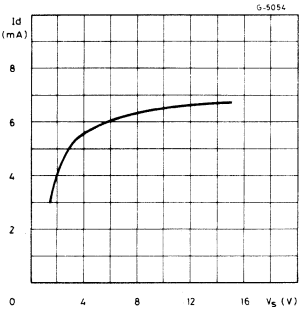



Fig. 5 - Supply voltage rejection vs. frequency (stereo)

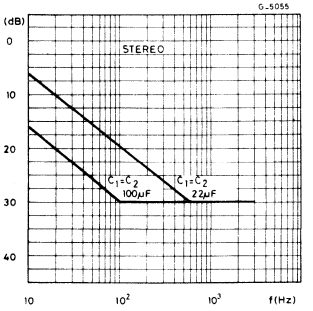



Fig. 6 - Typical application in portable players

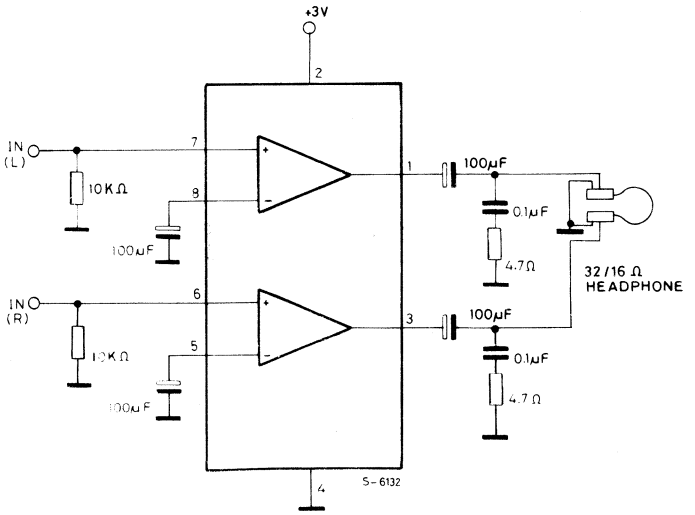


Fig. 7 - Application circuit for portable radio receivers

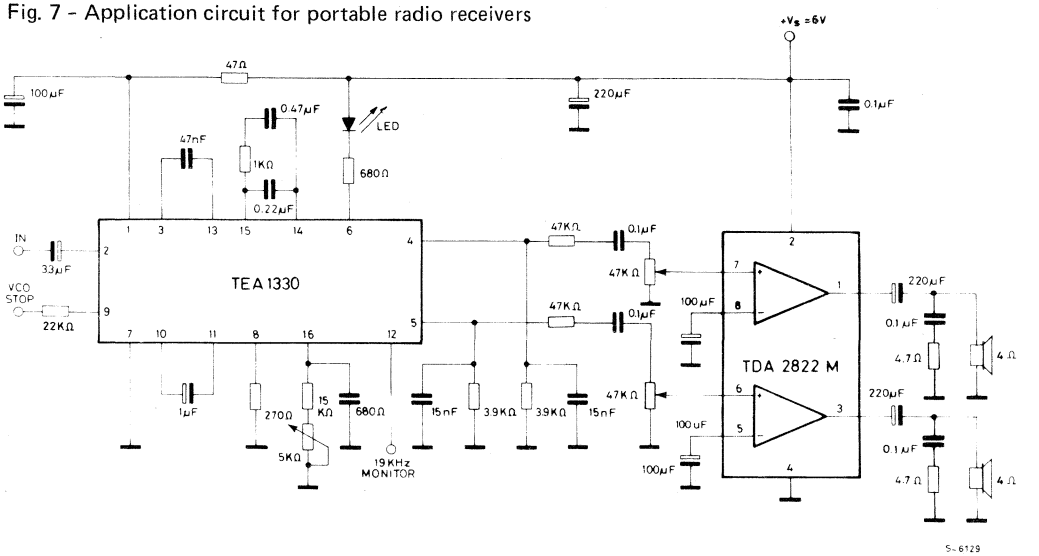
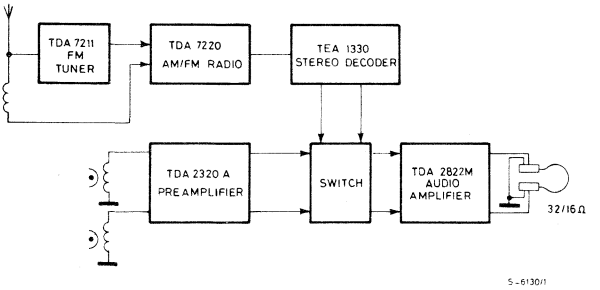
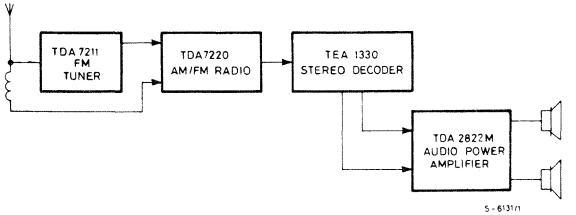



Fig. 8 - Portable radio cassette players



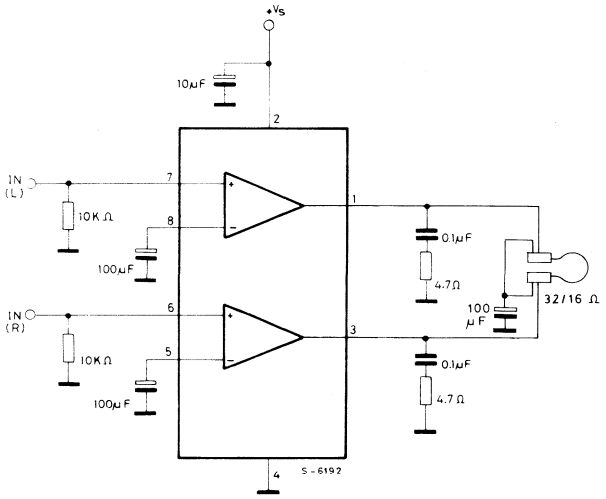

| TYPE | SUPPLY VOLTAGE |
|---|---|
| TDA 7220 | 1.5V to 6V |
| TDA 7211 | 1.2V to 6V |
| TEA 1330 | 3V to 15V |
| TDA 2320A | 3V to 36V |
| TDA 2822M | 1.8V to 15V |

Fig. 9 - Portable stereo radios




| TYPE | SUPPLY VOLTAGE |
|---|---|
| TDA 7220 | 1.5V to 6V |
| TDA 7211 | 1.2V to 6V |
| TEA 1330 | 3V to 15V |
| TDA 2822M | 1.8V to 15V |

Fig. 10 - Low cost application for portable players (using only one 100 $\mu$F output capacitor)



# TDA3190

## COMPLETE TV SOUND CHANNEL

The TDA3190 is a monolithic integrated circuit in a 16-lead dual in-line plastic package. It performs all the functions needed for the TV sound channel:

- IF limiter-amplifier
- Active low-pass filter
- FM detector
- DC volume control
- AF preamplifier
- AF output stage

The TDA 3190 can give an output power of 4.2W (d = 10%) into a 16Ω load at $V_s$= 24V, or 1.5W (d = 10%) into an 8Ω load at $V_s$= 12V. This performance, together with the FM-IF section characteristics of high sensitivity, high AM rejection and low distortion, enables the device to be used in almost every type of television receivers.
The device has no irradiation problems, hence no external screening is needed.
The TDA 3190 is a pin to pin replacement of TDA 1190Z.

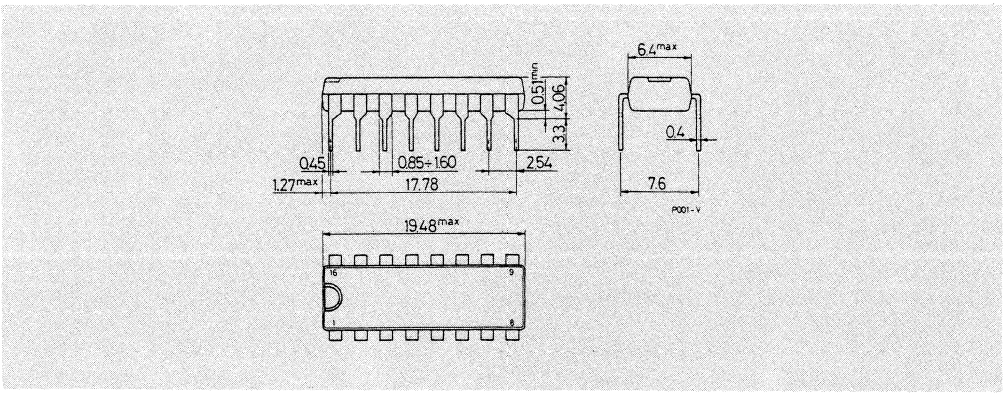
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 10) | 28 | V |
| $V_i$ | Input signal voltage (pin 1) | 1 | V |
| $I_o$ | Output peak current (non-repetitive) | 2 | A |
| $I_o$ | Output peak current (repetitive) | 1.5 | A |
| $P_{tot}$ | Power dissipation: at $T_{pins}$ = 90°C | 4.3 | W |
| | at $T_{amb}$ = 70°C (free air) | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

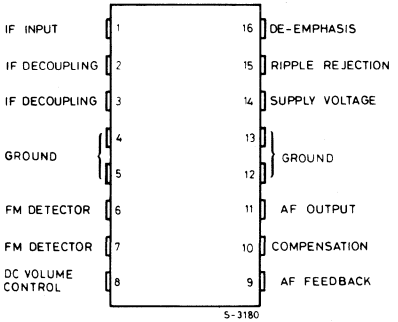
**ORDERING NUMBERS:** TDA 3190

## MECHANICAL DATA

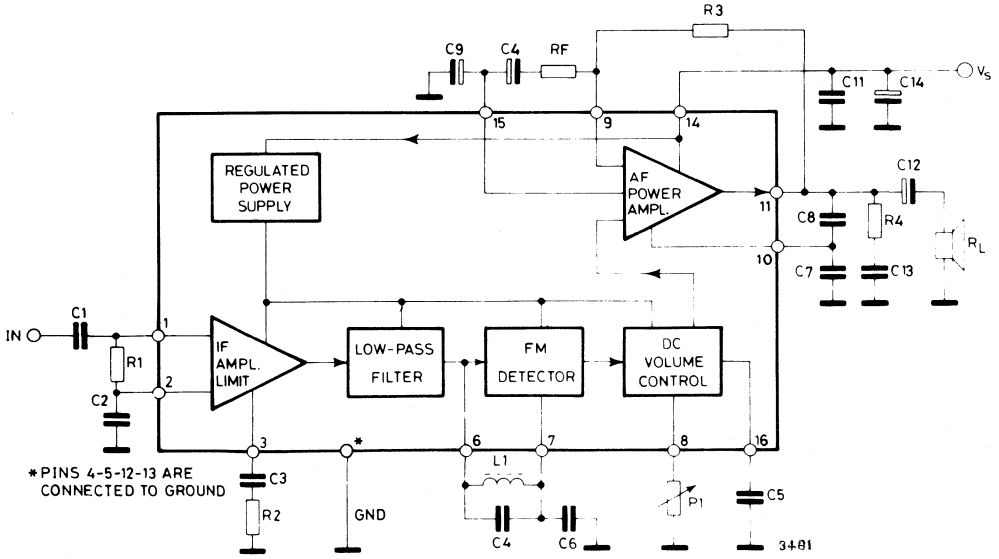
Dimensions in mm



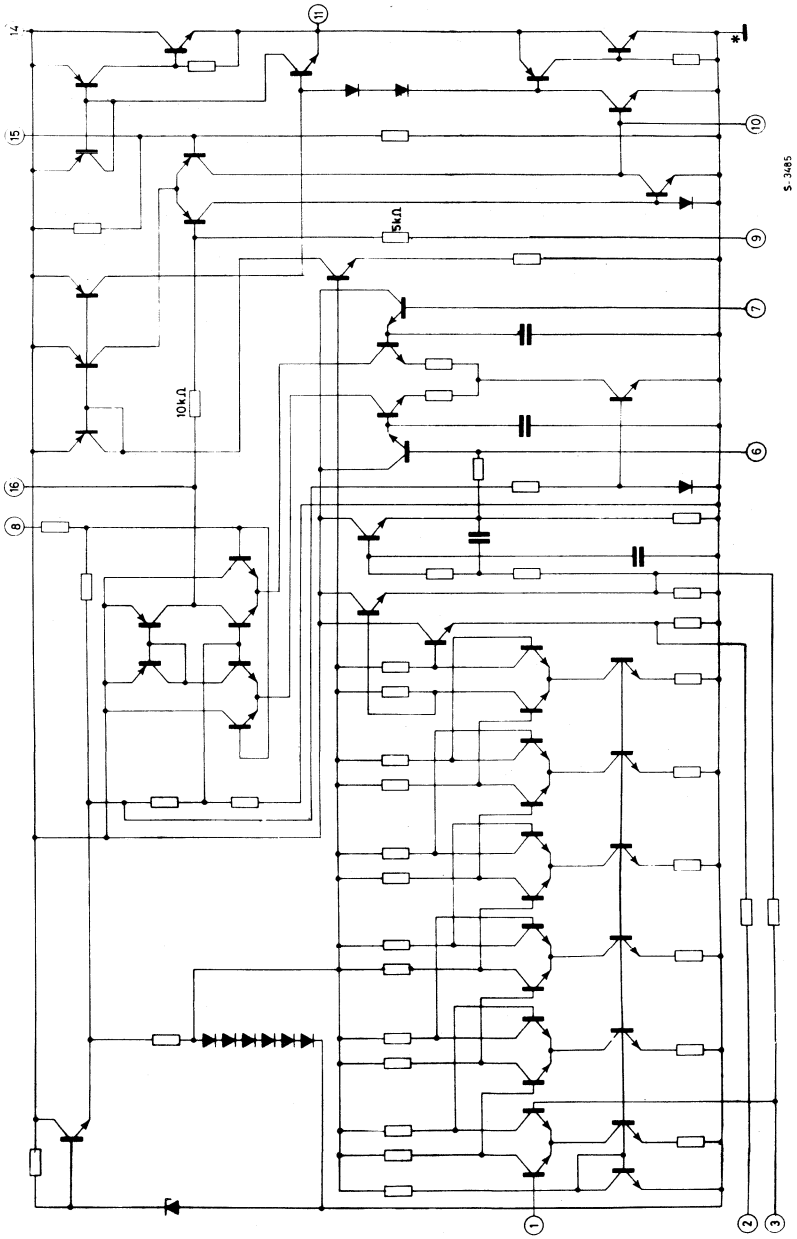
## CONNECTION DIAGRAM




## BLOCK DIAGRAM

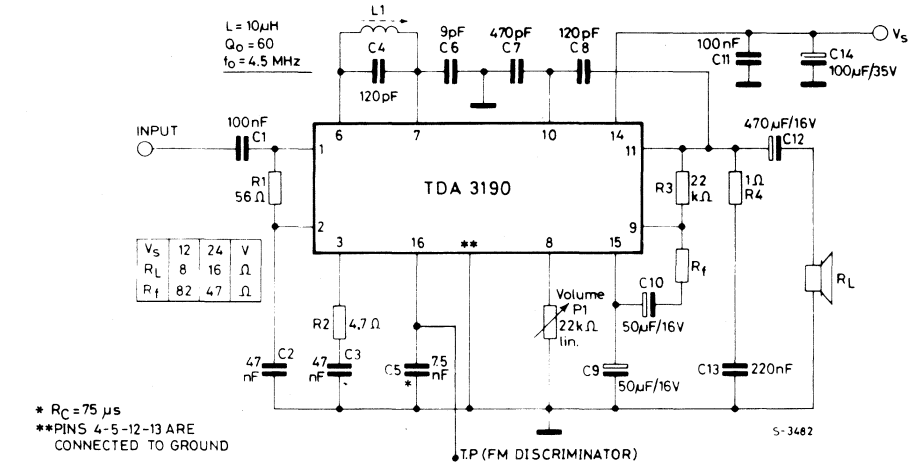


## SCHEMATIC DIAGRAM




*PINS 4-5-12-13 ARE CONNECTED TO GROUND

## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}pins}$ | Thermal resistance junction-pins | max | 14 | °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 80* | °C/W |

* Obtained with the GND pins soldered to printed circuit with minimized copper area.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s$= 24V, $T_{amb}$= 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage (pin 14) | | 9 | | 28 | V |
| $V_o$ | Quiescent output voltage (pin 11) | $V_s$= 24V<br>$V_s$= 12V | 11<br>5.1 | 12<br>6 | 13<br>6.9 | V<br>V |
| $I_d$ | Quiescent drain current | $P_1$ = 22KΩ<br>$V_s$ = 24V<br>$V_s$ = 12V | 11 | 22<br>19 | 45<br>40 | mA<br>mA |
| $P_o$ | Output power | d = 10% $f_m$= 400 Hz<br>$f_o$= 4.5 MHz Δf = ± 25 KHz<br>$V_s$ = 24V $R_L$= 16Ω<br>$V_s$ = 12V $R_L$= 8Ω | | 4.2<br>1.5 | | W<br>W |
| | | d = 2% $f_m$= 400 Hz<br>$f_o$ = 4.5 MHz Δf= ± 25 KHz<br>$V_s$ = 24V $R_L$= 16Ω<br>$V_s$ = 12V $R_L$= 8Ω | | 3.5<br>1.4 | | W<br>W |

## ELECTRICAL CHARACTERISTICS (continued)

| | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_i$ | Input limiting voltage (-3 dB) at pin 1 | $f_o$ = 4.5 MHz $\Delta f$ = ± 7.5 KHz<br>$f_m$ = 400 Hz<br>$P_1$ = 0 | | 40 | 100 | μV |
| d | Distortion | $P_o$ = 50 mW $f_m$ = 400 Hz<br>$f_o$ = 4.5 MHz $\Delta f$ = ± 7.5 KHz<br>$V_s$ = 24V $R_L$ = 16Ω<br>$V_s$ = 12V $R_L$ = 8Ω | | 0.75<br>1 | | %<br>% |
| B | Frequency response of audio amplifier (-3 dB) | $R_L$ = 16Ω $C_8$ = 120 pF<br>$C_7$ = 470 pF $P_1$ = 22 KΩ<br>$R_f$ = 82Ω<br>$R_f$ = 47Ω | | 70 to 12000<br>70 to 7000 | | Hz<br>Hz |
| $V_o$ | Recovered audio voltage (pin 16) | $V_i$ ⩾ 1 mV $f_o$ = 4.5 MHz<br>$f_m$ = 400 Hz $\Delta f$ = ± 7.5 KHz<br>$P_1$ = 0 | | 120 | | mV |
| AMR | Ampliture modulation rejection | $V_i$ ⩾ 1 mV $f_o$ = 4.5 MHz<br>$f_m$ = 400 Hz $\Delta f$ = ± 25 KHz<br>m = 0.3 | | 55 | | dB |
| $\frac{S+N}{N}$ | Signal to noise ratio | $V_i$ ⩾ 1 mV $V_o$ = 4V<br>$f_o$ = 4.5 MHz $f_m$ = 400 Hz<br>$\Delta f$ = ± 25 KHz | 50 | 65 | | dB |
| $R_3$ | External feedback resistance (between pins 9 and 11) | | | | 25 | KΩ |
| $R_i$ | Input resistance (pin 1) | $V_i$ = 1 mV<br>$f_o$ = 4.5 MHz | | 30 | | KΩ |
| $C_i$ | Input capacitance (pin 1) | | | 5 | | pF |
| SVR | Supply voltage rejection | $R_L$ = 16Ω<br>$f_{ripple}$ = 120 Hz<br>$P_1$ = 22 KΩ | | 46 | | dB |
| $A_V$ | DC volume control attenuation | $P_1$ = 12 KΩ | | 90 | | dB |

Fig. 1 - Relative audio output voltage and output noise vs. input signal.

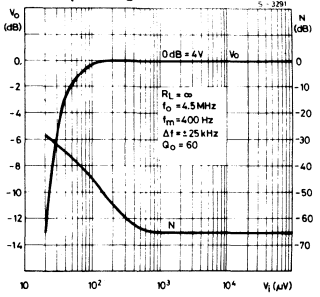



Fig. 2 - Output voltage attenuation vs. DC volume control resistance.

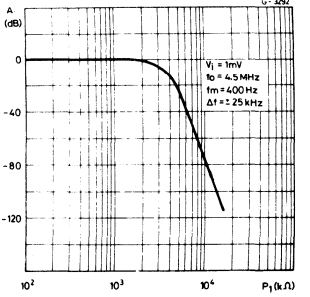



Fig. 3 - Amplitude modulation rejection vs. input signal

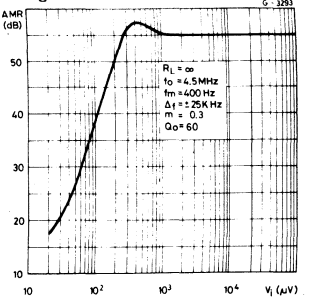



Fig. 4 - ΔAMR vs. tuning frequency change.

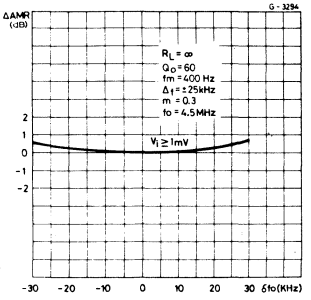



Fig. 5 - Recovered audio voltage vs. unloaded Q factor of the detector coil

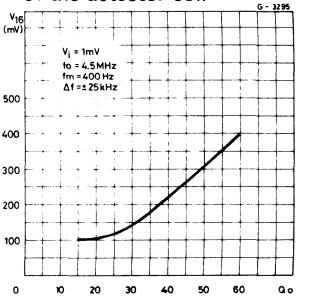



Fig. 6 - Distortion vs. output power

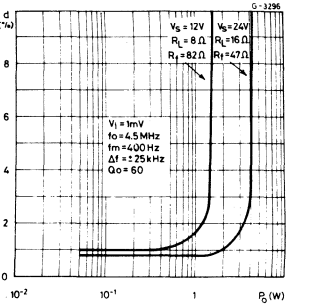



Fig. 7 - Distortion vs. frequency deviation

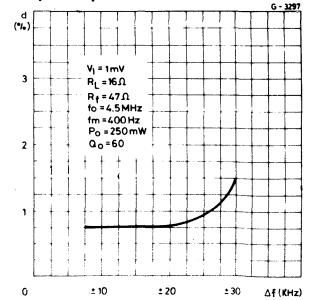



Fig. 8 - Distortion vs. tuning frequency change

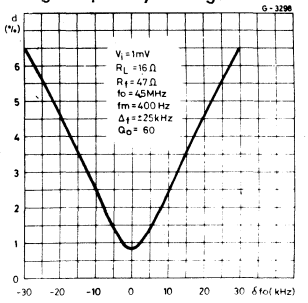



Fig. 9 - Audio amplifier frequency response

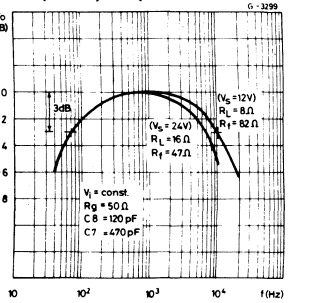


Fig. 10 - Supply voltage ripple rejection vs. ripple frequency

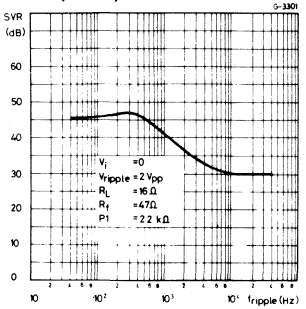



Fig. 11 - Supply voltage ripple rejection vs. volume control attenuation

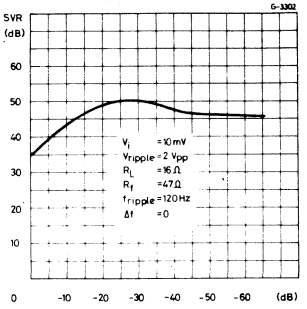



Fig. 12 - Output power vs. supply voltage

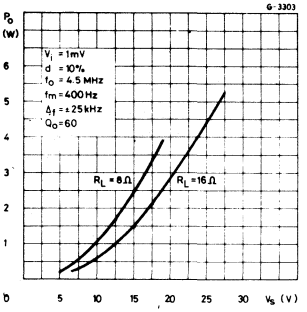



Fig. 13 - Maximum power dissipation vs. supply voltage (sine wave operation)

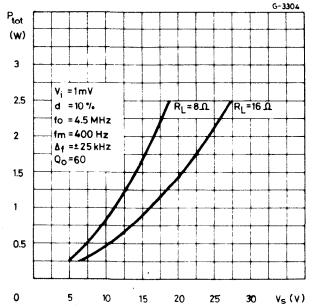



Fig. 14 - Power dissipation and efficiency vs. output power

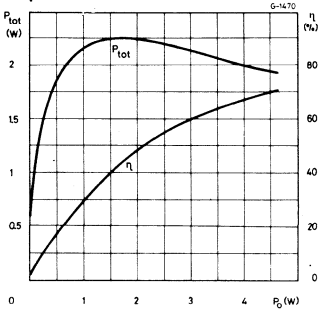
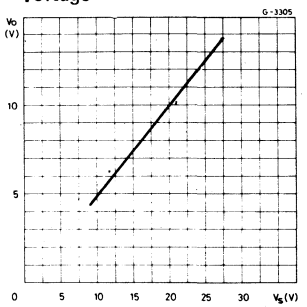



Fig. 15 - Quiescent output voltage (pin 11) vs. supply voltage




## APPLICATION INFORMATION

The electrical characteristics of the TDA 3190 remain almost constant over the frequency range 4.5 to 6 MHz, therefore it can be used in all television standards (FM mod.). The TDA 3190 has a high input impedance, so it can function with a ceramic filter or with a tuned circuit that provide the necessary input selectivity.

The value of the resistors connected to pin 9, determine the AC gain of the audio frequency amplifier. This enables the desired gain to be selected in relation to the frequency deviation at which the output stage of the AF amplifier, must enter into clipping.

Capacitor C8, connected between pins 10 and 11, determines the upper cutoff frequency of the audio bandwidth. To increase the bandwidth the values of C8 and C7 must be reduced, keeping the ratio C7/C8 as shown in the table of fig. 16.

The capacitor connected between pin 16 and ground, together with the internal resistor of 10 KΩ forms the de-emphasis network. The Boucherot cell eliminates the high frequency oscillations caused by the inductive load and the wires connecting the loudspeaker.

## APPLICATION INFORMATION (continued)

Fig. 16 - Typical application circuit

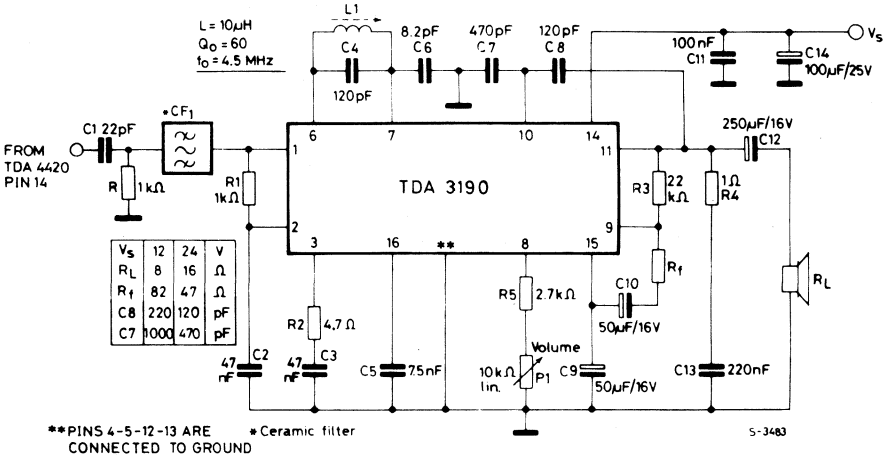
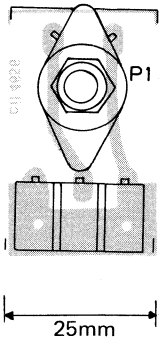
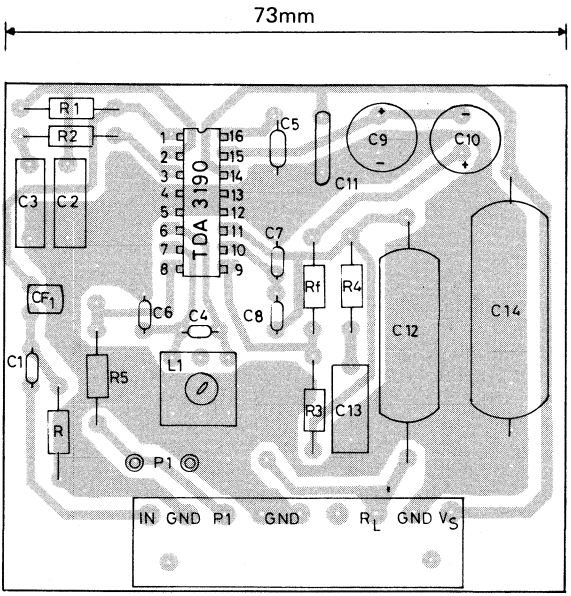



Fig. 17 - P.C. board and component layout of the circuit shown in Fig. 16 (1:1 scale)




CS-0097/1

## MOUNTING INSTRUCTION

The $R_{th\ j\text{-}amb}$ of the TDA 3190 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board (Fig. 18) or to an external heatsink (Fig. 19).
The diagram of figure 20 shows the maximum dissipable power $P_{tot}$ and the $R_{th\ j\text{-}amb}$ as a function of the side "ℓ" of two equal square copper areas having a thickness of 35μ (1.4 mils).
During soldering the pins temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.
The external heatsink or printed circuit copper area must be connected to electrical ground.

Fig. 18 - Example of P.C. board copper area which is used as heatsink.

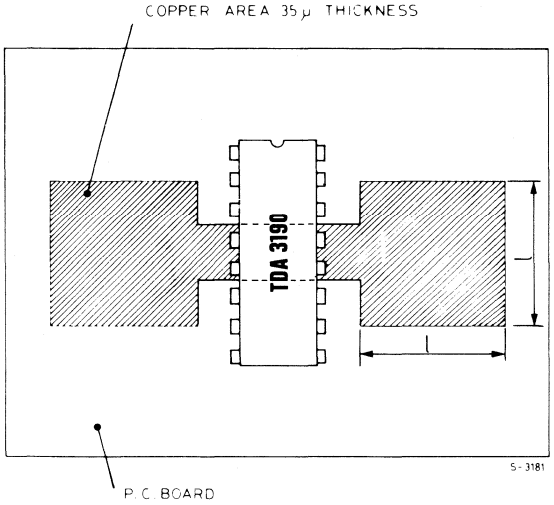



Fig. 19 - External heatsink mounting example

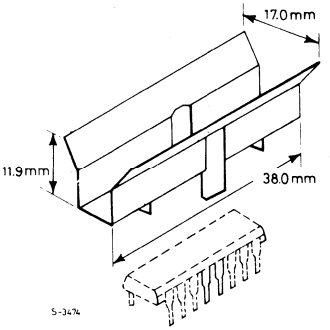



Fig. 20 - Maximum dissipable power and junction to ambient thermal resistance vs. side "ℓ"

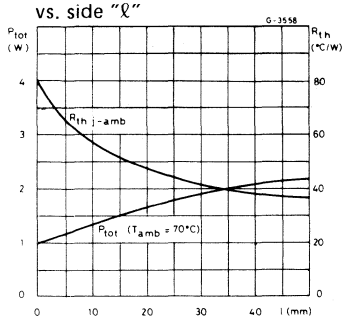
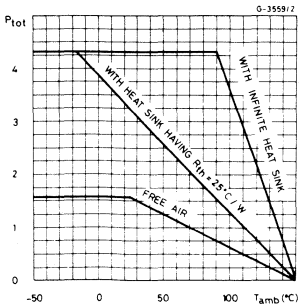



Fig. 21 - Maximum allowable power dissipation vs. ambient temperature



## DUAL LOW NOISE TAPE PREAMPLIFIER WITH AUTOREVERSE

The TDA 3410 is a dual preamplifier with tape autoreverse facility for the amplification of low level signals in applications requiring very low noise performance, as stereo cassette players. Each channel consists of two independent amplifiers. The first has a fixed gain of 30 dB while the second one is an operational amplifier optimized for high quality audio application.
The TDA 3410 is a monolithic integrated circuit in a 16-lead dual in-line plastic package and its main features are:

- Very low noise
- High gain
- Low distortion
- Single supply operation
- Wide supply range
- SVR = 120 dB
- Large output voltage swing
- Tape autoreverse facility
- Short circuit protection

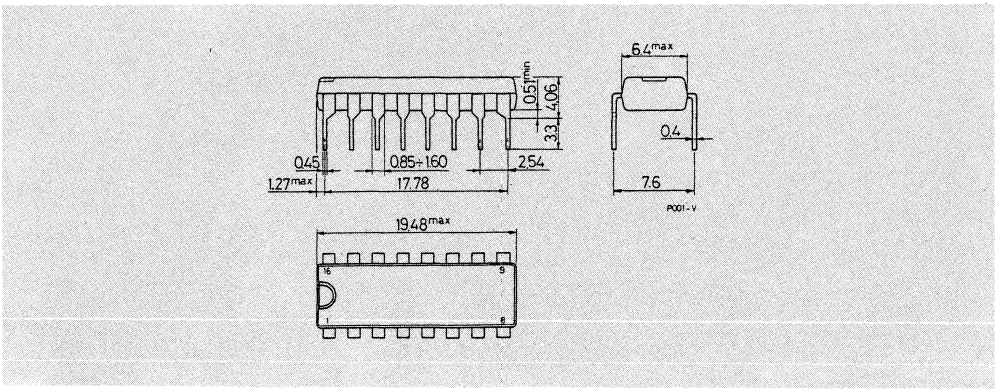
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 36 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb} = 60°C$ | 600 | mW |
| $T_j$, $T_{stg}$ | Storage and junction temperature | -40 to 150 | °C |

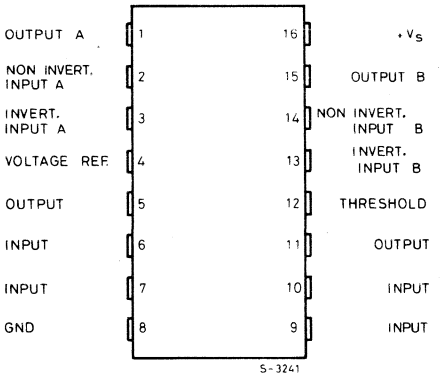
**ORDERING NUMBER:** TDA 3410

## MECHANICAL DATA

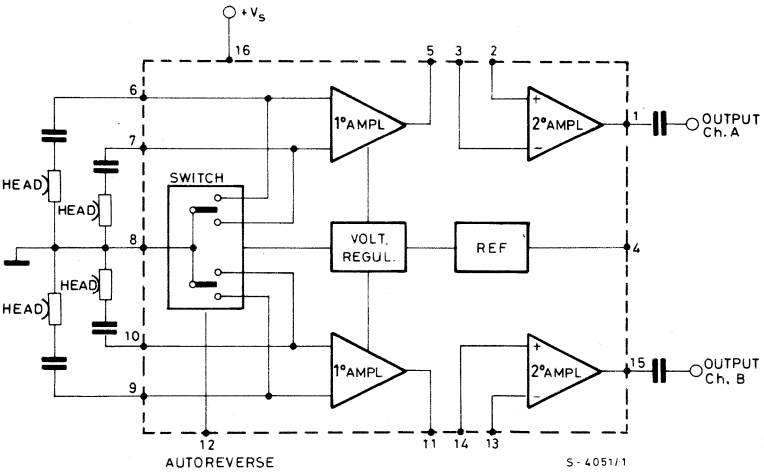
Dimensions in mm



## CONNECTION DIAGRAM (top view)



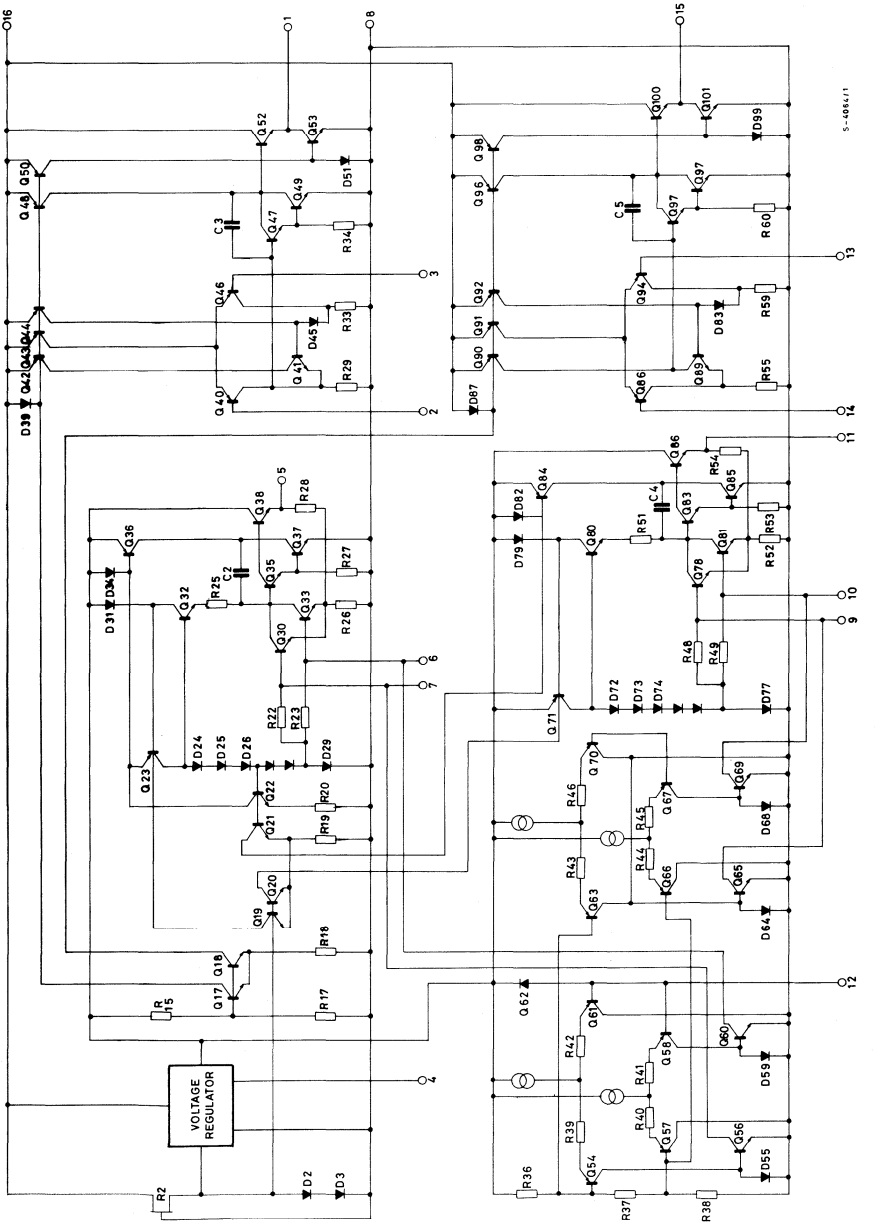

## BLOCK DIAGRAM



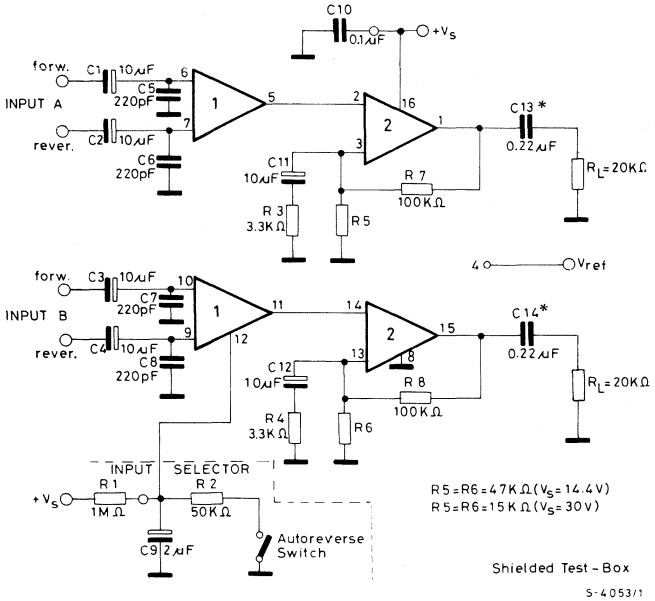

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 150 | °C/W |

## SCHEMATIC DIAGRAM



## TEST CIRCUIT (Flat Gain - $G_v$= 60 dB)




* Mylar or polycarbonate capacitors.

## ELECTRICAL CHARACTERISTICS ($T_{amb}$= 25°C, $V_s$= 14.4V, $G_v$= 60 dB, refer to the test circuit, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_s$ | Supply current | $V_s$= 8V to 30V | | 10 | | mA |
| $I_o$ | Output current (pins 1-15) | Source $V_s$= 8V to 30V | | 10 | | mA |
| | | Sink | | 1 | | mA |
| $G_v$ | Closed loop gain | f = 20 Hz to 20 KHz | | 60 | | dB |
| $R_i$ | Input resistance | f = 1 KHz | 50 | 80 | | KΩ |
| $R_o$ | Output resistance (pins 1-15) | f = 1 KHz | | 50 | | Ω |
| THD | Total harmonic distortion | $V_o$= 300 mV f = 1 KHz | | 0.05 | | % |
| | | f = 10 KHz | | 0.05 | | % |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_o$ | Output voltage swing (pins 1-15) | Peak to Peak $V_s$= 14.4V<br>$V_s$= 30V | | 12<br>28 | | .V<br>V |
| $V_o$ | Output voltage (pins 1-15) | d = 0.5% $V_s$= 14.4V<br>f = 1 KHz $V_s$= 30V | | 4<br>8 | | $V_{rms}$<br>$V_{rms}$ |
| $e_n$ | Total input noise (°) | $R_g$= 50Ω<br>$R_g$= 600Ω<br>$R_g$= 5KΩ | | 0.25<br>0.4<br>1.3 | <br>0.6<br> | μV<br>μV<br>μV |
| S/N | Signal to noise ratio (°) | $V_{in}$= 0.3 mV $R_g$= 600Ω<br>$V_{in}$= 1 mV $R_g$= 0 | | 57<br>73 | | dB<br>dB |
| CS | Channel separation | f = 1 KHz | | 60 | | dB |
| CT(°°°) | Cross-talk (differential input) | f = 1 KHz | | 80 | | dB |
| SVR | Supply voltage rejection (°°) | f = 1 KHz $R_g$= 600Ω | | 120 | | dB |
| SVR (°°) | Of reference voltage (Pin 4) | f = 1 KHz<br>$R_g$= 600Ω | | 100 | | dB |
| $V_{ref}$ | Reference voltage (pin 4) | | | 55 | | mV |
| $R_{ref}$ | Ref. voltage output resistance (pin 4) | | | 100 | | Ω |
| $\frac{\Delta V_{ref}}{\Delta T}$ | Voltage temperature coefficient | | | 10 | | μV/°C |

(°) The weighting filter used for the noise measurement has a curve A frequency response.
(°°) Referred to the input.
(°°°) Between a disabled input and an input ON.

## ELECTRICAL CHARACTERISTICS (Refer test circuit, $V_s$= 30V)

### AMPLIFIER N° 1

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $G_v$ | Gain (pins 6 to 5) | | 29 | 30 | 30.5 | dB |
| d | Distortion | $V_o$= 300 mV f = 1 KHz<br>f = 10 KHz | | 0.05<br>0.05 | | % |
| $e_n$ | Total input noise (°) | $R_g$= 600Ω | | 0.4 | | μV |
| $Z_o$ | Output impedance (pin 5) | f = 1 KHz | | 100 | | Ω |
| $I_o$ | Output current (pin 5) | | | 1 | | mA |
| $V_5$ | DC output voltage (pin 5) | $V_s$ = 10V | 1.3 | 2 | 2.7 | V |

### AMPLIFIER N° 2

| | | | | | | |
|---|---|---|---|---|---|---|
| $G_v$ | Open loop voltage gain (pins 2 to 1) | | | 100 | | dB |
| $I_B$ | Input bias current | | | 0.2 | | μA |
| $V_{os}$ | Input offset voltage | | | 2 | | mV |
| $I_{os}$ | Input offset current | | | 0.05 | | μA |
| BW | Small signal bandwidth | $G_v$= 30 dB | | 150 | | KHz |
| $e_n$ | Total input noise (°) | $R_g$= 600Ω | | 2 | | μV |
| $R_i$ | Input impedance | f = 1 KHz (open loop) | 150 | 500 | | KΩ |

### AUTOREVERSE

| $P_{in}$ | $V_{12} < 2V$ | $V_{12} > 4.5V$ |
|---|---|---|
| 6 – 10 | OFF | ON |
| 7 – 9 | ON | OFF |

(°) The weighting filter used for the noise measurement has a curve A frequency response.

Fig. 1 - Total input noise vs. source resistance (curve A)

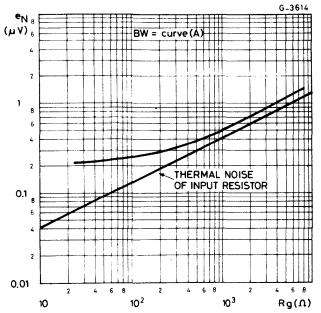



Fig. 2 - Total input noise vs. source resistance (BW= 22 Hz to 22 KHz)

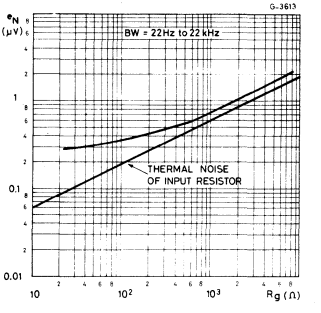



Fig. 3 - Total harmonic distortion vs. output voltage

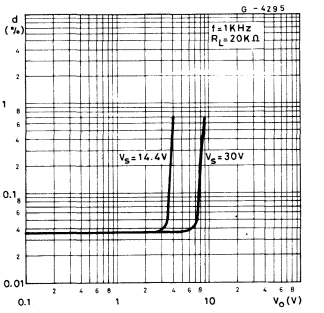



Fig. 6 - Very low noise stereo preamplifier for car cassette players (with Gap Loss Correction and autoreverse function)

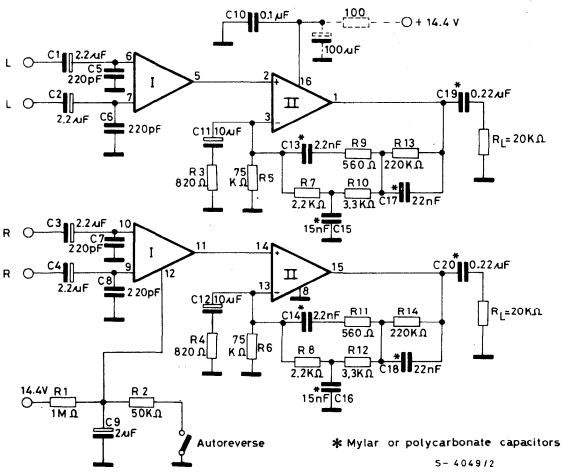



Fig. 5 - Frequency response

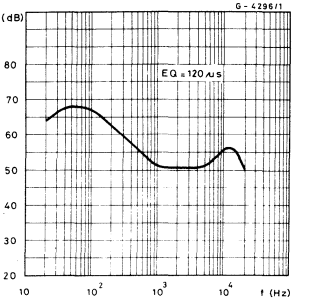


Fig. 6 - P.C. board and component lay-out (1:1 scale) for the circuit of fig. 4

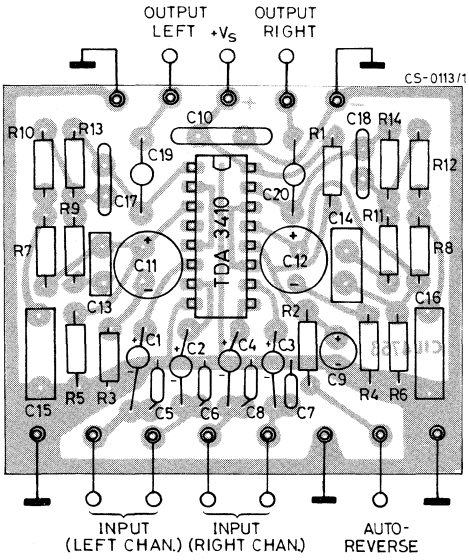



Fig. 7 - Stereo preamplifier for car cassette players, with low value capacitors (Autoreverse function)

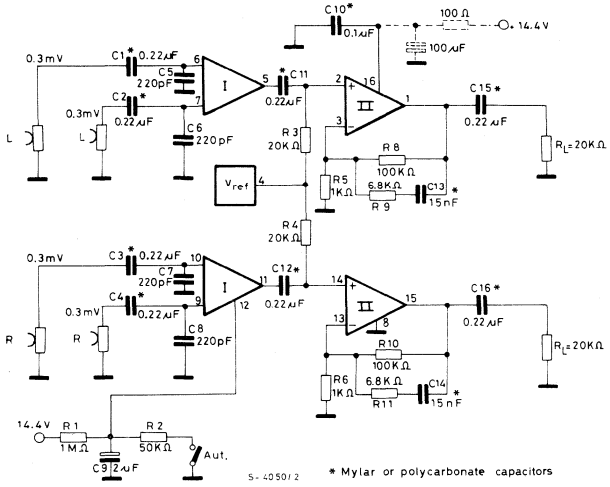
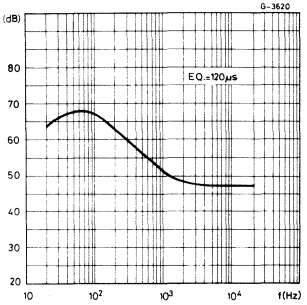



Fig. 8 - Frequency response



# TDA3420

# LINEAR INTEGRATED CIRCUITS

**PRELIMINARY DATA**

## DUAL VERY LOW NOISE PREAMPLIFIER

The TDA 3420 is a dual preamplifier for applications requiring very low noise performance, **as stereo cassette players** and quality audio systems. Each channel consists of two independent amplifiers.
The first one has a fixed gain while the second one is an operational amplifier for audio application.
The TDA 3420 is available in two packages: 16-lead daul in-line plastic and 16 lead micropackage.
Its main features are:

- Very low noise
- High gain
- Low distortion
- Single supply operation
- Large output voltage swing
- Short circuit protection

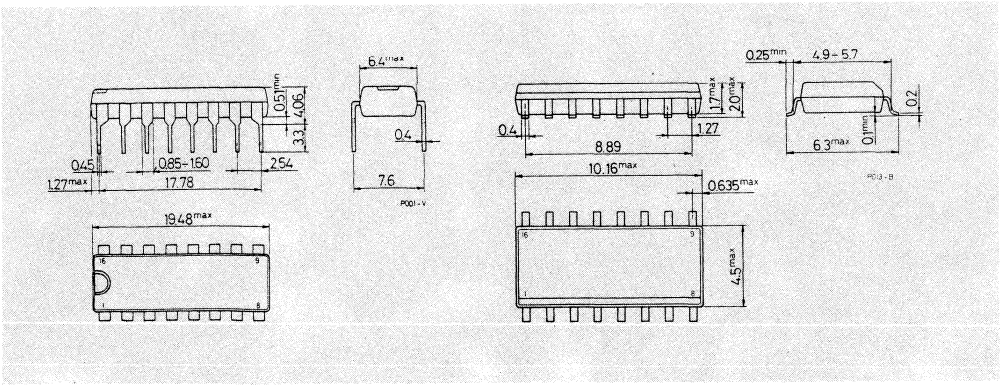
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 20 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb}$ = 70°C Dip | 550 | mW |
| | SO-16 | 400 | mW |
| $T_j$, $T_{stg}$. | Storage and junction temperature | -40 to 150 | °C |

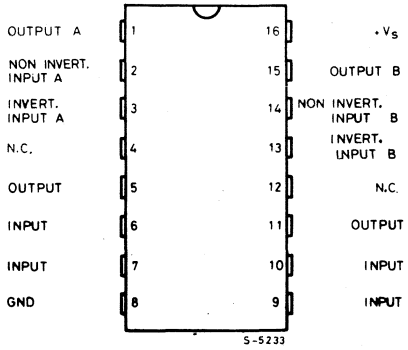
**ORDERING NUMBERS:** TDA 3420 (DIP)
L 343M (SO-16)

## MECHANICAL DATA

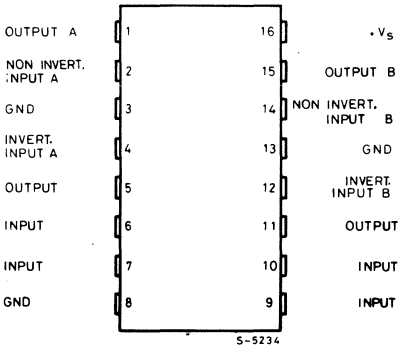
Dimensions in mm



## CONNECTION DIAGRAMS

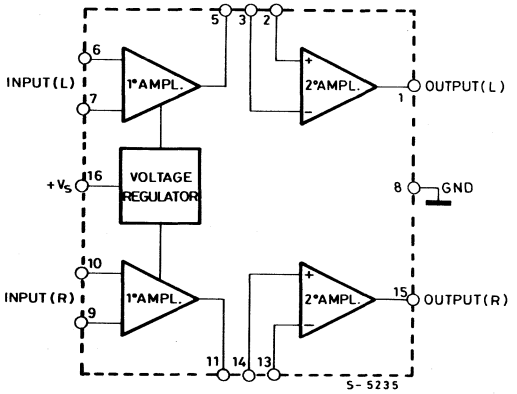



DIP




SO-16

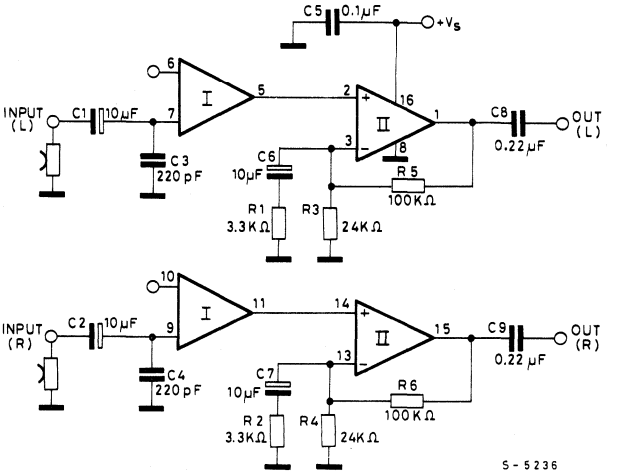
## BLOCK DIAGRAM (Pin numbers refer to the DIP)




| THERMAL DATA | | | DIP | SO-16 |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 150 °C/W | 200°C/W * |

* The thermal resistance is measured with the device mounted on a ceramic substrate (25 x 16 x 0.6 mm).

Fig. 1 - Test circuit




**Note:** Pin numbers refer to DIP.

Fig. 2 - P.C. board and components layout of the circuit of fig. 1 (1:1 scale)

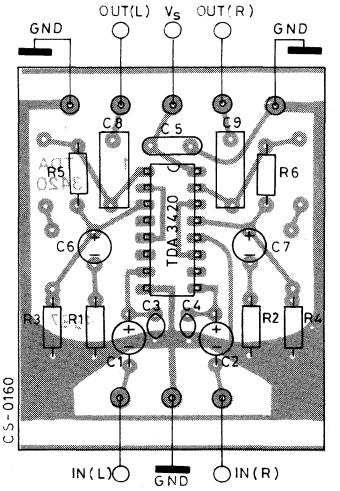
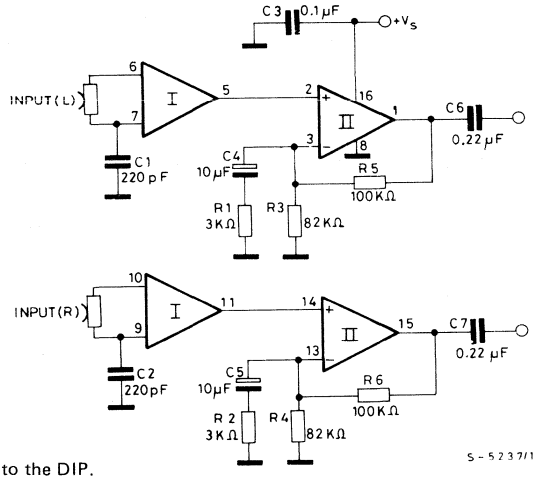


Fig. 3 - Test circuit without input capacitors




**Note:** Pin numbers refer to the DIP.

**ELECTRICAL CHARACTERISTICS** ($T_{amb}$= 25°C, $V_s$= 14.4V, $G_v$= 60 dB refer to the test circuit of fig. 1, unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_s$ | Supply current | $V_s$= 8V to 20V | | | 8 | | mA |
| $I_o$ | Output current | Source | $V_s$= 8V to 20V | | 10 | | mA |
| | | Sink | | | 1 | | mA |
| $G_v$ | Gain | f = 1 KHz | | | 60 | | dB |
| $R_i$ | Input resistance | | | 50 | 100 | | KΩ |
| $R_o$ | Output resistance | | | | 50 | | Ω |
| THD | Total harmonic distortion without noise | $V_o$= 300 mV | f = 1 KHz | | 0.05 | | % |
| | | | f = 10 KHz | | 0.05 | | % |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_o$ | Peak to peak output voltage | f = 40 Hz to 15 KHz | | 12 | | V |
| $e_n$ | Total input noise (°) | $R_s$= 50 Ω<br>$R_s$= 600 Ω<br>$R_s$= 5 KΩ | | 0.25<br>0.4<br>1.3 | 0.7 | μV<br>μV<br>μV |
| S/N | Signal to noise ratio (°) | $V_{in}$= 0.3 mV $R_s$= 600 Ω<br>$V_{in}$= 1 mV $R_s$= 0 | | 57<br>73 | | dB |
| | (°°) | $V_{in}$= 0.3 mV $R_s$= 600 Ω<br>$V_{in}$= 1 mV $R_s$= 0 | | 55<br>71 | | dB |
| CS | Channel separation | f = 1 KHz | | 60 | | dB |
| SVR | Supply voltage rejection (°°°) | f = 1 KHz $R_s$= 600 Ω | | 110 | | dB |

(°) Weighting filter : curve A.
(°°) Weighting filter : Dolby CCIR/ARM.
(°°°) Referred to the input.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit of fig. 1, $V_s$= 14.4V)

### AMPLIFIER N° 1

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $G_v$ | Gain (pin 6 to pin 5) | | 27.5 | 28.5 | 29 | dB |
| d | Distortion | $V_o$= 300 mV f = 1 KHz<br>f = 10 KHz | | 0.05<br>0.05 | | % |
| $e_n$ | Total input noise (°) | $R_s$= 600Ω | | 0.4 | | μV |
| $Z_o$ | Output impedance (pin 5) | f = 1 KHz | | 100 | | Ω |
| $I_o$ | Output current (pin 5) | | | 1 | | mA |
| V5 | DC output voltage (pin 5) | Test circuit fig. 3 | | 2.8 | | V |
| | | Test circuit fig. 1 | 1.0 | 1.5 | | |

(°) Weighting filter: curve A.

## ELECTRICAL CHARACTERISTICS (continued)

### AMPLIFIER N° 2

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $G_v$ | Open loop voltage gain | | | 100 | | dB |
| $I_B$ | Input bias current | | | 0.2 | | μA |
| $V_{os}$ | Input offset voltage | | | 2 | | mV |
| $I_{os}$ | Input offset current | | | 50 | | nA |
| $e_n$ | Total input noise (°) | $R_s$= 600Ω | | 2 | | μV |
| $R_i$ | Input impedance | f = 1 KHz (open loop) | 150 | 500 | | KΩ |

(°) Weighting filter: curve A.

Fig. 4 - Total input noise vs. source resistance (curve A)

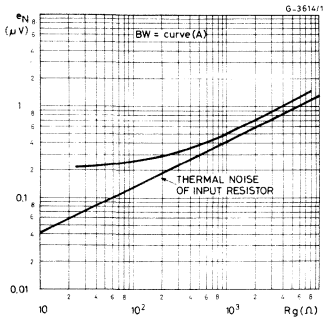



Fig. 5 - Total input noise vs. source resistance(BW=22Hz to 22 KHz)

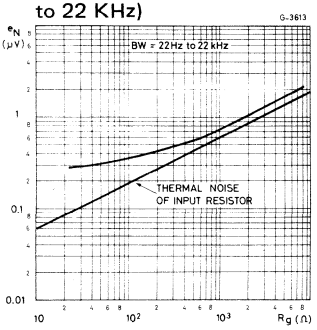



Fig. 6 - Total harmonic distortion vs. output voltage

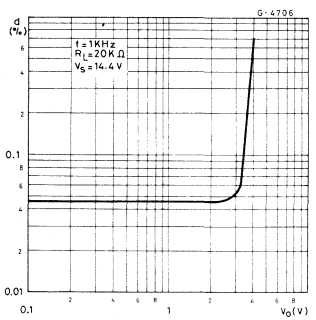



Fig. 7 - Output voltage vs. frequency

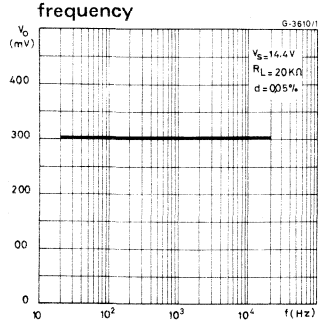



Fig. 8 - Distortion vs. input level (test circuit of fig. 1)

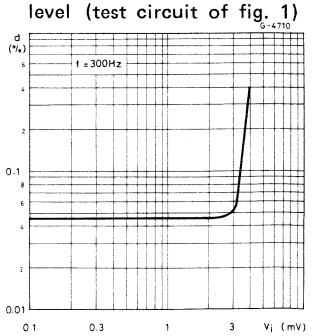



Fig. 9 - Frequency response of the circuit of fig. 10

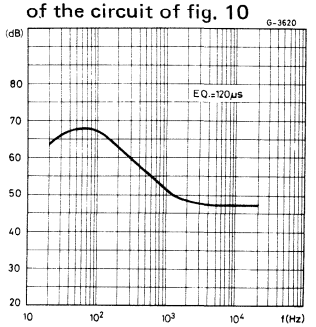


Fig. 10 - Very low noise stereo preamplifier for cassette players

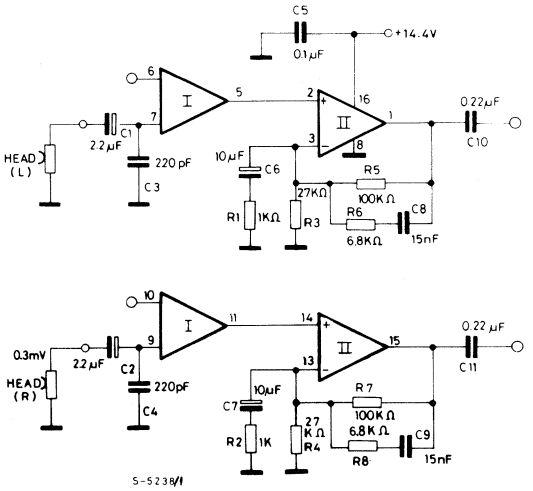
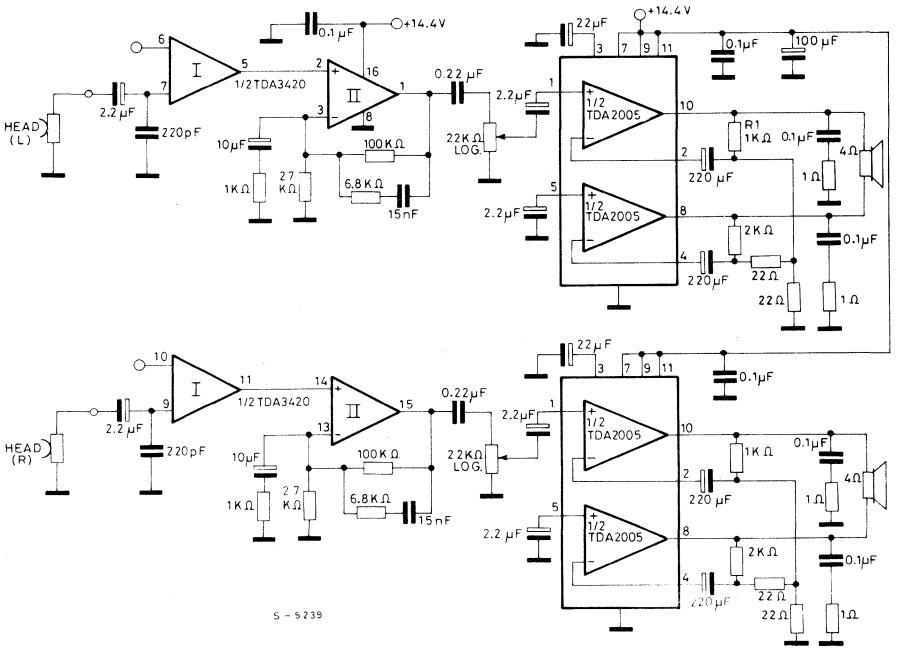



Fig. 11 - Complete 20 + 20W stereo tape playback system



# LINEAR INTEGRATED CIRCUITS

**TDA4092**

## 5 BIT BINARY TO 7-SEGMENT DECODER DRIVER

- ROM MASK OPTION
- STANDARD CONFIGURATION FOR 2 DIGIT 7-SEGMENT LED TO PRESENT THE NUMBERS 1 TO 32
- CONSTANT CURRENT OUTPUT STAGES FOR DIRECT DRIVING OF COMMON ANODE LEDs
- OUTPUT PROVIDED TO DISPLAY THE STAND-BY MODE
- $\overline{AV}$ OUTPUT ACTIVATED WHENEVER PROGRAM 32 IS SELECTED
- TTL COMPATIBLE INPUTS
- 5V SUPPLY VOLTAGE

The TDA 4092 is a monolithic integrated circuit designed to display the program number (1 to 32) in TV or Radio sets in conjunction with voltage or frequency synthesizers. The inputs accept a 5 bit binary code with TTL levels and have internal pull-up.
The outputs can directly drive LED display elements with common anode.
One of these outputs is intended to display the stand-by mode of the set.
No external resistors are required if the LEDs are supplied at 5V.
The LEDs can also be supplied with higher voltage (up to 18V) but in this case a single resistor in series with the LED elements must be used in order to limit the power dissipation of the IC; moreover, a suitable $R_{ext}$ must be chosen.
The circuit is produced in $I^2L$ technology and is available in a 24 pin dual in-line plastic package.

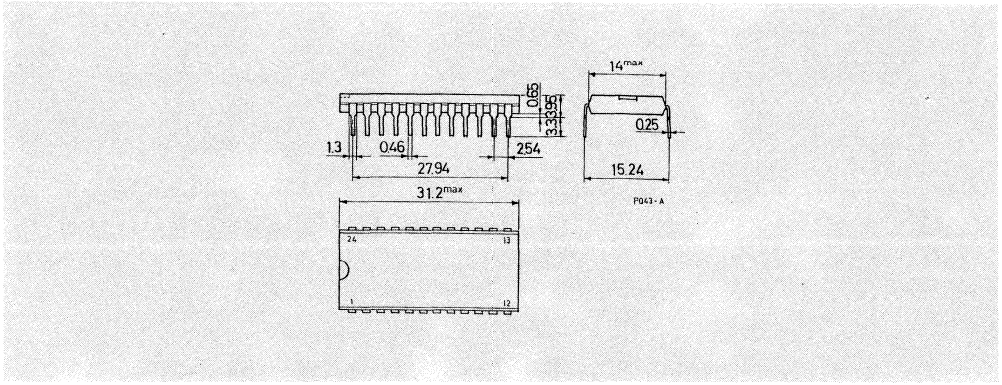
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 10 | V |
| $V_I$ | Input voltage | 10 | V |
| $V_{O\,(off)}$ | Off state output voltage | 20 | V |
| $I_{OL}$ | Output current | 22 | mA |
| $P_{tot}$ | Total power dissipation at $T_{amb}$ = 55°C | 0.8 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -25 to 150 | °C |
| $T_{op}$ | Operating temperature | 0 to 70 | °C |

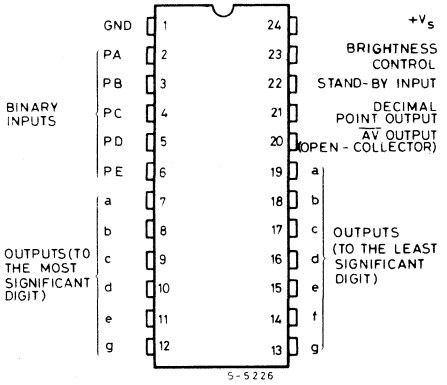
**ORDERING NUMBER:** TDA 4092

## MECHANICAL DATA

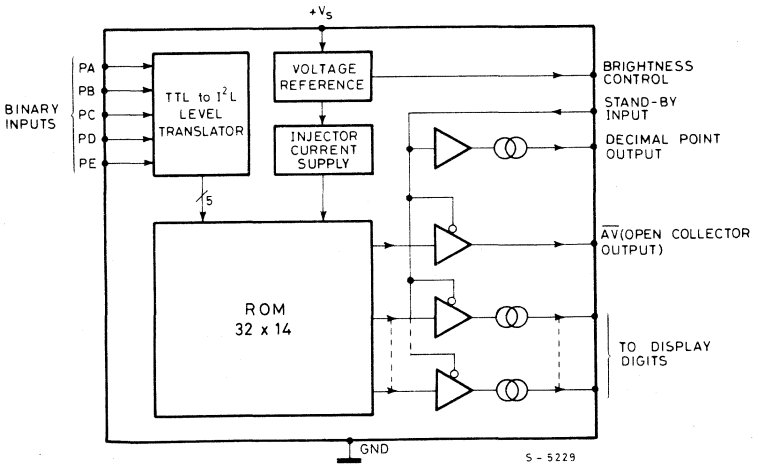
Dimensions in mm



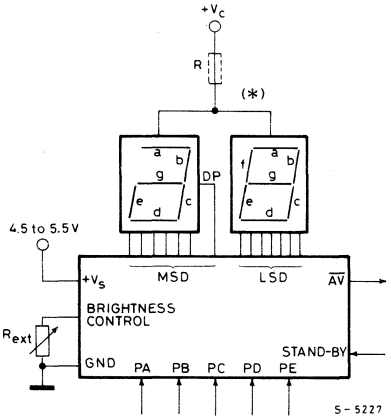
## CONNECTION DIAGRAM (top view)




## BLOCK DIAGRAM



## APPLICATION CIRCUIT




(*) R is necessary only with $V_c$ greater than 5.5V.

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction ambient | max | 120 | °C/W |

## ELECTRICAL CHARACTERISTICS ($V_s$= 5V, $T_{amb}$= 25°C unless otherwise specified)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | | 4.5 | | 5.5 | V |
| $I_s$ | Quiescent supply current | $V_s$= 5.5V | | | 20 | 28 | mA |
| $V_{IH}$ | High level input voltage | $T_{amb}$= 0 to 70°C | | 2 | | | V |
| $V_{IL}$ | Low level input voltage | $T_{amb}$= 0 to 70°C | | | | 0.8 | V |
| $I_{IH}$ | High level input current | $T_{amb}$= 0 to 70°C, $V_s$ = 5.5V | $V_{IH}$= 2V | | | -30 | μA |
| $I_{IL}$ | Low level input current | | $V_{IL}$= 0.8V | | -50 | -200 | μA |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{out}$ | Output voltage | $I_o$= 15 mA | 2 | | | V |
| $V_{AV}$ | AV output voltage (pin 20) | (All the binary inputs high)<br>$I_{AV}$= 1.6 mA | | 50 | 260 | mV |
| $I_B$ | Pin 23 input current (Brightness control) | $R_{ext}$= 3.3 KΩ | | -375 | | μA |
| | | $R_{ext}$= 5.6 KΩ | | -225 | | |
| $I_o$ | Output current (*) | $R_{ext}$= 3.3 K | 13.5 | 15 | 16.5 | mA |
| | | $R_{ext}$= 5.6 K | 8 | 9 | 10 | |
| $I_{DP}$ | Output current for decimal point (pin 21)(**) | | | 12.5 | | mA |
| $\frac{\Delta I_o}{I_o}$ /$\Delta V_s$ | Segment current stability | $I_o$ = 15 mA<br>$V_s$= 4.5 to 5.5V | | 0.2 | | % |

(*) $I_o = 40 \cdot I_B$

(**) $I_{DP}$ is fixed and independent of $R_{ext}$ value.

## FUNCTION TABLE

| INPUTS | | | | | | Number displayed | OUTPUTS | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | ten's digit (MSD) | | | | | | unit's digit (LSD) | | | | | | | DP | $\overline{AV}$* |
| A | B | C | D | E | Standby | | a | b | c | d | e | g | a | b | c | d | e | f | g | | |
| L | L | L | L | L | L | 1 | | | | | | | | on | on | | | | | | |
| H | L | L | L | L | L | 2 | | | | | | | on | on | | on | on | | on | | |
| L | H | L | L | L | L | 3 | | | | | | | on | on | on | on | | | on | | |
| H | H | L | L | L | L | 4 | | | | | | | | on | on | | | on | on | | |
| L | L | H | L | L | L | 5 | | | | | | | on | | on | on | | on | on | | |
| H | L | H | L | L | L | 6 | | | | | | | on | | on | on | on | on | on | | |
| L | H | H | L | L | L | 7 | | | | | | | on | on | on | | | | | | |
| H | H | H | L | L | L | 8 | | | | | | | on | on | on | on | on | on | on | | |
| L | L | L | H | L | L | 9 | | | | | | | on | on | on | on | | on | on | | |
| H | L | L | H | L | L | 10 | | on | on | | | | on | on | on | on | on | on | | | |
| L | H | L | H | L | L | 11 | | on | on | | | | | on | on | | | | | | |
| H | H | L | H | L | L | 12 | | on | on | | | | on | on | | on | on | | on | | |
| L | L | H | H | L | L | 13 | | on | on | | | | on | on | on | on | | | on | | |
| H | L | H | H | L | L | 14 | | on | on | | | | | on | on | | | on | on | | |
| L | H | H | H | L | L | 15 | | on | on | | | | on | | on | on | | on | on | | |
| H | H | H | H | L | L | 16 | | on | on | | | | on | | on | on | on | on | on | | |
| L | L | L | L | H | L | 17 | | on | on | | | | on | on | on | | | | | | |
| H | L | L | L | H | L | 18 | | on | on | | | | on | on | on | on | on | on | on | | |
| L | H | L | L | H | L | 19 | | on | on | | | | on | on | on | on | | on | on | | |
| H | H | L | L | H | L | 20 | on | on | | on | on | on | on | on | on | on | on | on | | | |
| L | L | H | L | H | L | 21 | on | on | | on | on | on | | on | on | | | | | | |
| H | L | H | L | H | L | 22 | on | on | | on | on | on | on | on | | on | on | | on | | |
| L | H | H | L | H | L | 23 | on | on | | on | on | on | on | on | on | on | | | on | | |
| H | H | H | L | H | L | 24 | on | on | | on | on | on | | on | on | | | on | on | | |
| L | L | L | H | H | L | 25 | on | on | | on | on | on | on | | on | on | | on | on | | |
| H | L | L | H | H | L | 26 | on | on | | on | on | on | on | | on | on | on | on | on | | |
| L | H | L | H | H | L | 27 | on | on | | on | on | on | on | on | on | | | | | | |
| H | H | L | H | H | L | 28 | on | on | | on | on | on | on | on | on | on | on | on | on | | |
| L | L | H | H | H | L | 29 | on | on | | on | on | on | on | on | on | on | | on | on | | |
| H | L | H | H | H | L | 30 | on | on | on | on | | on | on | on | on | on | on | on | | | |
| L | H | H | H | H | L | 31 | on | on | on | on | | on | | on | on | | | | | | |
| H | H | H | H | H | L | 32 | on | on | on | on | | on | on | on | | on | on | | on | | on |
| X | X | X | X | X | H | none | | | | | | | | | | | | | | on | ** |

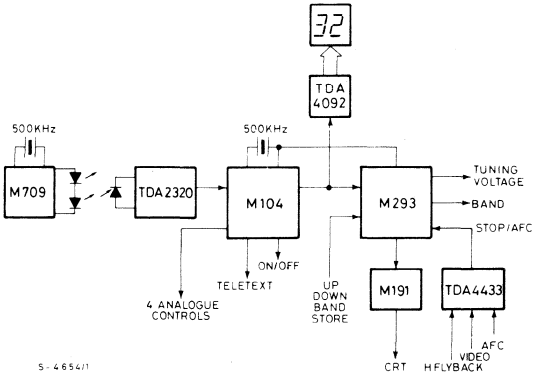
H = High L = Low X = Don't care

* $\overline{AV}$: open collector output.

** $\overline{AV}$ output is "on" whenever the input bits are all high, regardless of the standby input.

## APPLICATION INFORMATION

Fig. 1 - Remote controlled voltage synthesizer (up to 32 stations) for TV and radio

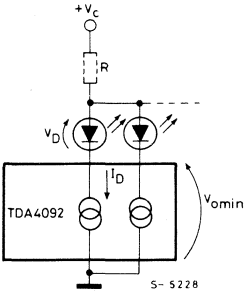



When operating with a supply voltage higher than 5.5V for LED elements, it is necessary to limit the IC power dissipation by means of one external resistance connected in series with the common point of the digits (R in fig. 2).
Unused outputs must be connected to $V_s$ taking into account the additional power dissipation.
The value of R must be chosen taking into account the worst working conditions.
The maximum number of ON segments is 12 (number 28 displayed), so,

$$R = \frac{V_C - V_D - V_{out\ min}}{12 \cdot I_D}$$

$I_D$, depending on $R_{ext}$ (see Table of Electrical characteristics), can be fixed to the most suitable value to minimize the power dissipation in the IC. Since the worst condition for the device is with seven outputs active, it follows that:

Fig. 2 - Schematic diagram for LED driving.




| | |
|---|---|
| $P_{d\ out} = 7 \cdot I_D\ (V_C - V_D - 7R \cdot I_D)$ | Power dissipation in the output stage |
| $P_d = V_s \cdot I_{s\ max}$ | Power drained from the supply |
| $P_{tot} = P_{d\ out} + P_D$ | Total power dissipation |

$P_{tot}$ must not exceed the Absolute Maximum Ratings of 800 mW, at $T_{amb} = 55°C$.
Otherwise the maximum operating ambient temperature can be fixed by:

$$T_{amb\ max} = T_{j\ max} - R_{th\ j\text{-}amb}\ P_{tot}$$

**Example:**

$V_c = 18V$; $I_D = 10$ mA (fixed by means of $R_{ext} = 5.6\ K\Omega$); $V_{out\ min} = 2V$; $I_{s\ max} = 28$ mA; $T_{j\ max} = 150°C$; $V_D = 2V$; $V_s = 5.5V$.

Applying the previous formulae, it follows that: $R \cong 120\Omega$; $P_{d\ out} = 0.532W$; $P_d = 0.154W$; $P_{tot} = 0.686W$; $T_{amb\ max} \cong 68°C$.

# LINEAR INTEGRATED CIRCUITS

**TDA4190**

**ADVANCE DATA**

## TV SOUND CHANNEL WITH DC CONTROLS

- INTERNAL VCR INPUT/OUTPUT SWITCHING
- 4W OUTPUT POWER INTO 16Ω
- NO SCREENING REQUIRED
- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- LOW DISTORTION
- DC TONE/VOLUME CONTROLS
- THERMAL PROTECTION

The TDA4190 is a complete TV sound channel with DC tone and volume controls plus an internally switched VCR input/output. Mounted in a Powerdip 16 + 2 + 2 package, the device delivers an output power of 4W into 16Ω (d = 10%, $V_s$ = 24V) or 1.5W into 8Ω (d = 10%, $V_s$ = 12V). Included in the TDA4190 are: IF amplifier limiter, active low-pass filter, AF preamplifier and power amplifier, turnoff muting, VCR switch, mute circuit and thermal protection.

High output, high sensitivity, excellent AM rejection and low distortion make the device suitable for use in TVs of almost every type. Further, no screening is necessary because the device is free of radiation problems.

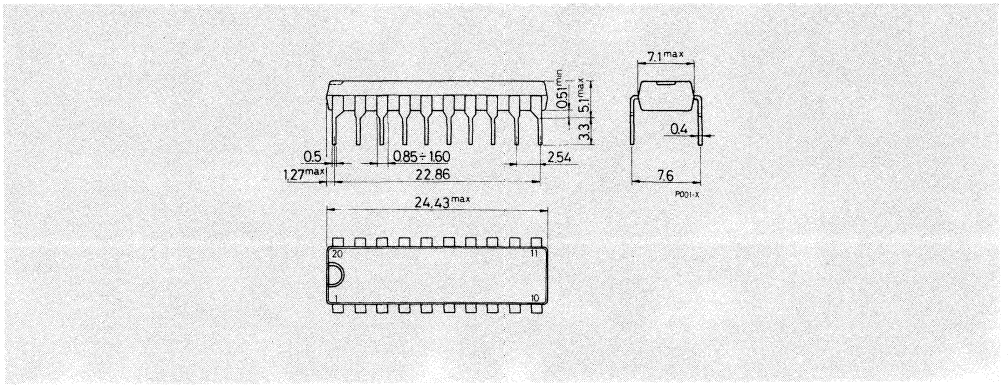
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 18) | 28 | V |
| $V_I$ | Voltage at pin 1 | ± $V_s$ | |
| $V_i$ | Input voltage (pin 2) | 1 | Vpp |
| $I_o$ | Output peak current (repetitive) | 1.5 | A |
| $I_o$ | Output peak current (non repetitive) | 2 | A |
| $I_4$ | Current (pin 4) | 10 | mA |
| $P_{tot}$ | Power dissipation at $T_{pins}$ = 90°C | 4.3 | W |
| | at $T_{amb}$ = 70°C | 1 | W |
| $T_{stg}$-$T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA4190

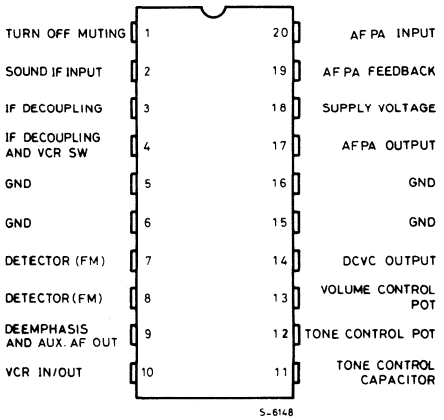
## MECHANICAL DATA

Dimensions in mm

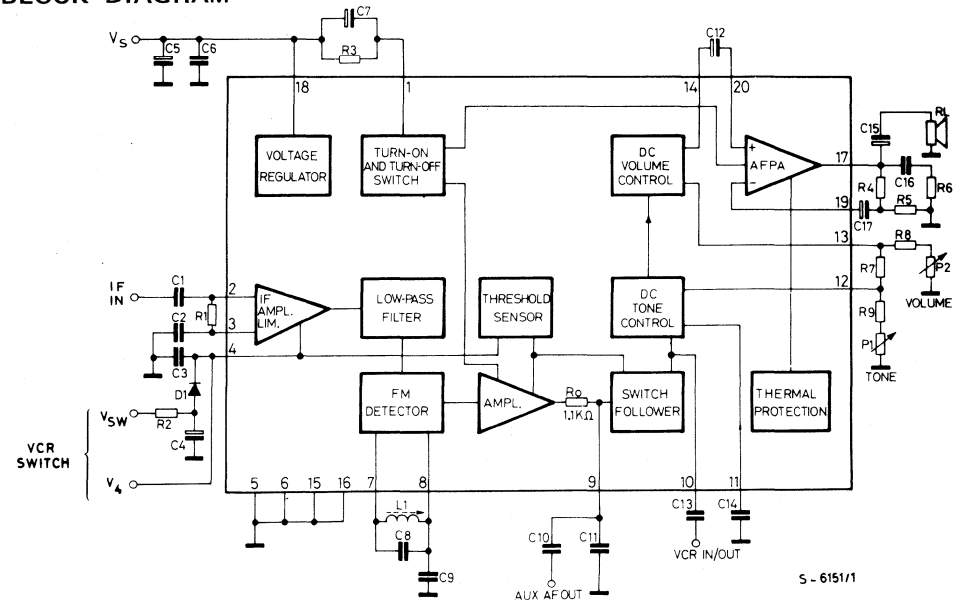


# TDA4190

## CONNECTION DIAGRAM




## BLOCK DIAGRAM




## THERMAL DATA

| | | |
|---|---|---|
| $R_{th\ j\text{-}pins}$ | Thermal resistance junction-pins | max 14 °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max 80 °C/W* |

(*) Obtained with GND pins soldered to printed circuit with minimized copper area.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s$= 24V, $V_{sw}$= 2V or no $V_4$, $\Delta f$= ±25 KHz, $R_L$= 16Ω, $V_i$= 1mV, $P_1$= 12 KΩ, $f_o$= 4.5 MHz, $f_m$= 400 Hz, $T_{amb}$= 25°C, unless otherwise specified)

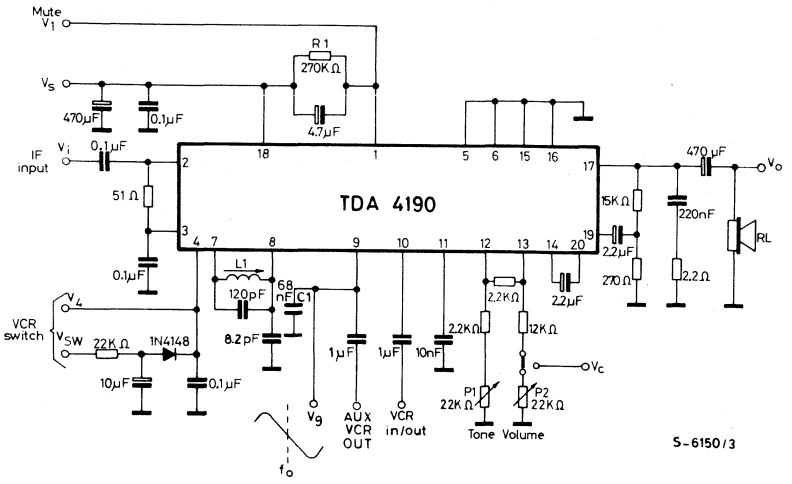
| Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| $V_s$ Supply voltage (pin 18) | $P_2$ = 12 KΩ | 10.8 | | 27 | V |
| $V_o$ Quiescent output voltage (pin 18) | $P_2$ = 12 KΩ | 11 | 12 | 13 | V |
| $V_1$ Pin 1 DC Voltage | $P_2$ = 12 KΩ $R_1$= 270 KΩ | | 5.3 | | V |
| $V_4$ Pin 4 DC voltage | $P_2$ = 12 KΩ | | 3.2 | | V |
| $I_d$ Quiescent drain current | $P_2$ = 12 KΩ | | 32 | | mA |
| **IF AMPLIFIER AND DETECTOR** | | | | | |
| $V_{i\ (threshold)}$ Input limiting voltage at pin 2 (-3 dB) | $V_o$ = 4 $V_{rms}$ | | 50 | 100 | μV |
| $V_9$ Recovered audio voltage (pin 9) | $\Delta f$ = ± 7.5 KHz $P_2$ = 12 KΩ | 140 | 200 | 280 | mV |
| AMR Amplitude modulation rejection (*) | m= 0.3; $V_I$= 1 mV; $V_o$= 4 $V_{rms}$ | | 60 | | dB |
| $R_i$ Input resistance (pin 2) | $\Delta f$ = 0 $P_2$ = 12 KΩ | | 30 | | KΩ |
| $C_i$ Input capacitance (pin 2) | $\Delta f$ = 0 $P_2$ = 12 KΩ | | 6 | | pF |
| $R_9$ Deemphasis resistance | $C_1$ = 68 to 888 nF | 0.75 | 1.1 | 1.5 | KΩ |
| **DC VOLUME CONTROL** | | | | | |
| $K_v$ Volume attenuation (resistance control) | $P_2$ = 0Ω<br>$P_2$ = 4.3 KΩ<br>$P_2$ = 12 KΩ | 20 | 0<br>26<br>88 | 32 | dB<br>dB<br>dB |
| $V_c$ Control voltage | K = 0 dB<br>K = 26 dB<br>K = 88 dB | | 0<br>1.3<br>2.6 | | V<br>V<br>V |
| $\frac{\Delta K_v}{\Delta T_{pins}}$ Volume attenuation thermal drift (resistance control) | $T_{pins}$ 25 to 85°C<br>$P_2$= 4.3 KΩ | | -0.05 | | $\frac{dB}{°C}$ |
| **DC TONE CONTROL** | | | | | |
| $K_T$ Tone cut | $V_{sw}$ = 8V or $V_4$ = 2V<br>$V_{10}$ = 200 mV<br>$P_1$ = 12 KΩ to 100 Ω<br>f = 10 KHz | | 14 | | dB |

## ELECTRICAL CHARACTERISTICS (Continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AUDIO FREQUENCY AMPLIFIER** | | | | | | |
| $P_o$ | Output power (d = 10%) | $V_s$ = 24V $R_L$ = 16Ω<br>$V_s$ = 12V $R_L$ = 8Ω | 3.5 | 4.1<br>1.5 | | W<br>W |
| B | Frequency response of audio amplifier (-3dB) | $P_o$ = 1W $R_L$ = 16Ω<br>$V_{sw}$ = 8V or $V_4$ = 2V<br>$V_{10}$ = 200mV $V_o$=4Vrms@400Hz | 15 | 50 | | KHz |
| SVR | Supply voltage rejection | $P_2$ = 12KΩ Δf= o $f_{ripple}$ = 120Hz | | 26 | | dB |
| **V.C.R.** | | | | | | |
| $V_4$ | Input switching voltage<br>for recording<br>for playback | | | floating | | |
| | | | | | 2 | V |
| $V_{sw}$ | Input switching voltage<br>for recording<br>for playback | | | | 2 | V |
| | | | 8 | | | V |
| $V_{10}$ | Input voltage (playback) | $V_4$ = 2V or $V_{sw}$ = 8V<br>$V_o$ = $4V_{rms}$ $P_2$ = o | 50 | 70 | 100 | mV |
| $V_{10}$ | Output voltage (recording) | $P_2$ = 12KΩ Δf = ±7.5KHz | 140 | 200 | 280 | mV |
| $R_{10}$ | Input resistance (playback) | $V_4$ = 2V or $V_{sw}$ = 8V | 10 | | | KΩ |
| $R_{10}$ | Output resistance (recording) | Δf = ± 7.5KHz, no $V_4$ or $V_{sw}$ = 2V | | | 100 | Ω |
| d | Total harmonic distortion of pin 10 output signal | Δf = ± 7.5KHz $V_i$ = 1mV | | 0.5 | | % |
| d | Total harmonic distortion for 20dB overload of $V_{10}$ | $V_4$ = 2V $V_{sw}$ = 8V<br>$V_{10}$ = $1V_{rms}$ $V_o$ = $4V_{rms}$ | | 0.5 | 2 | % |
| SVR | Supply voltage rejection at output pin 10 | Δf = 0 $f_{ripple}$ = 120Hz $P_2$ = 12KΩ | | 66 | | dB |
| $\frac{S+N}{N}$ | Signal and noise to noise ratio at output pin 10 | Δ f = ± 25KHz $V_i \geq$ 1mV | | 70 | | dB |
| **OVERALL CIRCUIT** | | | | | | |
| $\frac{S+N}{N}$ | Signal to noise ratio (*) | $V_i \geq$ 1mV $V_o$ = $4V_{rms}$<br>Δf = 0 | | 70 | | dB |
| d | Distortion (*) | $P_o$ = 50mW Δf = ± 7.5Hz<br>$V_s$ = 24V $R_L$ = 16Ω<br>$V_s$ = 12V $R_L$ = 8Ω | | 0.5<br>0.5 | | %<br>% |
| M | Muting (*) | $V_o$ = $4V_{rms}$ @ no $V_1$; $V_1$ = 0 | 100 | | | dB |
| Δf | | $P_2$ = 0 $V_o$ = $4V_{rms}$ | | 3 | 6 | KHz |

* Test bandwidth = 20 KHz.

## TEST CIRCUIT




## TEST CONDITIONS (unless otherwise specified)

$V_s$ = 24V; $V_{SW}$ = 2V or no $V_4$; $R_L$ = ∞;
$V_{in}$ = 1 mV; $Q_o$ = 60; $f_o$ = 4.5 MHz;
$P_1$ = 12 KΩ; $f_m$ = 400 Hz; Δf = ± 25 KHz.

Fig. 1 - Relative audio output voltage and output noise vs. input signal.

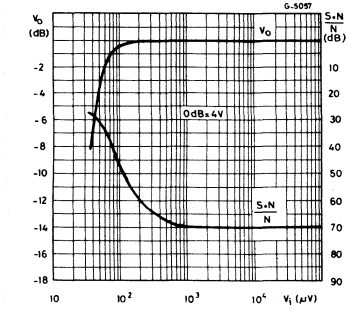



Fig. 2 - Output voltage alternation vs. DC volume control resistance (a) or Vs. DC volume control voltage (b)

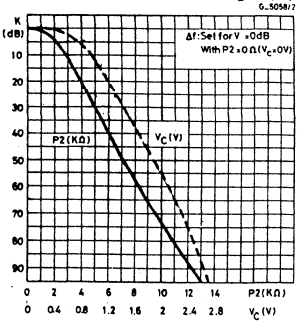



Fig. 3 - DC tone control cut of the high audio frequencies for some values of resistance adjusted by P1.

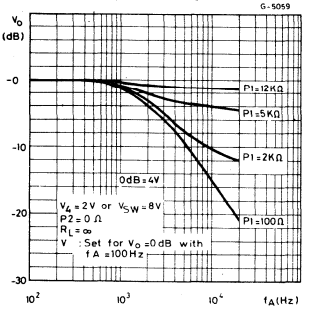


Fig. 4 - Amplitude modulation rejection vs. input signal.

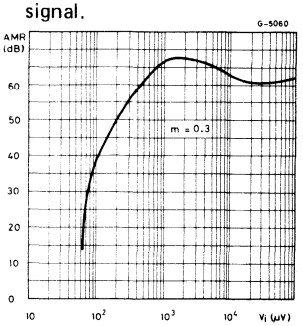



Fig. 5 - ΔAMR vs. timing frequency change

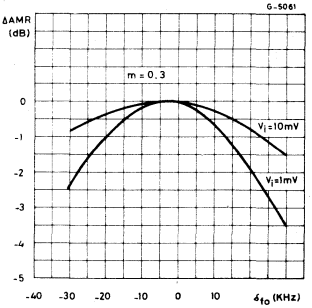



Fig. 6 - Recovered audio voltage vs. unloaded Q-factor of the detector coil

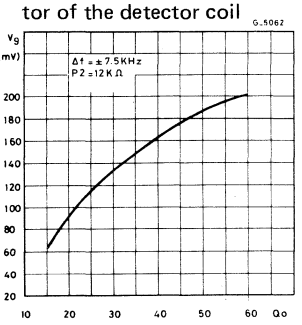



Fig. 7 - Distortion vs. unloaded Q-factor of the detector coil.

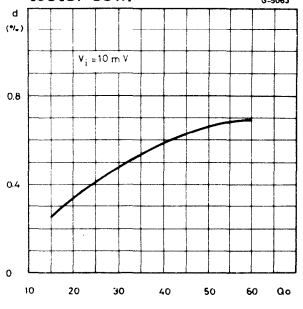



Fig. 8 - Distortion vs. frequency variation

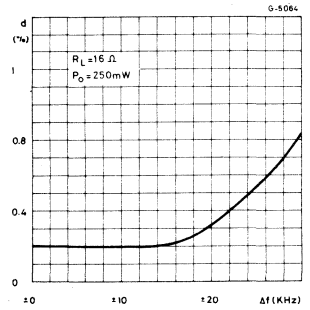



Fig. 9 - Distortion vs. tuning frequency change

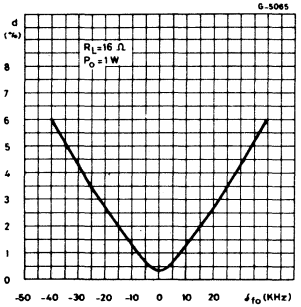



Fig. 10 - Distortion vs. output power

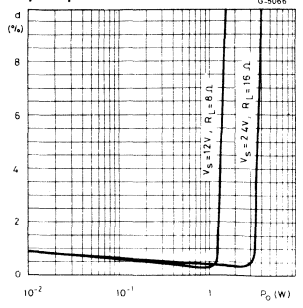



Fig. 11 - Audio amplifier frequency response

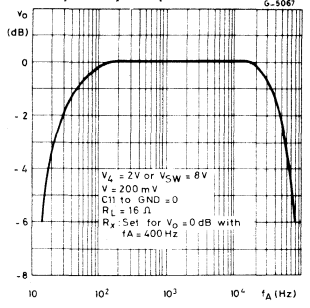



Fig. 12 - Output power vs. supply voltage.

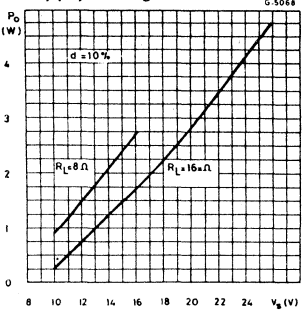


Fig. 13 - Power dissipation vs. supply voltage (sine wave operation).

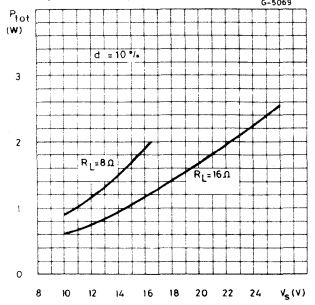



Fig. 14 - Power dissipation and efficiency vs. output power

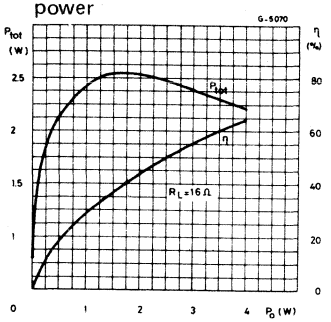
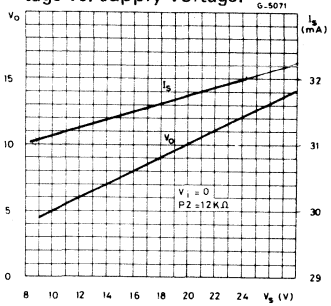



Fig. 15 - Quiescent drain and quiescent output voltage vs. supply voltage.




## APPLICATION INFORMATION (Refer to the block diagram)

### IF Amplifier-limiter

It is made by six differential stages of 15dB gain each so that an open loop gain of 90dB is obtained.

While a unity DC gain is provided, the AC closed loop gain is internally fixed at 70dB that allows a typical input sensitivity of 50 $\mu$V.

The differential output signal is single ended by a 20dB gain amplifier that through a buffer stage, feeds the detector system.

Internal diodes protect the inputs against overloads.

- Pin 2 if the IF non-inverting input
- Pin 3 is decoupled by a capacitor to open the AC loop
- Pin 4 grounded by a capacitor, allows a typical sensitivity of 50 $\mu$V. (See VCR facility too).

### Low-pass filter, FM detector and amplifier

The IF signal is detected by converting the frequency modulation into amplitude modulation and then detecting it.

Since the available modulated signal is a square wave, a 40dB/decade low-pass filter cuts its harmonics so that a sine wave can feed the two-resonances external network L1, C8 and C9.
This network defines the working frequency value, the amplitude of the recovered audio signal and its distortion at the highest frequency deviations.
The two resonances f1 (series resonance) and f2 (parallel resonance) can be computed respectively by:

$$X_{C9} = \frac{X_{L1} \cdot X_{C8}}{X_{L1} + X_{C8}} \text{ and } X_{L1} = X_{C8}$$

The ratio of these frequencies defines the peak-to-peak separation of the "S" curve:

$$\frac{f2}{f1} = \sqrt{1 + \frac{C_9}{C_8}}$$

## APPLICATION INFORMATION (continued)

A differential peak detector detects the audio frequency signal that amplified, reaches the deemphasis network R0; C11.

The AF amplifier can be muted (see turn-on and turn-off switch and VCR facility).

- Pin 7 is the output of the low-pass filter and one input of the differential peak detector
- Pin 8 is the other input of the differential peak detector
- Pin 9 is used to provide the required deemphasis time constant by grounding it with C11. At this pin, the internal impedance of which is typically of 1.1 KΩ, is available the recovered audio signal as auxiliary output.

### VCR Facility

The deemphathized AF signal reaches the switch follower block can provide to change the impedance of its output depending on the VCR function required.

The switch follower is driven by the threshold sensor block. This one switches both the amplifier and the switch follower by sensing the voltage at pin 4.

When no voltage is forced at pin 4 the function of pin 10 is of VCR output with low impedance; when the voltage at pin 4 is lower or higher than its quiescent value, the amplifier is muted and the impedance of pin 10 is switched to a high value for a proper VCR input operation.

Since pin 4 reaches also the inverting input of the If amplifier-limiter, this one can be switched off two for best insulation of the pin 10 with the TV signal path.

So, the VCR facility followd this truth table:

| Mode | $V_{sw}$ | or $V_4$ | Function of pin 10 | Impedance of pin 10 |
|---|---|---|---|---|
| Recording | $\leqslant$ 2V | no one | Output | $\leqslant$ 100Ω |
| Playback | $\geqslant$ 8V | $\leqslant$ 2V | Input | $\geqslant$ 10KΩ |

The output signal available when operating during recording is not dependent from both the volume and tone controls while, during playback, the input signal can be regulated by P1 and P2.

Pin 10, as input, can accept until 1VRMS of overload.

- Pin 4 is the VCR switch driver
- Pin 10 is the VCR input/output pin.

### DC Tone Control

The same signal available or applied to pin 10, after a voltage to current converter, reaches, the DC Tone Control block. It operates, inside the 10 KHz bandwidth, by cutting the high audio frequencies with a variable slope of an RC network, by means of $P_1$.

The maximum slope of the RC network is of 20dB per decade and its pole is defined by:

$X_{C11}$ = 6.8KΩ, tipically.

Pin 11 – At this pin is tied the tone capacitor

Pin 12 – is the DC Tone Control input.

## APPLICATION INFORMATION (continued)

### DC Volume Control

After tone control regulation, the AF current signal reaches the DC volume control block that controls its intensity. The normal control, for which the block has been designed for a narrow spread, is produced by P2; however, without P2, a voltage control can be operated by forcing a voltage at pin 13 through R8.

- Pin 12, already seen as a DCTC input, is the reference voltage for the DCVC. Because of this, a small interface between tone and volume regulation can be expected.
- Pin 13 is the DC volume control input.
- Pin 14 after a current to voltage converter, the audio frequency signal comes out at this pin.

### Audio Frequency power amplifier and thermal protection

Through C12 the signal reaches the amplifier non-inverting input. The closed loop gain is defined by the feedback at pin 19 (inverting input) or by the ratio:

$$G_v = 20 \text{ Log } \frac{R5 + R4}{R5} \text{ (dB)}$$

The amplifier, thermally protected, can supply 4W of power into a 16Ω load with 24V of supply voltage. The power output stage is a class B type.

- Pin 20 is the non-inverting input
- Pin 19 is the inverting input
- Pin 17 is the output of the AFPA.

### Turn-on and turn-off switch

This block has been mainly designed to avoid, turning on the TV set, that transients, produced by the vision output, can reach the speaker.

Moreover this block, together an optimized rise time and full time of the supply voltage $V_s$, can avoid any pop generally produced during the turn-on and the turn-off transients.

Turning on, pin 1 follows the supply voltage $V_s$ by means of C7; a threshold is reached and the muting of the AFPA output (pin 17) is suddenly produced.

When $V_s$ reaches it stop, C7 charges itself through the input impedance of pin 1 and the muting is removed with a time constant depending on the C7 value.

Turning off, the $V_s$ trend, in series to the voltage $V_s$-$V_1$ and which C7 is charged, drives pin 1 at a low level threshold and a sudden muting is produced again.

Since the turn-off can be operated with high output power, if the muting operates when the current through the inductance of the speaker is different from zero, a flyback is generated and then a small pop can be produced.

The flyback is clipped by integrated diodes.

The thresholds that produce the muting have been chosen in the way that 1Vpp of ripple on the supply voltage does not produce any switching.

By shorting pin 1 to ground through a 10 KΩ resistor the muting can be obtained.

- Pin 1 is the turn-on and turn-off muting input.

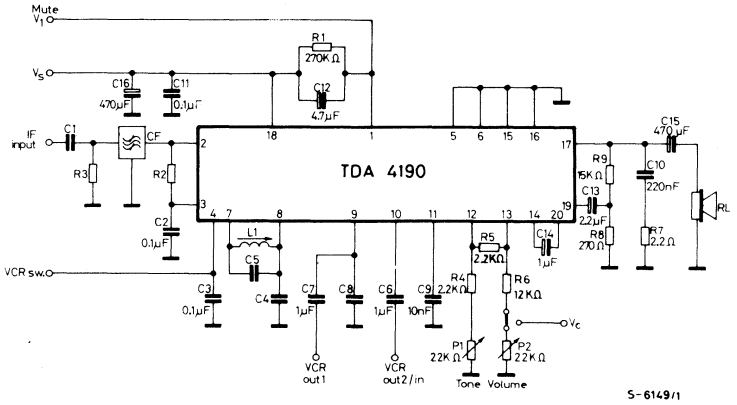
## APPLICATION INFORMATION (continued)

### Supply

An integrated voltage regulator with different output levels, supplies all the blocks operating with small signal.

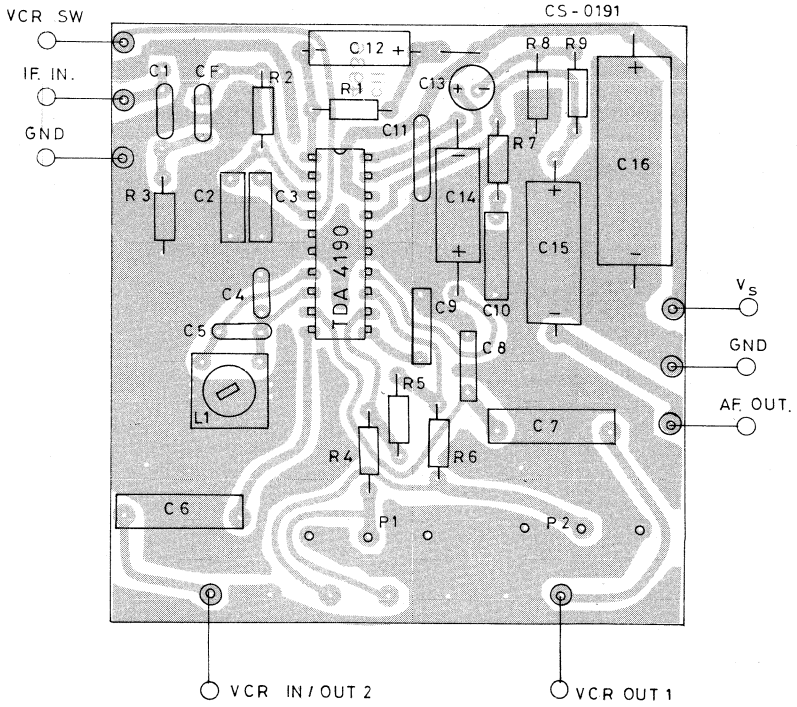
- Pin 18 is the main supply of the device.
- Pin 5; pin 6; pin 15 and pin 16 are the ground of the supply. These pins are used to drain out from the device the heat produced by the dissipated power.

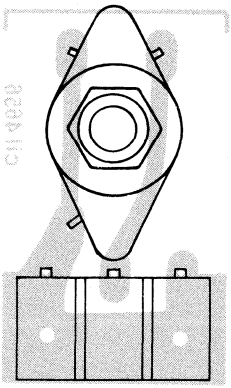
Fig. 16 - Application circuit



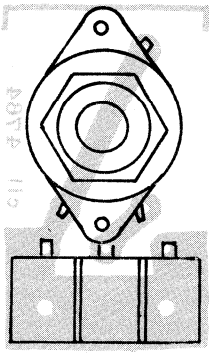

| Components | Units | Appl. 4.5 MHz | Appl. 5.5 MHz | Appl. 6 MHz |
|---|---|---|---|---|
| L1 | µH | 10<br>$Q_O$ = 60 | 12<br>$Q_O$ = 80 | 10<br>$Q_O$ = 70 |
| C5 | pF | 120 | 68 | 68 |
| C4 | pF | 9 | 8.2 | 6.8 |
| C8 | nF | 68 | 47 | 47 |
| C.F. | – | Murata SFE 4.5 MA | Murata SFE 5.5 MB | Murata SFE 6.0 MB |
| C1 | pF | 22 | 18 | 18 |
| R2 | Ω | 1000 | 560 | 470 |
| R3 | Ω | 1000 | 560 | 470 |

Fig. 17 - PC board and components layout of the circuit of fig. 16 (1:1 scale)



P1



P2

# TDA4420

# LINEAR INTEGRATED CIRCUITS

## VISION IF SYSTEM WITH AFC

- HIGH GAIN-HIGH STABILITY
- VERY LOW INTERMODULATION PRODUCTS
- MINIMUM DIFFERENTIAL ERROR
- CONSTANT INPUT IMPEDANCE INDEPENDENT OF AGC
- FAST AGC GATING-ACTION, LARGELY INDEPENDENT OF PULSE SHAPE AND AMPLITUDE
- ADJUSTABLE WHITE LEVEL
- LARGE AFC OUTPUT CURRENT SWING (PUSH-PULL OUTPUT)
- SWITCHABLE AFC

The TDA4420 is a monolithic integrated circuit in 18 lead dual in-line plastic package. The functions incorporated are:

- gain controlled vision IF amplifier
- video demodulator controlled by picture carrier
- AGC detector with gating facility
- AGC amplifier for tuner drive with variable delay
- phase comparator for AFC current generation
- electronic AFC switch, controlled by a DC threshold detector
- thermally compensated push-pull AFC output stage.

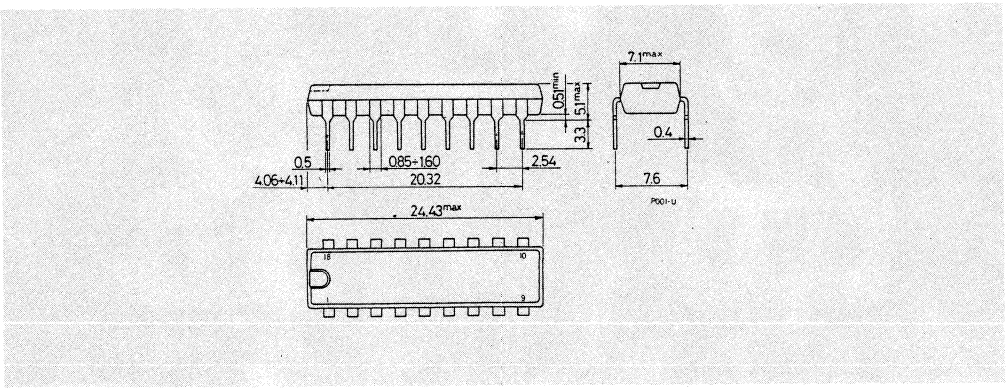
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 15) | 15 | V |
| $V_5$ | Voltage at pin 5 | 15 | V |
| $I_{13}$, $I_{14}$ | Video DC output current | 5 | mA |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 70°C$ | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

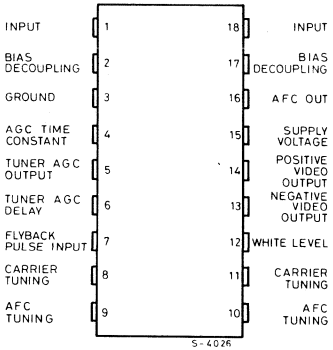
**ORDERING NUMBER:** TDA 4420

## MECHANICAL DATA

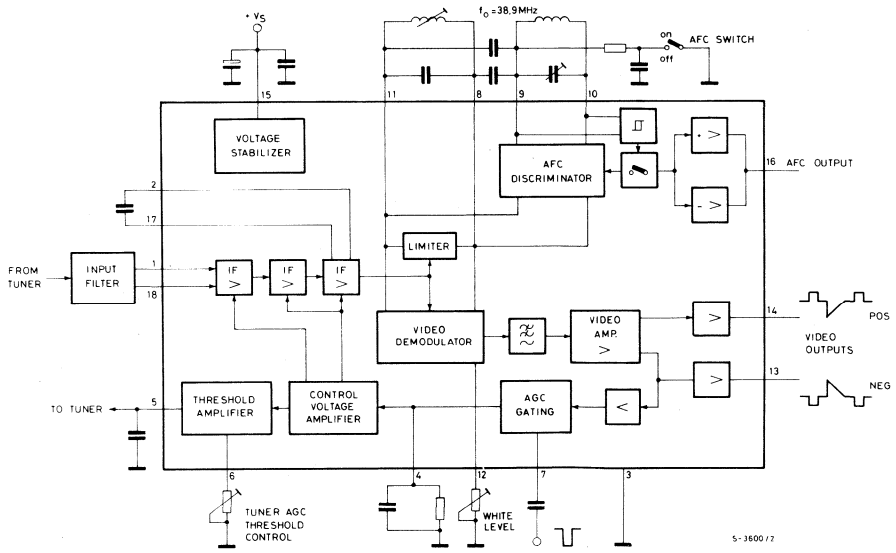
Dimensions in mm



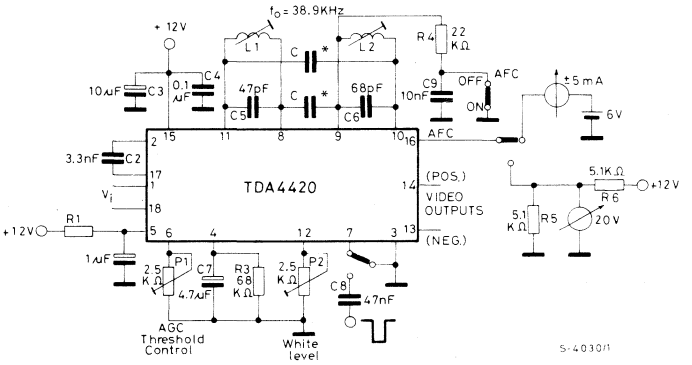
## CONNECTION DIAGRAM (top view)




## BLOCK DIAGRAM



## TEST CIRCUIT




Note: (*) C ≅ 1.5 pF (pin and lead capacitance).

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 80 | °C/W |

**ELECTRICAL CHARACTERISTICS** (Refer to the test circuit; $V_s$ = 12V, $f_o$ = 38.9 MHz; $P_1$ = 2.5 KΩ; pin 7 connected to GND; $P_2$ adjusted for $V_{13}$= 3.3Vpp; AFC off; $T_{amb}$= 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | | |
| $V_s$ | Supply voltage range (pin 15) | | 10 | 12 | 15 | V |
| $I_s$ | Supply current (pin 15) | | | 52 | | mA |
| $V_{14}$ | Video output DC voltage | $V_{13}$= 5.5V (1) | | 5.6 | | V |
| $V_{13}$ | Video output DC voltage | pin 12 open (1) | | | 4.5 | V |
| | | pin 12 grounded (1) | 7 | | | V |
| $V_{13}$ | Peak black clamping level at negative video output | | 1.75 | 1.9 | 2.15 | V |
| $I_{13}$ | Output DC current (pin 13) | $V_s$ = 15V $V_{13}$= 8V | | 1.6 | | mA |
| $I_9$, $I_{10}$ | DC control current for AFC off | | 150 | 300 | | μA |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **AC CHARACTERISTICS** | | | | | | |
| $I_5$ | Available tuner AGC current | (2) | | 10 | | mA |
| $V_7$ | AGC gating pulse input peak voltage | f pulse = 15625 Hz (3) | -1.5 | -3 | -5 | V |
| $V_o$ | Peak to peak video output signal (pin 13) | $V_{13}$= 5.5V (4), (5) | | 3.3 | | V |
| | | $V_{13}$= 6.4V (4), (5) | | 4.2 | | V |
| $\Delta V_i$ | AGC range | (6) | 50 | 60 | | dB |
| B | Frequency response (-3 dB) | (4) | 8 | 10 | | MHz |
| $V_i$ | Input sensitivity | (7), (8) | 100 | 150 | 200 | $\mu$V |
| $V_{13}$, $V_{14}$ | Video carrier and video carrier 2nd harmonic leakage at video output | $V_i$ = 30 dB $f_o$ = 38.9 MHz<br>(4) 2 $f_o$= 77.8 MHz | | | 30<br>50 | mV<br>mV |
| $V_{14}$ | Sound IF at positive video output (5.5 MHz) | (4), (9) | 30 | | | mV |
| d | Differential distortion of negative video output signal | $V_i$ = 30 dB (standard staircase modulating signal) | | 3 | | % |
| $d_{im}$ | Intermodulation product at video outputs (1.07 MHz) | (4), (10) | | -50 | | dB |
| $R_i$ | Input resistance between pins 1 and 18 | (4) | | 1.4 | | K$\Omega$ |
| $C_i$ | Input capacitance between pins 1 and 18 | | | 2 | | pF |
| $V_{16}$ | AFC voltage range | (11) | 1 | | $V_s$-1.5 | V |
| $I_{16}$ | Maximum available AFC current | (12) | | | ± 3 | mA |
| $\frac{\Delta I_{16}}{\Delta f}$ | AFC slope | (13) | | ±0.01 | | $\frac{mA}{KHz}$ |

**Notes:**

(1) $V_{13}$ and $V_{14}$ are simultaneously adjustable by means of the resistance connected between pin 12 and ground ($P_2$).
(2) $\Delta V_i$ = +60 dB (see note 7); $f_m$ = 100 KHz; m = 0.82.
(3) Input at pin 7 through C8.
(4) The input voltage $V_i$ can have any value within the AGC range.
(5) $P_2$ adjusted for $V_{13}$= 5.5V or $V_{13}$= 6.4V; $f_m$= 100 KHz; m = 0.82.
(6) $\Delta V_o$ = 1 dB; $f_m$= 100 KHz; m = 0.82.

(7) The measured amplitude is assumed as 0 dB reference level of $V_i$ that is the rms value of the unmodulated video carrier (modulation down).

(8) $P_2$ is adjusted in order to have $V_{13}$= 3Vpp at $V_i$ = 4 mV, then the sensitivity is obtained as the minimum input voltage that maintains this output level. $f_m$= 100 KHz; m = 82%.

(9) $f_o$= 38.9 MHz (video carrier); $f_a$ = 33.4 MHz (sound carrier); the amplitude of the sound carrier is 30 dB below the amplitude of the video carrier.

(10) $V_i$ at $f_o$ = 38.9 MHz (video carrier); $f_a$ = 33.4 MHz, 6 dB below $V_i$ (sound carrier); $f_b$ = 34.47 MHz, 24 dB below $V_i$ (Chroma subcarrier).

(11) $V_i$ = 40 dB; $R_5$ = $R_6$ = 5.1 KΩ; AFC on; $f_o$ = 39.9 MHz; $f_o$ = 37.9 MHz.

(12) $V_i$ = 40 dB; $f_o$ = 39.2 MHz; AFC on; $V_{16}$= 6V.

(13) $V_i$ = 40 dB; $f_o$ = 38.9 MHz; $f_2$ = 39.2 MHz; AFC on; $V_{16}$= 6V.

Fig. 1 - Set-up for measurement of $d_{im}$

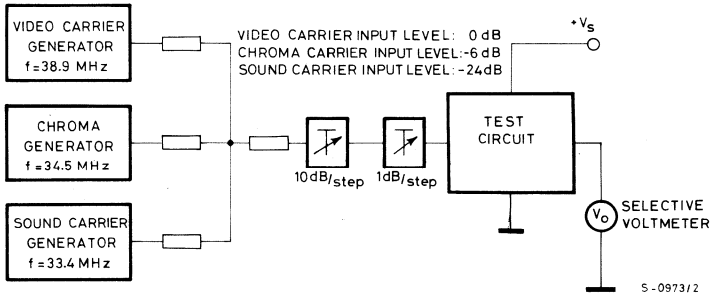
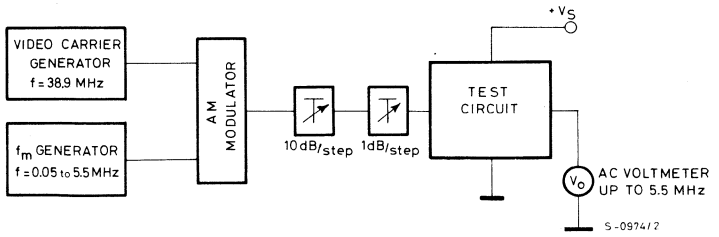
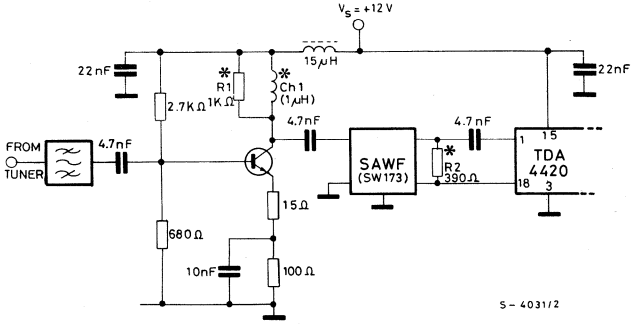



Fig. 2 - Set-up for measurement of $\Delta V_o$



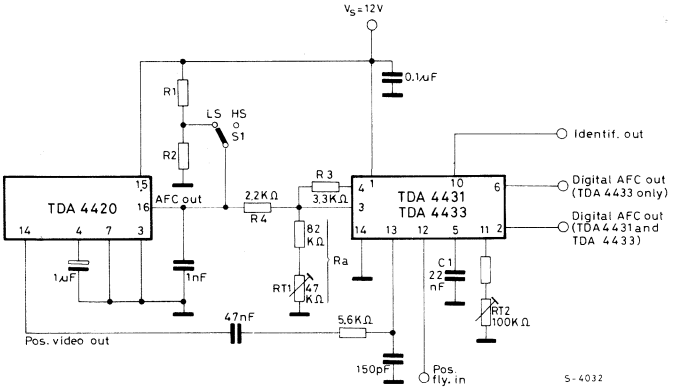
## APPLICATION INFORMATION

Fig. 3 - Application circuit




* $R_1$; $R_2$; $Ch_1$, depend from the SAWF characteristics

Fig. 4 - TV Signal identification circuit




### TV signal identification circuit:

The suggested application circuit is shown in fig. 4.
The passive components are chosen as follows:

$R_1$ and $R_2$ : these define the AFC response slope. For $R_1 = R_2 = 5.1$ KΩ, the typical slope is 750/11 KHz/V (with AFC output unloaded).

$S_1$ : switches between low slope (LS) and high slope (HS). The high slope is typically 88/11 KHz/V.

## APPLICATION INFORMATION (continued)

$R_3$ and $R_4$ : the ratio $(R_3 + R_4)/R_3$ defines the digital AFC width ($\delta f$) calculated from the linear AFC width ($2\Delta f$). With $V_s = 12V$, the relation is:

$$\delta f = 0.036\ (2\Delta f)\ \frac{R_3 + R_4}{R_3}$$

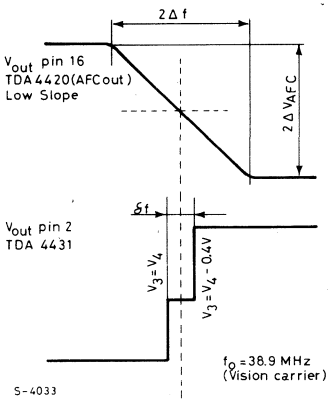
$R_{T1}$ : by means of this trimmer it is possible to align the linear tuning with the digital one, at the same frequency. The typical relation is:

$$R_a = 33\ R_3$$

with $R_3 = 3.3\ K\Omega$, $R_a$ can be a fixed resistor of $110\ K\Omega$.

To make better sensitivity adjustment of trimmer $R_{T2}$, it is necessary to use only a weak signal at the antenna. The video information must be a black picture or a field of small white points on a black field. Furthermore, the action of the syncs separator must be as quick as possible.
In receivers with automatic program search, S1 should be in the HS position and then the components S1, R1 and R2 can be omitted completely.

Fig. 5 - Linear and digital AFC characteristics (TDA 4420 and TDA 4431)



# TDA4431
# TDA4433

## TV SIGNAL IDENTIFICATION CIRCUIT AND AFC INTERFACE

The TDA4431 and the TDA4433 are monolithic integrated circuits in a 14 lead dual-in-line plastic package. They integrate the following functions:

– TV signal identificator – Sync. separator – Threshold detector – Digital Interface – Voltage regulator

They are intended for use in Electronic Program Memory tuning systems, the TDA4431 in conjunction with M193B1, while the TDA4433 with M293B1. The circuits features are:

– Identification of true TV stations only.
– Low impedance output of the identification signal.
– Digital control signal for automatic search and AFC operation.
– Thermal compensation of the voltage regulator.

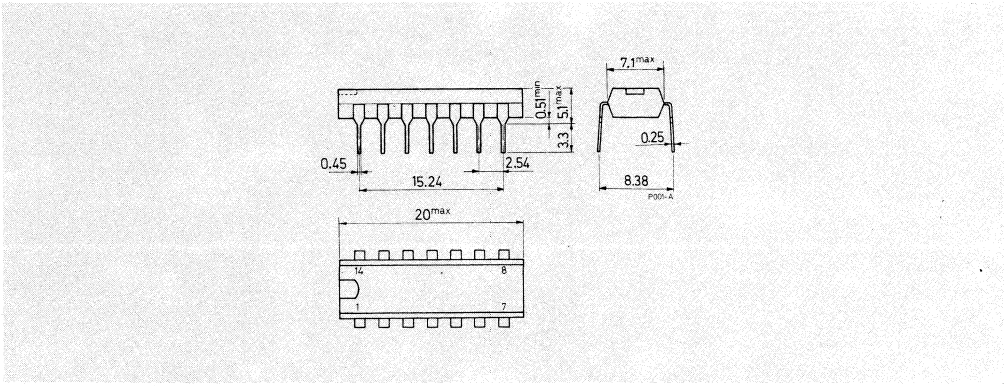
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 1) | 16 | V |
| $V_3$ | Voltage at pin 3 | 16 | V |
| $V_{13}$ | Voltage at pin 13 | -5 to +6 | V |
| $I_2$ | Pin 2 current (TDA4431) | ± 1 | mA |
| $I_6$ ; $I_2$ | Pin 6 and pin 2 current (TDA4433) | 1 | mA |
| $I_{10}$ | Pin 10 current | 2 | mA |
| $I_{11}$ | Pin 11 current | 2 | mA |
| $I_{12}$ | Pin 12 current | ± 2 | mA |
| $P_{tot}$ | Total power dissipation at $T_{amb} \leqslant 70°C$ | 800 | mW |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBERS:** TDA 4431
TDA 4433

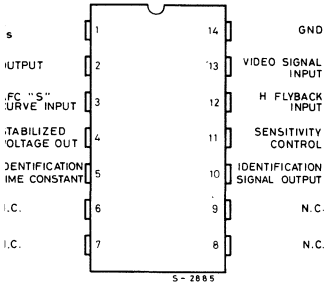
## MECHANICAL DATA

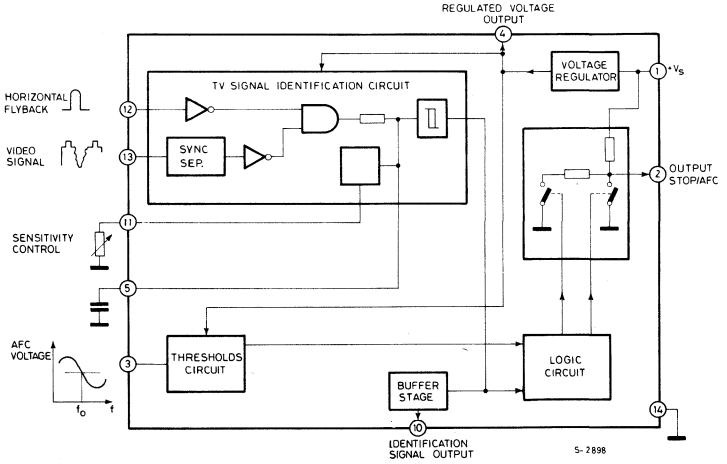
Dimensions in mm



## CONNECTION AND BLOCK DIAGRAM (TDA4431)

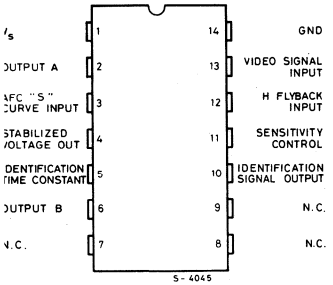
(Top view)

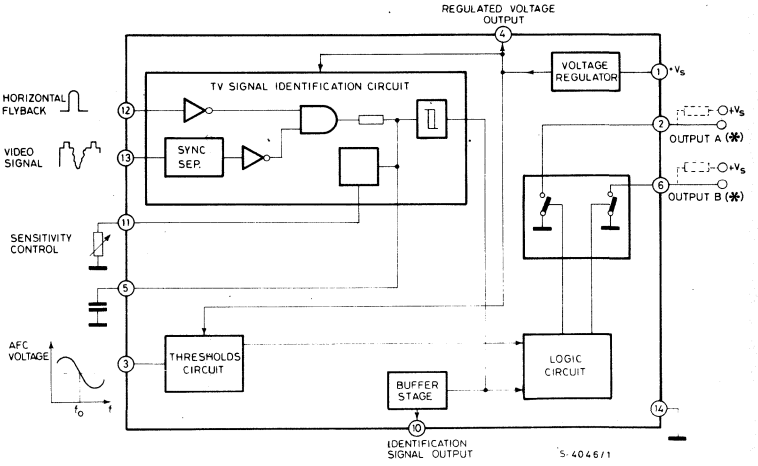



## CONNECTION AND BLOCK DIAGRAM (TDA4433)

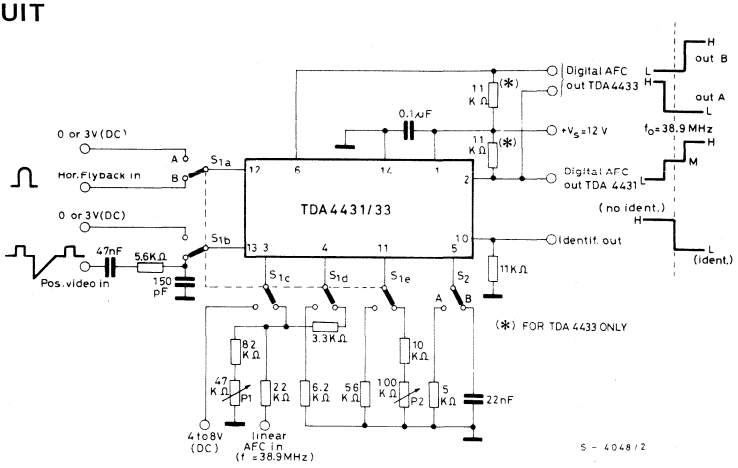
(Top view)




* Open collector outputs

## TEST CIRCUIT




$S_1$ A : Static tests
B : Functional tests

$S_2$ A : DC or pulses width
B : Functional tests

$P_1$ Digital AFC perfect tuning
$P_2$ Sensitivity control

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS (refer to the test circuit; $V_s$ = 12V, $T_{amb}$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage range (pin 1) | | 10.8 | | 14.5 | V |
| $I_s$ | Supply current (pin 1) | $V_s$ = 14.5V | | | 30 | mA |
| $V_2$ | Output voltage: low | $f_{tuning} < f_o$ | | | 0.8 | V |
| | medium | $f_{tuning} = f_o$ $V_s$ = 10.8 to 14.5 | 5.5 | | 8.5 | V |
| | high (TDA4431) | $f_{tuning} > f_o$ | $V_s$-0.5 | | | V |
| $V_2$ | Output voltage | $f_{tuning} < f_o$ $I_2$ = 1mA | $V_s$-0.5 | | | V |
| | | $f_{tuning} = f_o$ | | | 0.8 | V |
| | (TDA4433) | $f_{tuning} > f_o$ | | | 0.8 | V |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_6$ | Output voltage | | $f_{tuning} < f_o$ $I_6$ = 1mA | | | 0.8 | V |
| | | | $f_{tuning} = f_o$ $I_6$ = 1mA | | | 0.8 | V |
| | (TDA4433) | | $f_{tuning} > f_o$ | $V_s$-0.5 | | | V |
| $I_2$ | Output current (TDA4431) | | | | | ± 25 | μA |
| $V_3$ | Input voltage range | | | 4 | | 8 | V |
| $V_{3U}$ | Upper threshold voltage (see fig. 2) | | | $V_4$-25 | $V_4$ | $V_4$+25 | mV |
| $V_{3L}$ | Lower threshold voltage (see fig. 2) | | | $V_4$-425 | $V_4$-400 | $V_4$-375 | mV |
| $R_3$ | Input resistance | | $V_3 = V_4$ | 1.4 | | | MΩ |
| $V_4$ | Regulated voltage | | $I_4$ = 1mA | | 6.6 | | V |
| $I_4$ | Output current | | | | | 1 | mA |
| $R_4$ | Output differential resistance | | | | 60 | | Ω |
| $\frac{\Delta V_4}{\Delta T_s}$ | Regulated voltage thermal drift | | | | | ± 2 | mV/°C |
| $V_{10}$ | Identification output voltage | no identification | $I_{10}$ = 1mA | $V_s$-1.3 | | | V |
| | | identification | | | | 20 | mV |
| $R_{10}$ | Output resistance | | | | 100 | | Ω |
| $V_{12}$ | Switch off threshold voltage | | | | | 1 | V |
| $I_{12}$ | Input flyback current | | | 0.5 | | 1.5 | mA |
| $R_{12}$ | Input resistance | | $V_{12}$= 3V | | 10 | | KΩ |
| $t_{fly}$ | Flyback pulse duration | | | 10 | | 17 | μsec. |
| t | Time delay between leading edges of flyback pulse and sync. pulse | | | 0 | | 3.5 | μ sec. |
| $V_{13}$ | Video input signal (peak to peak) | | | 2.5 | | 4.5 | V |
| $V_{13}$ | Sync. pulse amplitude (above black level) | | | 0.52 | | | V |
| $R_{13}$ | Input resistance | | | | | 1.5 | KΩ |

Fig. 1 - Medium output voltage Vs. Supply voltage.

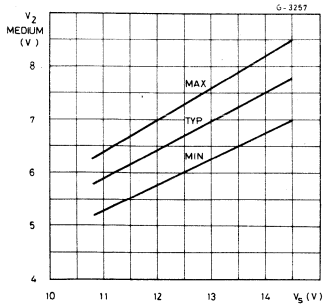
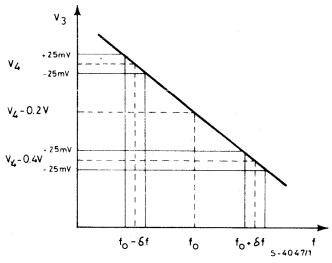



Fig. 2 - Digital AFC threshold voltage vs. frequency.




| Input Voltage ($V_3$) | TDA4431 | TDA4433 | |
|---|---|---|---|
| | Output voltage ($V_2$) | Output voltage ($V_2$) | Output voltage ($V_6$) |
| $V_3 > V_4$ | Low level | High level | Low level |
| $V_4$-0.4V $< V_3 < V_4$ | Medium level | Low level | Low level |
| $V_3 < V_4$-0.4V | High level | Low level | High level |

## APPLICATION INFORMATION (refer to the block diagram)

**TV signal identification circuit:**

The circuit recognizes only TV signals by checking logically during one line the coincidence between the horizontal flyback pulse and the pulse detected by a sync. separator.
The signal identification is carried out by charging the capacitor connected to pin 5; when the capacitor voltage overcomes a fixed threshold voltage, a Schmitt trigger switches and enables the AFC control. If a TV signal is recognized, the capacitor is slightly charged every line and its voltage reaches the threshold after a number of line which is defined by the value of the capacitor itself. The sensitivity of the identification circuit, hence the number of lines required to charge the capacitor, can be adjusted by means of the resistor connected between pin 11 and ground.
When the identification has been made, a signal (level L) is available at pin 10.

**Threshold circuit:**

The circuit detects 3 ranges of AFC voltage and in combination with the TV signal identification circuit drives the electronic switches.
With a correct TV signal, the output levels corresponding to the 3 ranges are:

| | TDA4431 ($V_2$) | TDA4433 | |
|---|---|---|---|
| | | ($V_2$) | ($V_6$) |
| $f_o - \delta f$ | L | H | L |
| $f_o$ | M | L | L |
| $f_o + \delta f$ | H | L | H |

L = Low level
M = Medium level
H = High level

Note that the output levels are different for the two devices.

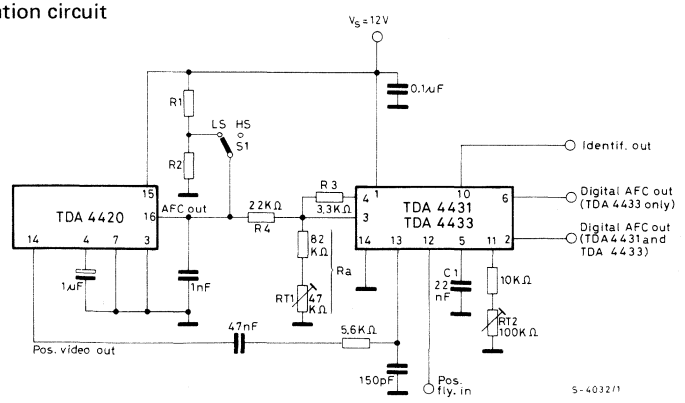
The TDA4431 provides three output levels: low (L), medium (M) and high (H). The output at pin 2 remains at medium level if no video signal is applied at the input or if a video signal is applied but is not identified as a true TV signal.

The TDA 4433 has two separate outputs which can have only two states, high (H) or low (L). The outputs at pin 2 and at pin 6 remain at a low level with no video signal input or with a video signal not identified as a true TV signal. Both pin 2 and pin 6 are open collector outputs and must be pulled-up to the positive supply voltage by external resistors.

**Voltage Regulator**

The circuit can deliver 1mA and it can be used as D/A converter reference to supply fine tuning voltage.

Fig. 3 - Application circuit



The passive components should be chosen as follows:

$R_1$ and $R_2$ : these define the AFC response slope. For $R_1 = R_2 = 5.1K\Omega$, the typical slope is 750/11 KHz/V (with AFC output unloaded).

$S_1$ : switches between low slope (LS) and high slope (HS). The high slope is typically 88/11 KHz/V.

$R_3$ and $R_4$ : the ratio $(R_3 + R_4)/R_3$ defines the digital AFC width ($\delta f$) calculated from the linear AFC width ($2\Delta f$). With $V_s = 12V$, the relation is:

$$\delta f = 0.036\,(2\Delta f)\,\frac{R_3 + R_4}{R_3}$$

$R_{T1}$ : by means of this trimmer it is possible to align the linear tuning with the digital one, at the same frequency. The typical relation is:

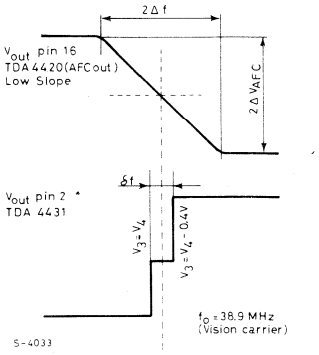
$$R_a = 33\,R_3$$

with $R_3 = 3.3K\Omega$, $R_a$ can be a fixed resistor of $110K\Omega$.

$R_{T2}$ : by means of this trimmer it is possible to choose the better sensitivity. It is possible to put a fixed resistor at pin 11 in the range of 68 K$\Omega$ to 100 K$\Omega$.

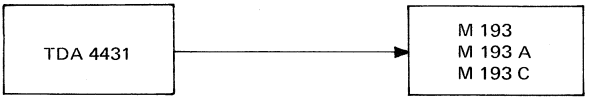
To make a better sensitivity adjustment of trimmer $R_{T2}$, it is necessary to use only a weak signal at the antenna. The video information must be a black picture or a field of small white points on a black field. Furthermore, the action of the syncs separator must be as quick as possible.
In receivers with automatic program search, S1 should be in the HS position and then the components S1, R1 and R2 can be omitted completely.

Fig. 4 – Linear and digital AFC

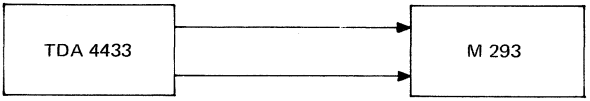


## EPM SYSTEM CONFIGURATIONS

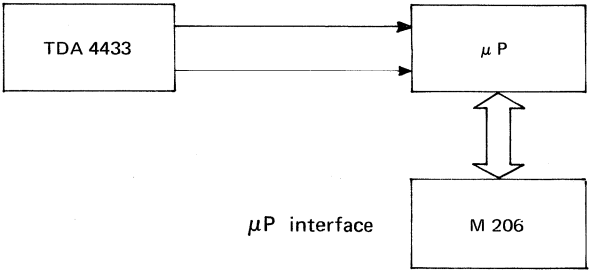
1) For 16 channels




2) For 32 channels




3) With microprocessor



# LINEAR INTEGRATED CIRCUITS

**TDA4950**

**ADVANCE DATA**

## TV EAST/WEST CORRECTION CIRCUIT

- LOW DISSIPATION
- SQUARE GENERATOR FOR PARABOLIC CURRENT
- EXTERNAL KEYSTONE ADJUSTMENT (SYMMETRY OF THE PARABOLA)
- INPUT FOR DYNAMIC FIELD CORRECTION (BEAM CURRENT CHANGE)
- STATIC PICTURE WIDTH ADJUSTMENT
- PULSE-WIDTH MODULATOR
- FINAL STAGE D-CLASS WITH ENERGY REDELIVERY
- PARASITIC PARABOLA SUPPRESSION, DURING FLYBACK TIME OF THE VERTICAL SAW-TOOTH

The TDA 4950 is a monolithic integrated circuit in a 8 pin minidip plastic package designed for use in the east-west pin-cushion correction by driving a diode modulator in TV and monitor applications.

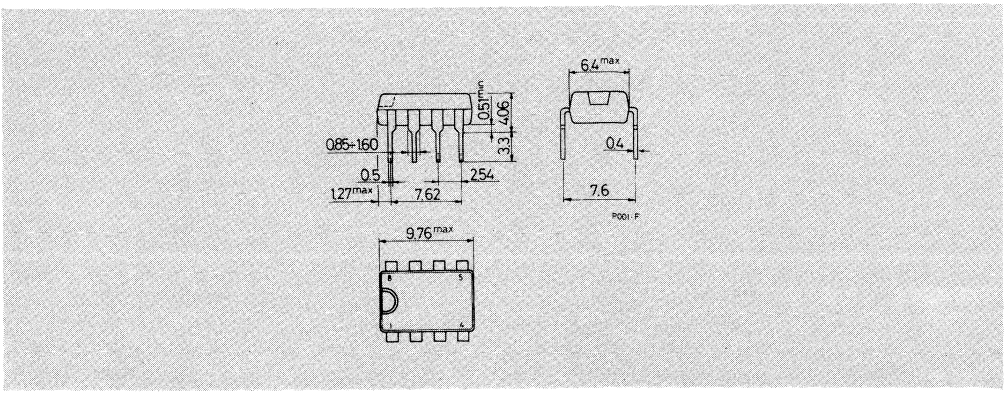
## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| $V_s$ | Supply voltage | 35 V |
| $I_s$ | Supply surrent | 500 mA |
| $P_{tot}$ | Power dissipation at $T_{amb} = 50°C$ | 500 mW |
| $T_{stg}$, $T_j$ | Storage and junction temperature | −25 to 150 °C |

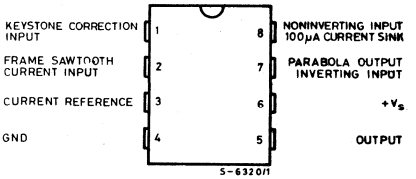
**ORDERING NUMBER:** TDA 4950

## MECHANICAL DATA

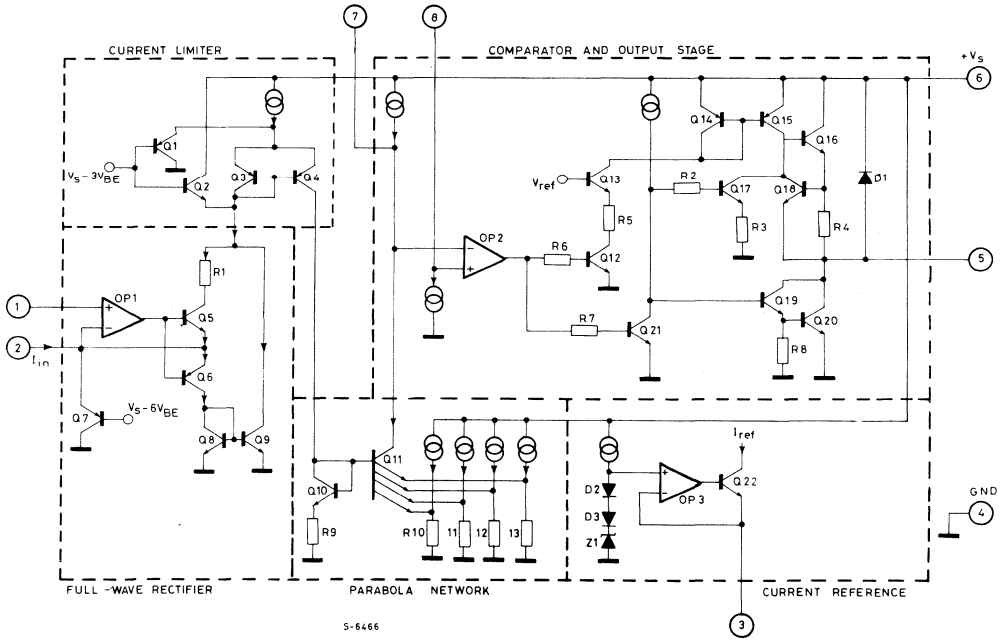
Dimensions in mm



## CONNECTION DIAGRAM




## SCHEMATIC DIAGRAM



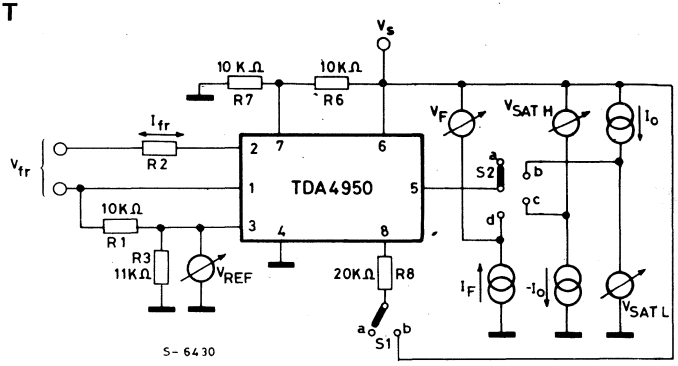

## THERMAL DATA

| | | |
|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max 100°C/W |
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-pin (4) | max 70°C/W |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $V_s$ = 24V, $V_{fr}$ = 0, S1 and S2 in "a" position, refer to test circuit unless otherwise specified).

| Parameter | | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 17 | 24 | 30 | V |
| $V_{ref}$ | Internal reference voltage | | | 8.2 | | V |
| $-I_{ref}$ | Internal reference current | $V_{ref}$ /R3 | | 0.75 | | mA |
| $V_{sat\ L}$ | Saturation voltage | $I_o$ = 400 mA sink S2 → b | | 1 | | V |
| $V_{sat\ H}$ | Saturation voltage | $-I_o$ = 100 mA source S2→C; S1→b | | 0.8 | | V |
| $V_F$ | Forward voltage | $I_F$ = 400 mA S2 → d; S1 → b | | 1.2 | | V |
| $I_{fr}$ | Frame sawtooth current | $V_{f2}$ = 6.6 Vpp | | 66 | | μApp |

## TEST CIRCUIT




## CIRCUIT OPERATION (see the schematic diagram)

A differential amplifier OP1 is driven by a vertical frequency sawtooth current of ± 33 μA which is produced via an external resistor from the sawtooth voltage. The non-inverting input of this amplifier is connected with a reference voltage corresponding to the DC level of the sawtooth voltage. This DC voltage should be adjustable for the keystone correction. The rectified output current of this amplifier drives the parabola network which provides a parabolic output current. This output current produces the corresponding voltage due to the voltage drop across the external resistor at pin 7.

If the input is overmodulated (> 40 μA) the internal current is limited to 40 μA. This limitation can be used for suppressing the parasitic parabolic current generated during the flyback time of the frame sawtooth.

A comparator OP2 is driven by the parabolic current. The second input of the comparator is connected with a horizontal frequency sawtooth voltage the DC level of which can be changed by the external circuitry for the adjustment of the picture width.

The horizontal frequency pulse-width modulated output signal drives the final stage. It consists of a class D push-pull output amplifier that drives, via an external inductor, the diode modulator.

Fig. 1 - Application circuit with keystone correction

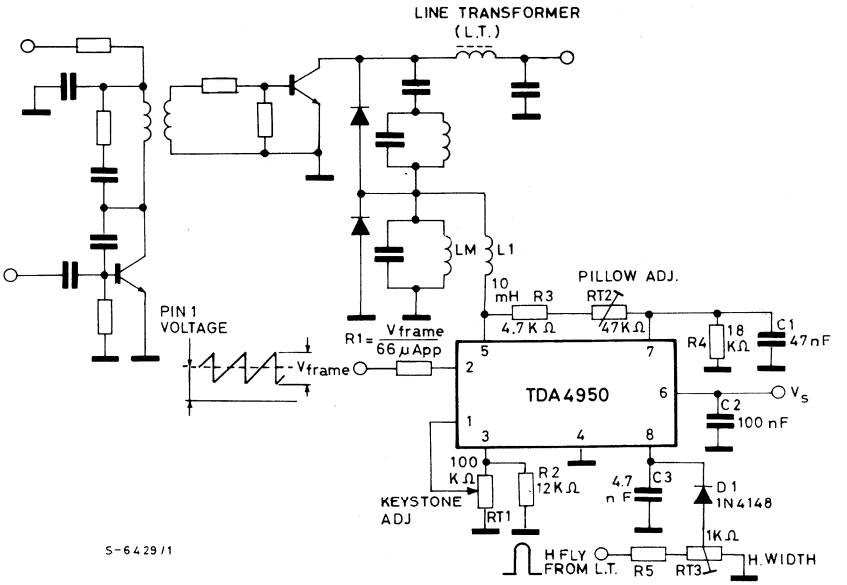
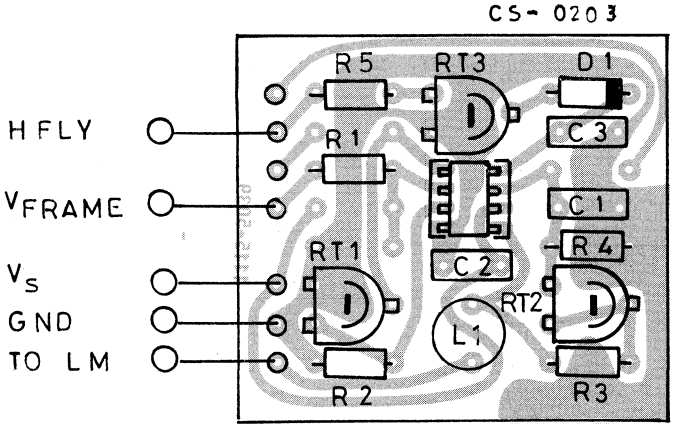



Fig. 2 - P.C. board and component layout of the circuit of fig. 1 (1:1 scale)



## CIRCUIT OPERATION (continued)

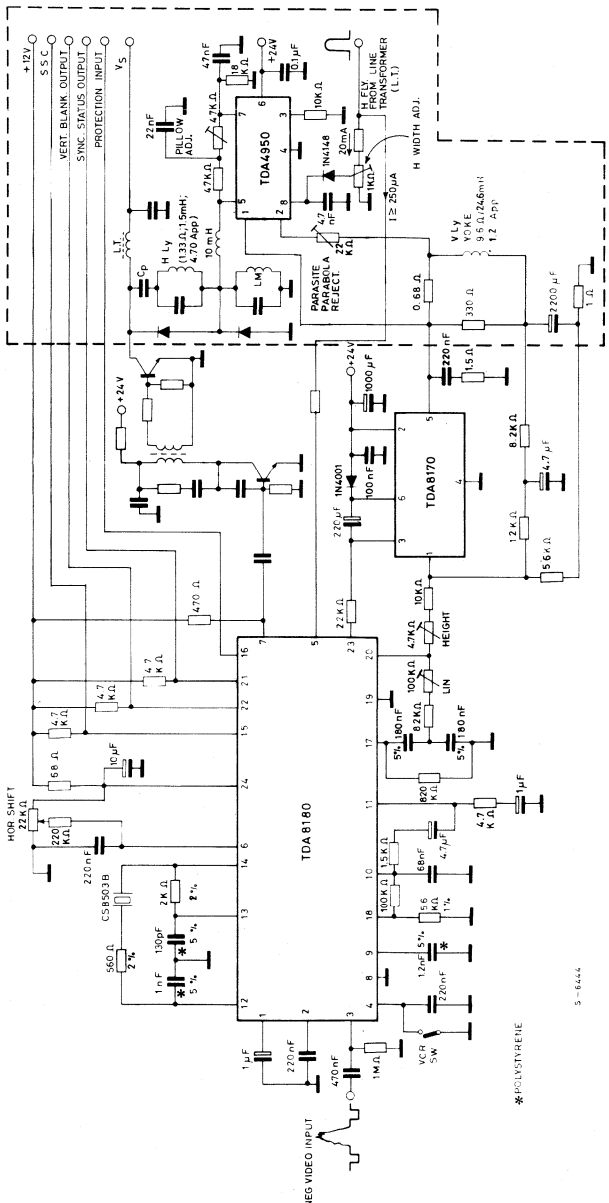



Fig. 4 - Complete circuit with deflection processor TDA8180 and vertical output TDA8170

# TDA7220

# LINEAR INTEGRATED CIRCUITS

**ADVANCE DATA**

## VERY LOW VOLTAGE AM-FM RADIO

- OPERATING SUPPLY VOLTAGE: 1.5 to 6V
- HIGH SENSITIVITY AND LOW NOISE
- LOW BATTERY DRAIN
- VERY LOW TWEET
- HIGH SIGNAL HANDLING
- VERY SIMPLE DC SWITCHING OF AM-FM
- AM SECTION OPERATES UP TO 30 MHz

The TDA 7220 is a monolithic integrated circuit in a 16-lead dual in-line plastic package designed for use in 3V, 4.5V and 6V portable AM-FM radio receivers.
The functions incorporated are:

### AM SECTION

- Preamplifier and double balanced mixer with AGC
- One pin local oscillator
- IF amplifier with internal AGC
- Detector and audio preamplifier

### FM SECTION

- IF amplifier and limiter
- Quadrature detector
- Audio preamplifier

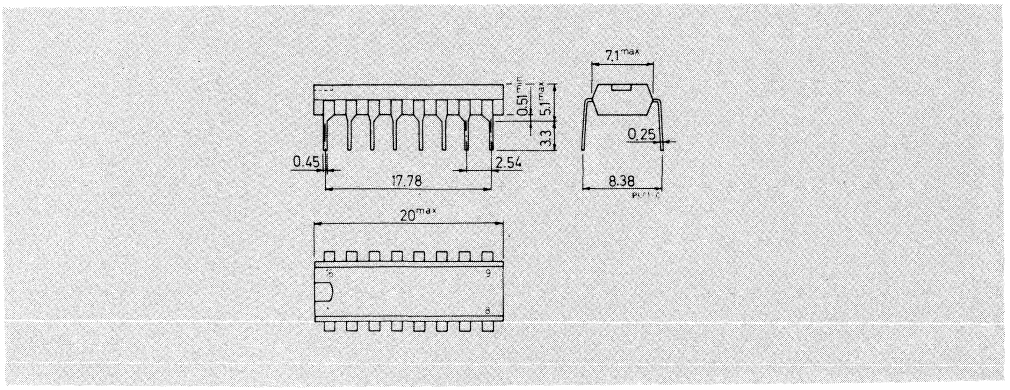
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 6.5 | V |
| $P_{tot}$ | Total power dissipation at $T_{amb} < 110°C$ | 400 | mW |
| $T_{op}$ | Operating temperature | -20 to 85 | °C |
| $T_{stg}, T_j$ | Storage and junction temperature | -55 to 150 | °C |

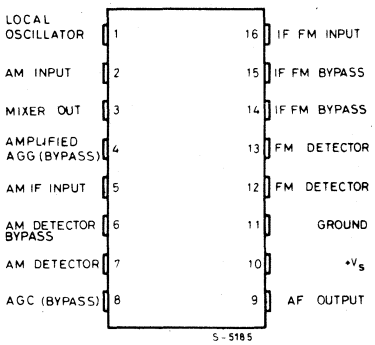
**ORDERING NUMBER:** TDA 7220

## MECHANICAL DATA

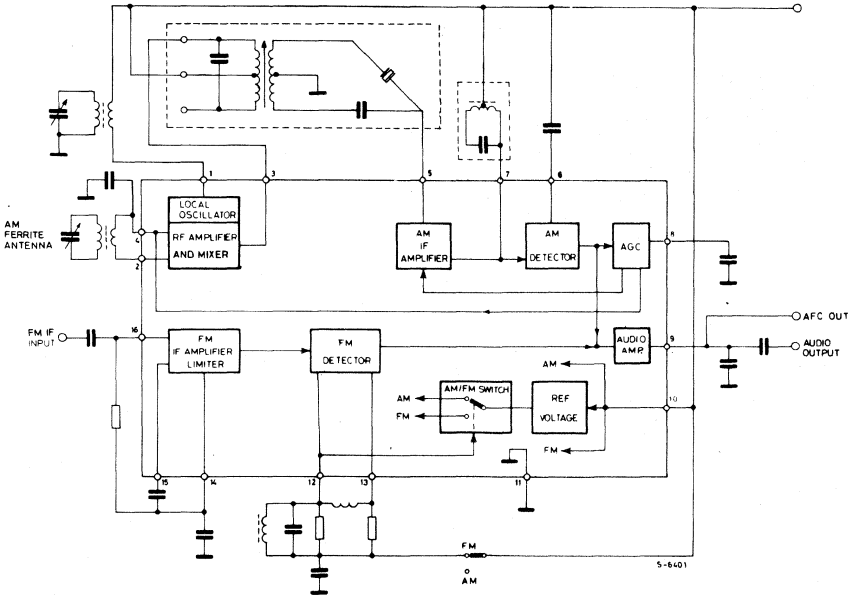
Dimensions in mm



## CONNECTION DIAGRAM




## BLOCK DIAGRAM




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $V_s$ = 1.6V unless otherwise specified, refer to test circuit)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_d$ | Drain current | AM section | | | 9 | | mA |
| | | FM section | | | 9 | | mA |
| **AM SECTION** ($f_o$ = 1 MHz; $f_m$ = 1 KHz) | | | | | | | |
| $V_i$ | Input sensitivity | S/N = 26 dB | m = 0.3 | | 15 | | μV |
| S/N | | $V_i$ = 1 mV | m = 0.3 | | 48 | | dB |
| $V_i$ | AGC range | $\Delta V_{out}$ = 10 dB | m = 0.8 | 90 | | | dB |
| $V_o$ | Recovered audio signal (pin 9) | $V_i$ = 1 mV | m = 0.3 | | 75 | | mV |
| d | Distortion | | | | 0.5 | | % |
| $V_H$ | Max input signal handling capability | m = 0.8 | d < 10% | 0.5 | | | V |
| $R_i$ | Input resistance between pins 2 and 4 | m = 0 | | | 7.5 | | KΩ |
| $C_i$ | Input capacitance between pins 2 and 4 | m = 0 | | | 18 | | pF |
| $R_o$ | Output resistance (pin 9) | | | | 4.5 | | KΩ |
| | Tweet 2 IF | m = 0.3 | $V_i$ = 1 mV | | 40 | | dB |
| | Tweet 3 IF | | | | 55 | | dB |
| **FM SECTION** ($f_o$ = 10.7 MHz; $f_m$ = 1 KHz) | | | | | | | |
| $V_i$ | Input limiting voltage | -3 dB limiting point | | | 50 | | μV |
| AMR | Amplitude modulation rejection | Δf = ± 22.5 KHz<br>$V_i$ = 3 mV | m = 0.3 | | 34 | | dB |
| S/N | Ultimate quieting | Δf = ± 22.5 KHz | $V_i$ = 1 mV | | 55 | | dB |
| d | Distortion | Δf = ± 22.5 KHz | $V_i$ = 1 mV | | 0.6 | | % |
| $V_o$ | Recovered audio signal (pin 9) | Δf = ± 22.5 KHz | $V_i$ = 1 mV | | 55 | | mV |
| $R_i$ | Input resistance between pin 16 and ground | | | | 6.5 | | KΩ |
| $C_i$ | Input capacitance between pin 16 and ground | | | | 14 | | pF |
| $R_o$ | Output resistance (pin 9) | | | | 4.5 | | KΩ |

## ELECTRICAL CHARACTERISTICS ($T_{amb}$ = 25°C, $V_s$ = 3V unless otherwise specified, refer to test circuit)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_d$ | Drain current | AM section | | | 10 | | mA |
| | | FM section | | | 10 | | mA |

### AM SECTION ($f_o$ = 1 MHz; $f_m$ = 1 KHz)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_i$ | Input sensitivity | S/N = 26 dB | m = 0.3 | | 12 | | μV |
| S/N | | $V_i$ = 1 mV | m = 0.3 | | 50 | | dB |
| $V_i$ | AGC range | $\Delta V_{out}$ = 10 dB | m = 0.8 | 90 | | | dB |
| $V_o$ | Recovered audio signal (pin 9) | $V_i$ = 1 mV | m = 0.3 | | 80 | | mV |
| d | Distortion | | | | 0.6 | | % |
| $V_H$ | Max input signal handling capability | m = 0.8 | d < 10% | 0.5 | | | V |
| $R_i$ | Input resistance between pins 2 and 4 | m = 0 | | | 7.5 | | KΩ |
| $C_i$ | Input capacitance between pins 2 and 4 | m = 0 | | | 18 | | pF |
| $R_o$ | Output resistance (pin 9) | | | | 4.5 | | KΩ |
| | Tweet 2 IF | m = 0.3 | $V_i$ = 1 mV | | 40 | | dB |
| | Tweet 3 IF | | | | 55 | | dB |

### FM SECTION ($f_o$ = 10.7 MHz; $f_m$ = 1 KHz)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_i$ | Input limiting voltage | -3 dB limiting point | | | 33 | | μV |
| AMR | Amplitude modulation rejection | $\Delta f$ = ± 22.5 KHz<br>$V_i$ = 3 mV | m = 0.3 | | 40 | | dB |
| S/N | | $\Delta f$ = ± 22.5 KHz | $V_i$ = 1 mV | | 65 | | dB |
| d | Distortion | $\Delta f$ = ± 22.5 KHz | $V_i$ = 1 mV | | 0.3 | | % |
| | | $\Delta f$ = ± 75 KHz | | | 1.1 | | % |
| $V_o$ | Recovered audio signal (pin 9) | $\Delta f$ = ± 22.5 KHz | $V_i$ = 1 mV | | 70 | | mV |
| $R_i$ | Input resistance between pin 16 and ground | | | | 6.5 | | KΩ |
| $C_i$ | Input capacitance between pin 16 and ground | | | | 14 | | pF |
| $R_o$ | Output resistance (pin 9) | | | | 4.5 | | KΩ |

Fig. 1 - Test circuit

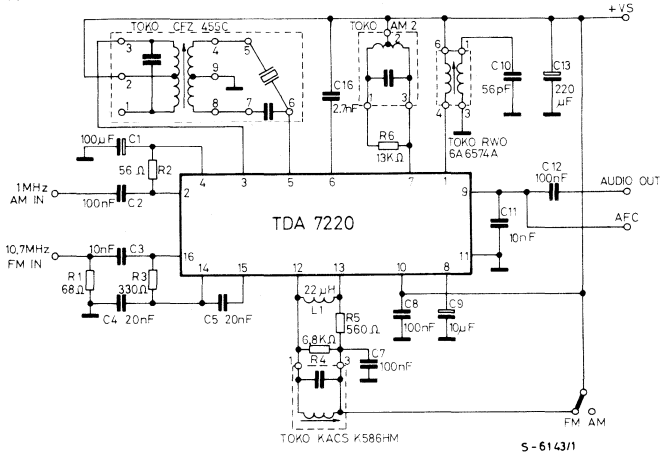
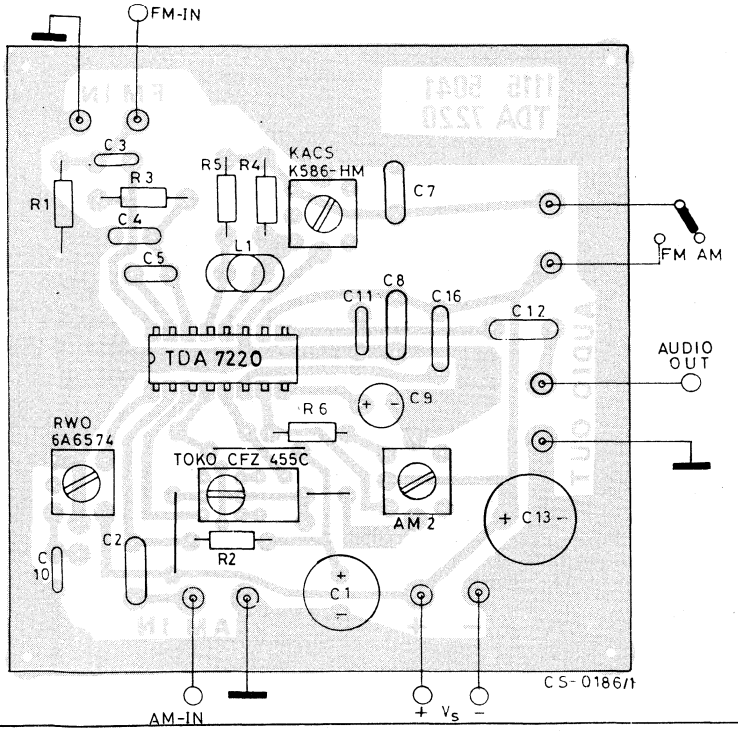



Fig. 2 - PC board and component layout (1:1 scale) of the test circuit



## APPLICATION INFORMATION

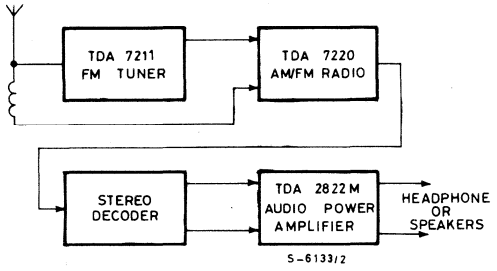
### AM-FM SWITCHING

AM-FM switching is achieved by applying a DC voltage at pin 13, to switch the internal reference.

### Typical DC voltages (refer to the test circuit)

| Pins | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AM | 3 | 1.1 | 3 | 1.1 | 1.1 | 2.5 | 3 | 0.7 | 1.2 | 3 | 0 | 2.1 | 2.1 | 2.9 | 3 | 2.9 | V |
| FM | 3 | 0 | 3 | 0 | 0 | 2.4 | 3 | 0 | 0.9 | 3 | 0 | 3 | 3 | 2.7 | 2.7 | 2.7 | V |

Fig. 3 - Stereo Radio/Cassette application ($V_s$ = 3V)



## MULTIFUNCTION SYSTEM FOR TAPE PLAYERS

The TDA 7270S is a multifunction monolithic integrated circuit in a 16-lead dual in-line plastic package specially designed for use in car radios cassette players, but suitable for all applications requiring tape playback.
It has the following functions:

- Motor speed regulator
- Automatic stop
- Manual stop
- Pause
- Cassette ejection
- Radio – Playback automatic switching.

The circuit incorporates also:

- Thermal protection
- Short circuit protection to ground (all the pins)

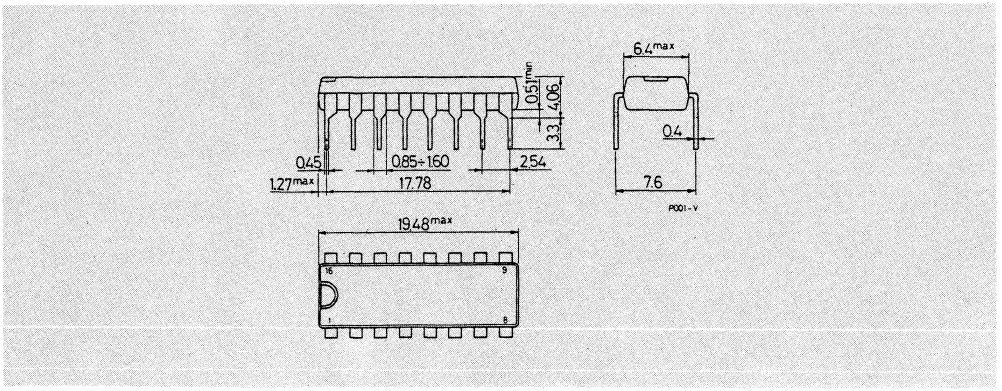
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 20 | V |
| $I_1$ | Sink peak current at pin 1 | 2 | A |
| $I_5$ | Sink peak current at pin 5 | 2 | A |
| $P_{tot}$ | Power dissipation at $T_{amb} \leqslant 80°C$ | 1 | W |
| $T_{stg}$ ; $T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA 7270 S

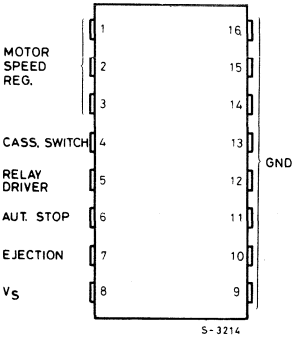
## MECHANICAL DATA

Dimensions in mm

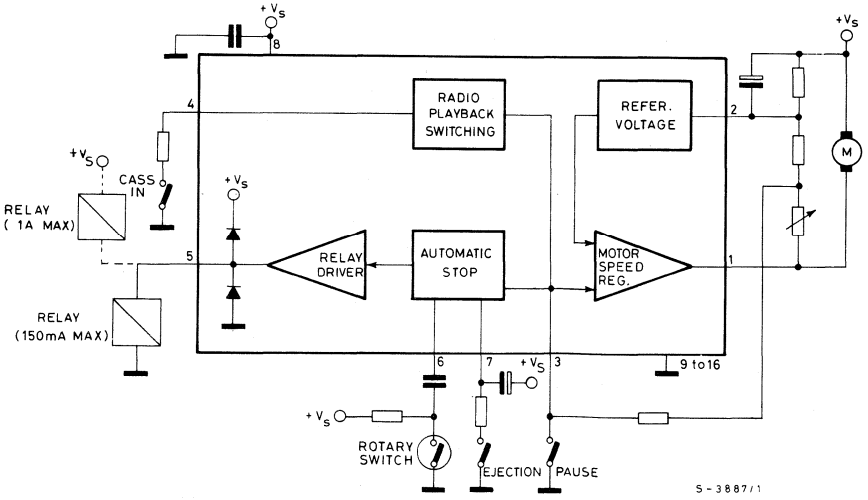


## CONNECTION DIAGRAM

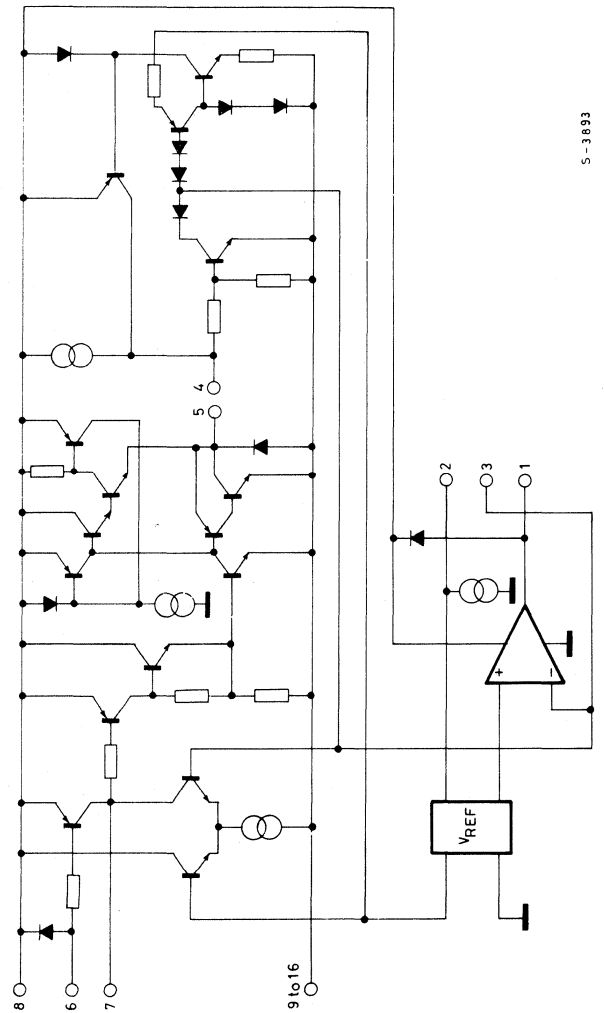
(top view)



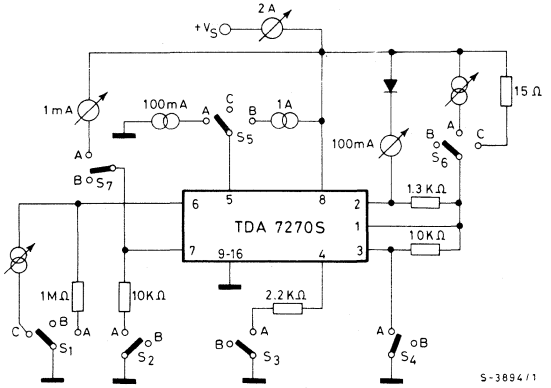

## BLOCK DIAGRAM



## SCHEMATIC DIAGRAM



## TEST CIRCUIT




## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 70 | °C/W |
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-pins | max | 15 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit; $T_{amb}$= 25°C; $V_s$ = 14V; $S_7$ at B, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage | | 6 | | 18 | V |
| $I_d$ | Quiescent drain current | Automatic stop-$S_3$ at B<br>$S_4$ at B | | 5 | 10 | mA |
| | | Pause - $S_3$ at A; $S_4$ at A | | 9 | 15 | |
| $I_5$ | Maximum output current for relay driving | | 150 | | | mA |
| $T_{sd}$ | Thermal shut-down case temperature | $P_{tot}$ = 1W<br>$(\frac{\Delta V_{ref}}{V_{ref}} = -5\%)$ | 105 | 125 | | °C |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **MOTOR SPEED CONTROL** | | | | | | |
| $I_{MS}$ | Starting current (pin 1) | | 1 | | | A |
| $V_{ref}$ | Reference voltage (pin 2-3) | $I_M$= 100 mA | 1.15 | 1.25 | 1.35 | V |
| $\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_s$ | | $I_M$= 100 mA<br>$V_s$= 8 to 18V | | 0.1 | 0.4 | %/V |
| $\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_M$ | | $I_M$= 50 to 400 mA | | 0.01 | 0.03 | %/mA |
| $\frac{\Delta V_{ref}}{V_{ref}}/\Delta T$ | | $I_M$= 100 mA<br>$T_{amb}$= -20 to 70°C | | 0.01 | | %/°C |
| $V_2$ | Operating voltage | $I_M$= 100 mA $\frac{\Delta V_{ref}}{V_{ref}}$ = -5% | 2.4 | | | V |
| K | Reflection coeff.(K= $I_M/I_T$ see fig. 12) | $I_M$= 100 mA | 18 | 20 | 22 | — |
| $\frac{\Delta K}{K}/\Delta V_s$ | | $I_M$= 100 mA<br>$V_s$= 8V to 18V | | 0.3 | 1 | %/V |
| $\frac{\Delta K}{K}/\Delta I_M$ | | $I_M$= 50 to 400 mA | | 0.005 | 0.02 | %/mA |
| $\frac{\Delta K}{K}/\Delta T$ | | $I_M$= 100 mA<br>$T_{amb}$= -20 to 70°C | | 0.01 | | %/°C |
| **PAUSE** | | | | | | |
| $I_3$ | Current consumption | $S_4$ at A | 1.4 | | | mA |
| $V_{8-1}$ | | $S_4$ at A | | | 0.2 | V |
| **EJECTION** | | | | | | |
| $I_7$ | | $S_2$ in A | 20 | | | μA |
| $V_{5-8}$ | Saturation voltage | $I_5$ = 100 mA | | 2.1 | 3 | V |
| $V_5$ | Saturation voltage | $I_{5-8}$= 1.5A | | 2.2 | 3 | V |
| $V_4$ | (Pause condition) | $S_1$ at A $S_3$ at A $S_4$ at A | 6 | | | V |
| $V_4$ | (Radio) | $S_1$ at A $S_3$ at B $S_4$ at B | 6 | 9 | | V |
| $V_4$ | (Tape) | $S_1$ at A $S_3$ at A $S_4$ at B | | | 1.7 | V |
| $R_o$ | Output impedance at pin 4 | $S_3$ at B | | 16 | 22 | KΩ |
| **AUTOMATIC STOP** | | | | | | |
| $V_{8-1}$ | Saturation voltage | $S_1$ at B $S_2$ at B $S_3$ at B | | | 1 | μA |
| $I_6$ | Minimum current to avoid stop | $S_1$ at C | | | 1 | μA |
| $I_{7-8}$ | Load current for delay circuit | $I_6$= 0 $S_7$ at A $S_2$ at B | 10.5 | 15 | 19.5 | μA |

Fig. 1 - Reference voltage vs. supply voltage.

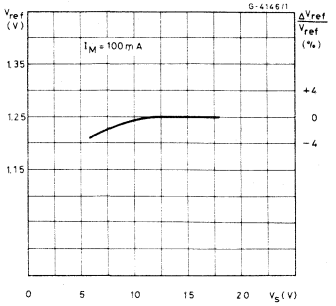



Fig. 2 - Reference voltage vs. motor current.

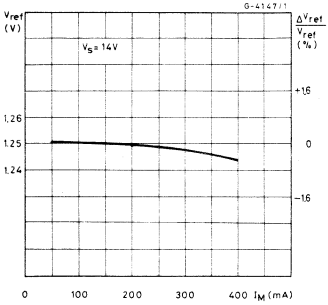



Fig. 3 - Reference voltage vs. ambient temperature.

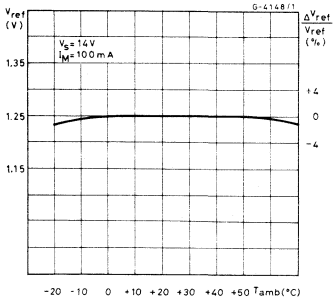



Fig. 4 - Saturation voltage (pins 5-8) vs. pin 5 current.

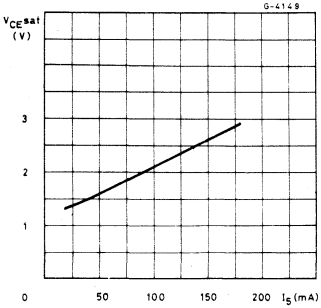



Fig. 5 - Reflection coefficient vs. supply voltage.

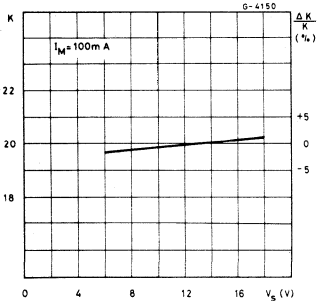



Fig. 6 - Reflection coefficient vs. motor current.

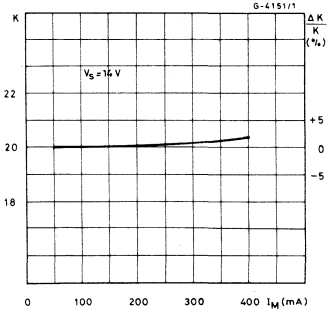



Fig. 7 - Reflection coefficient vs. ambient temperature.

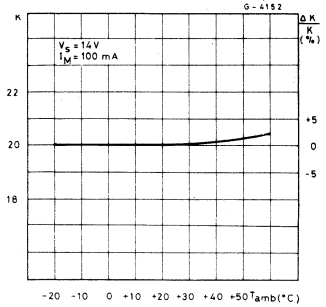
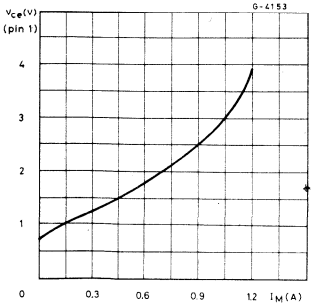



Fig. 8 - Pin 1 saturation voltage vs. motor current.



## APPLICATION INFORMATION

The TDA 7270S incorporates four different functional blocks:

1) Motor speed control.
2) Autostop circuit.
3) Radio/Playback switching
4) Relay driver.

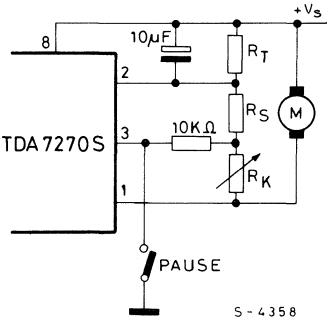
**The motor speed control** is a conventional circuit providing correction for the internal losses of the motor. Fig. 9 shows the external circuit.
The values of $R_T$, $R_S$ and $R_K$ determine the regulation characteristics and motor speed.

$$R_T = K \cdot R_M$$

where K = the IC regulator reflection coefficient and $R_M$ = motor internal resistance.
The following condition must be always satisfied

$$R_S \leqslant 4\, R_T$$

Fig. 9




The voltage applied across the motor is given by

$$V_{8-1} = V_{ref}\ [\,1 + \frac{R_T}{R_S}\ (\,1 + \frac{1}{K}) + \frac{R_K}{R_S}\,]$$

and this is proportional to $R_K$ which therefore adjusts the speed.
The voltage between pin 2 and the supply must not fall below 0.3V and so

$$[\,V_{ref\ min}\ (\frac{R_T}{R_S}) + I_{M\ min}\ (\frac{R_T}{K_{max}})\,] > 0.3V$$

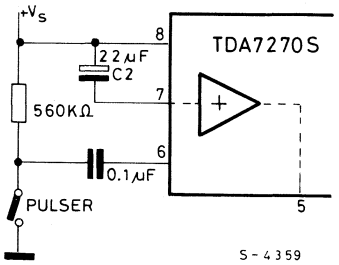
The "pause" condition corresponds to $V_3 < 50$ mV; in this condition the motor will stop ($V_{1-8} < 0.2V$), the capacitor $C_2$ on the autostop circuit (see below) will no longer be charged and the pin 4 (cassette/radio switch output) will be pulled high.

## APPLICATION INFORMATION (continued)

**The autostop circuit** is shown in fig. 10.
In normal operation the capacitor $C_2$ (22 $\mu$F) is slowly charged by a constant current drawn by pin 7 of 15 $\mu$A, and each time the pulser (a switch on the cassette take-up speed shaft) closes, $C_2$ is discharged. If the cassette stops, and the pulse stops, the voltage on pin 7 falls.
This switches the power amplifier state and pin 5 goes low. Pin 5 can be used for one of two purposes:

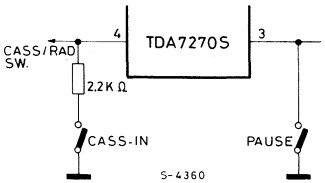
1) to drive a stop warning light connected from pin 5 supply $V_S$.
2) to actuate a solenoid wired either to ground (to release the cassette) or to supply (to eject the cassette).

Fig. 10




The **pause and/or cassette/radio switching** shown in fig. 11 has an input/output on pin 4.
If pin 4 is not used it should be grounded.

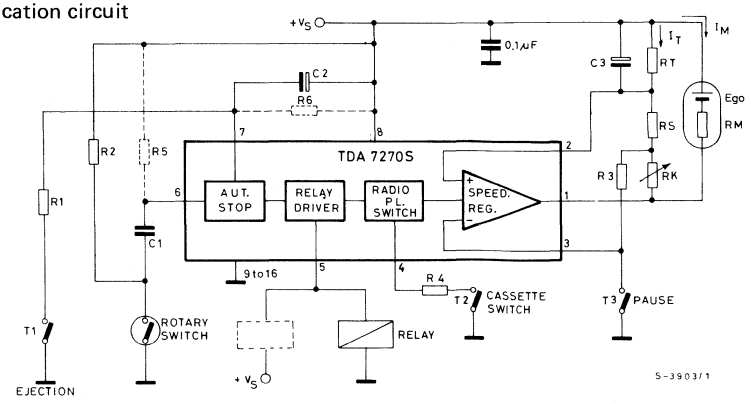
Fig. 11




This pin has the following logic.

| Cass IN | Pause | Pin 4 | Function |
|---|---|---|---|
| Open | Open | > 6V | motor off/radio on |
| Open | Close | > 6V | motor off/radio on |
| Close | Open | < 1.7V | motor on/cass. on |
| Close | Close | > 6V | pause/radio on |

Fig. 12 - Application circuit



## DESCRIPTION OF OPERATION (Refer to fig. 12)

When the cassette is introduced the switch $T_2$ closes, the motor start to turn and the rotary switch generates the pulses which keep the levels of pin 5 and pin 7 high. A relay between pin 5 and ground holds the cassette. If there are no pulses at pin 6 (because tape stopped) or if the ejection switch $T_1$ is closed, the voltages at pin 5 and pin 7 drop; the relay is thus de-energized and the cassette ejected; as soon as the cassette is ejected, the switch $T_2$ opens and the motor stops. The capacitor at pin 7 discharges allowing the system to start again when another cassette is inserted. In other types of mechanical systems the cassette is ejected by energizing a relay; in this case the relay must be connected between pin 5 and the supply; the sequence of operations is then the same as described above. If the pause switch $T_3$ is closed, the motor stops even though there are no pulses at pin 6, the voltage levels at pins 7 and 5 remain high so the cassette is not ejected and the motor is ready to start again as soon as the pause key is released. A voltage for driving the radio-tape switching is available at pin 4. This voltage level is high ($> 6V$) with stopped motor and is low ($< 1.7V$) with running motor.

## APPLICATION SUGGESTION (See figure 12)

| Component | Recommended value | Purpose | Larger than recommended value | Smaller than recommended value | Allowed range | |
|---|---|---|---|---|---|---|
| | | | | | Min. | Max. |
| $R_1$ | 10 KΩ | Limits current from pin 7 | Delayed ejection. Possibility that ejection does not work | High driving current at pin 7 | 0 | 100KΩ |
| $R_2$ | 560 KΩ | By rotary switch it produces pulses which disable the automatic stop | Undesired operation of automatic switch | Possibility of audio interference spikes | 100KΩ | 2MΩ |
| $R_3$ | 10 KΩ | Limits the motor current during pause ($T_3$ closed) | Reference voltage variation | Higher motor current during pause ($T_3$ closed) with delayed stop of motor | 1KΩ | 47KΩ |
| $R_4$ | 2.2 KΩ | Fixes voltage of pin 4 during pause and playback | Voltage at pin 4 increases | Voltage at pin 4 decreases. Radio-Playback switching could not work | 1.5KΩ | 2.7KΩ |
| $R_5$ | 560 KΩ | Compensates for current loss between pin 6 and ground | Limited compensation | Necessity to increase $C_1$ and decrease $R_2$ | 100KΩ | ∞ |
| $R_6$ | 1 MΩ | Compensates for current loss between pin 7 and ground. Also reduces recovery time | Limited compensation | Possibility that automatic stop will not work | 560KΩ | ∞ |
| $R_T$ | $K \cdot R_M$ (typical values) | Compensates for voltage drops at motor terminals vs. $\Delta I_M$ | Danger of oscillations | Poor speed regulation versus $\Delta I_M$ | See note on next page | |

## APPLICATION SUGGESTION (continued)

| Component | Recommended value | Purpose | Larger than recommended value | Smaller than recommended value | Allowed range Min. | Allowed range Max. |
|---|---|---|---|---|---|---|
| $R_S$ | See Note (*) | Fixes the current value in $R_T$ and and $R_K$ for $I_M = 0$ | Danger of saturation of non inverting input of regulator (pin 2). Considerable speed variation for small variation of $R_K$ | Impossibility to obtain a low motor speed | | $4\,R_T$ |
| $R_K$ | See Note (*) | Fixes the requested $V_{8-1}$ | Wide speed variation versus $\Delta R_K$ | Limited speed variation versus $\Delta R_K$ | | |
| $C_1$ | 0.1 $\mu$F | DC isolation | Electrolytic capacitors cannot be used | Undesired automatic stop | 0.047 $\mu$F | |
| $C_2$ | 22 $\mu$F | Integrates the pulses of the rotary switch | High recovery time | Low recovery time. Undesired automatic stop | 3.3 $\mu$F | |
| $C_3$ | 10 $\mu$F | By pass | Wow and flutter problems | Instability at low temperature | 5 $\mu$F | 22 $\mu$F |
| Rotary switch frequency | 20 Hz | Keeps automatic stop off | Possibility of audio interference spikes | Necessity to increase $C_1$ and $C_2$ | | |

NOTE (*):

– $V_{8-1} = V_{ref}\left[1 + \frac{R_T}{R_S}\left(1 + \frac{1}{K}\right) + \frac{R_K}{R_S}\right]$ from which it can be seen that $V_{8-1}$ varies linearly with $R_K$.

– The voltage between pin 2 and the supply must not fall below 0.5V, so the following expression must be verified

$$\left[V_{ref\,min}\left(\frac{R_T}{R_S}\right) + I_{M\,min}\left(\frac{R_T}{K_{max}}\right)\right] > 0.3V$$

– During the pause, the voltage between pin 3 and ground must be lower than 1.3V.

Fig. 13 - Speed variation vs. supply voltage

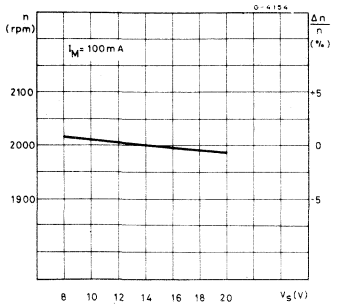



Fig. 14 - Speed variation vs. motor current

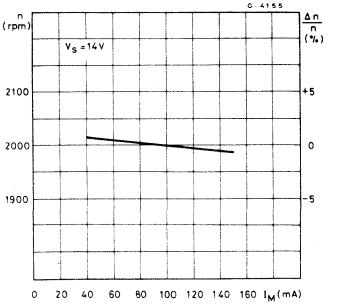
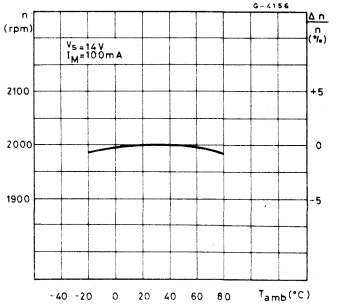



Fig. 15 - Speed variation vs. ambient temperature



## APPLICATION SUGGESTION (continued)

Fig. 16 - Delay time of the relay driver ($C_2$= 2.2 $\mu$F)

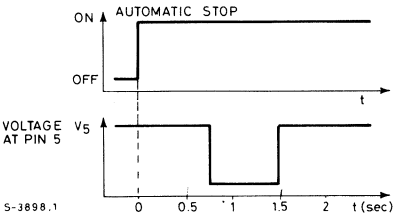
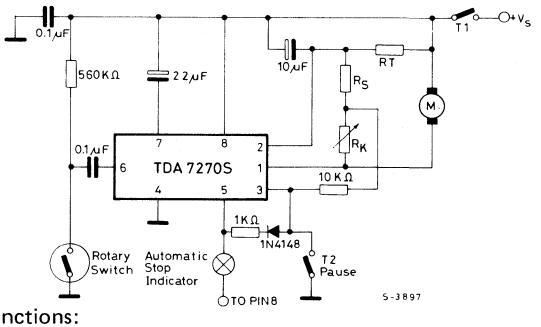



Fig. 17 - Low cost application circuit




The circuit shown in fig. 17 offers the following functions:

1) motor speed regulation
2) automatic stop
3) autostop warning light
4) pause.

The circuit incorporates an additional resistor/diode from pin 3 to pin 5. When the cassette stops, and the pulser no longer generates pulses, pin 5 falls to a low level and the stop indicator is on.
Pin 3 is pulled low through the 1 KΩ resistor and the diode, however pin 3 must not be pulled lower than 1.3V since this would cause pin 5 to go high again. The current of about 1 mA out of pin 3 causes $V_{3-5}$ to be about 1.5V.
In this way the motor remains stopped and pin 5 remains low.

## MOUNTING INSTRUCTIONS

Fig. 18 - Example of heatsink using PC board copper

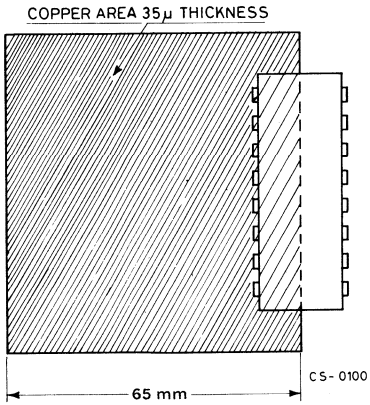
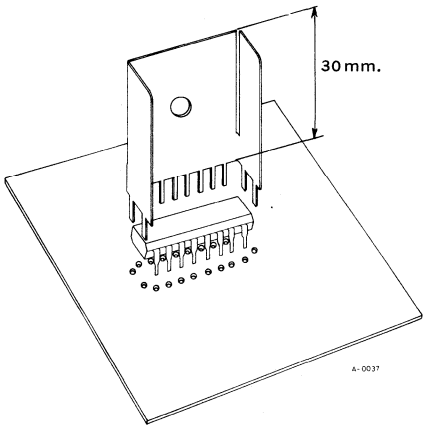



Fig. 19 - Example of external heatsink




Figures 18 and 19 show two ways to make the device dissipate.
In both cases, $R_{th}$= 35°C/W.

# LINEAR INTEGRATED CIRCUITS

**TDA8170**

ADVANCE DATA

## TV VERTICAL DEFLECTION OUTPUT CIRCUIT

The TDA 8170 is a monolithic integrated circuit in HEPTAWATT™ package. It is a high efficiency power booster for direct driving of vertical windings of TV yokes. It is intended for use in Colour and B & W television receivers as well as in monitors and displays. The functions incorporated are:

- power amplifier
- flyback generator
- reference voltage
- thermal protection

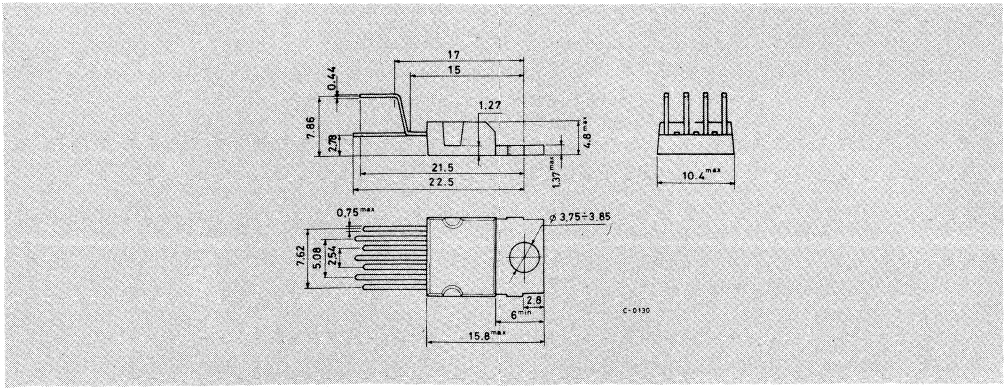
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 2) | 35 | V |
| $V_5$, $V_6$ | Flyback peak voltage | 60 | V |
| $V_3$ | Voltage at pin 3 | $+ V_s$ | |
| $V_1$, $V_7$ | Amplifier input voltage | $\pm V_s$ | |
| $I_o$ | Output peak current (non repetitive, t = 2 msec) | -0.5<br>2.5 | V<br>A |
| $I_o$ | Output peak current at f = 50 or 60 Hz, $t \leqslant 10\ \mu$sec | 3 | A |
| $I_o$ | Output peak current at f = 50 or 60 Hz, $t > 10\ \mu$sec | 2 | A |
| $I_3$ | Pin 3 DC current at $V_5 < V_2$ | 100 | mA |
| $I_3$ | Pin 3 peak to peak flyback current at f = 50 or 60 Hz, $t_{fly} \leqslant 1.5$ msec | 3 | A |
| $P_{tot}$ | Total power dissipation at $T_{case}$ = 70°C | 20 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to 150 | °C |

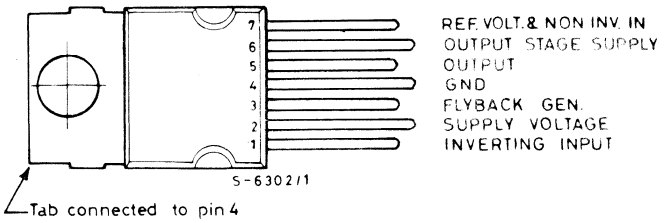
**ORDERING NUMBER:** TDA 8170

## MECHANICAL DATA

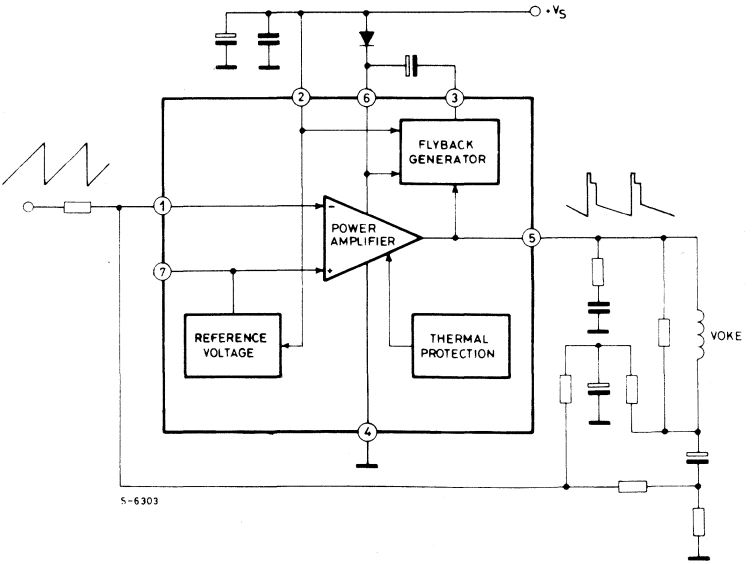
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## BLOCK DIAGRAM



## SCHEMATIC DIAGRAM

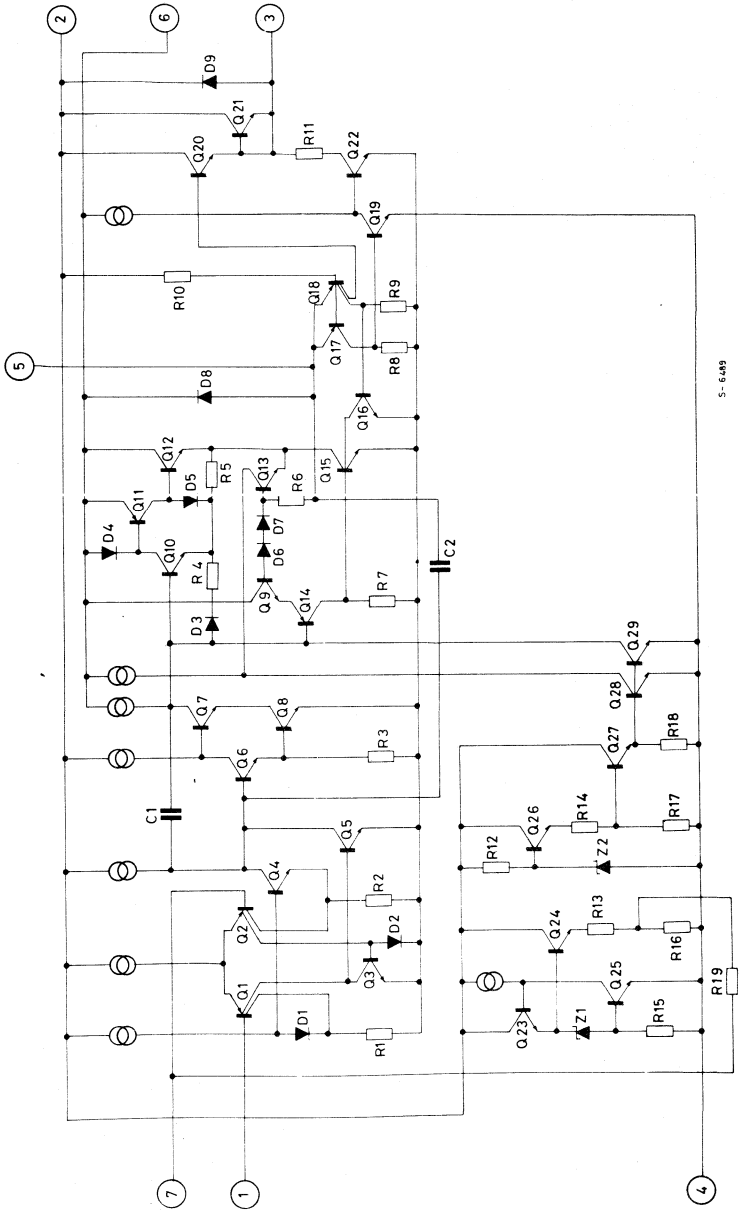
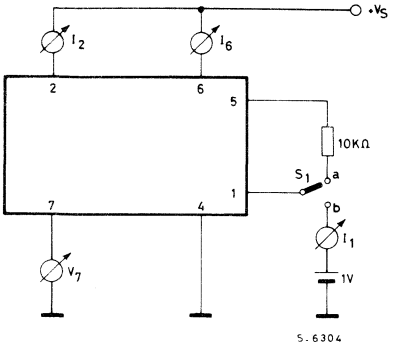


Fig. 1 - DC test circuits

Fig. 1a - Measurement of $I_1$; $I_2$; $I_6$; $V_7$; $\Delta V_7/\Delta V_s$.




$S_1$ : (a) $I_2$ and $I_6$; (b) $I_1$

Fig. 1b - Measurement of $V_{5H}$

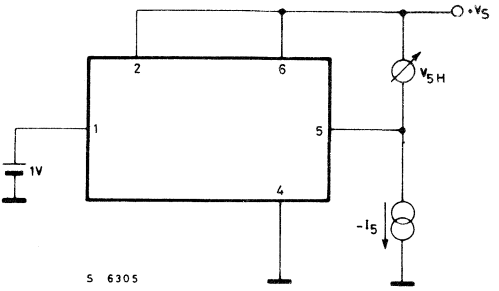
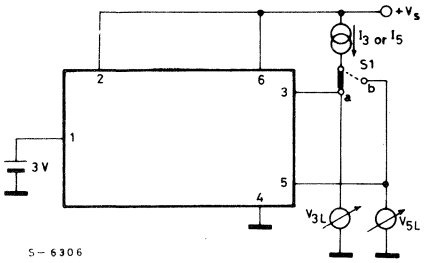
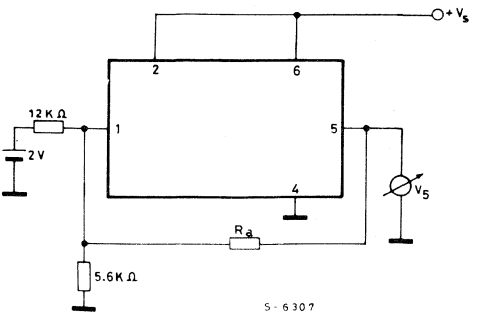



Fig. 1c - Measurement of $V_{3L}$; $V_{5L}$




S1 : (a) $V_{3L}$; (b) $V_{5L}$.

Fig. 1d - Measurement of $V_5$



## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}case}$ | Thermal resistance junction-case | max | 4 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuits, $V_s$ = 35V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit | Fig. |
|---|---|---|---|---|---|---|---|
| $I_2$ | Pin 2 quiescent current | $I_3 = 0$ $I_5 = 0$ | | 8 | 16 | mA | 1a |
| $I_6$ | Pin 6 quiescent current | $I_3 = 0$ $I_5 = 0$ | | 16 | 36 | mA | 1a |
| $I_1$ | Amplifier input bias current | $V_1$ = 1V | | -0.1 | -1 | μA | 1a |
| $V_7$ | Reference voltage | | | 2.2 | | V | 1a |
| $\frac{\Delta V_7}{\Delta V_s}$ | Reference voltage drift vs. supply voltage | $V_s$ = 15 to 30V | | 1 | 2 | mV/V | 1a |
| $V_{3L}$ | Pin 3 saturation voltage to GND | $I_3$ = 20 mA | | 1 | | V | 1c |
| $V_5$ | Quiescent output voltage | $V_s$ = 35V; $R_a$ = 39 KΩ | | 18 | | V | 1d |
| | | $V_s$ = 15V; $R_a$ = 13 KΩ | | 7.5 | | V | 1d |
| $V_{5L}$ | Output saturation voltage to GND | $I_5$ = 1.2A | | 1 | 1.4 | V | 1c |
| | | $I_5$ = 0.7A | | 0.7 | 1 | V | 1c |
| $V_{5H}$ | Output saturation voltage to supply | $-I_5$ = 1.2A | | 1.6 | 2.2 | V | 1b |
| | | $-I_5$ = 0.7A | | 1.3 | 1.8 | V | 1b |
| $T_j$ | Junction temperature for thermal shut down | | | 140 | | °C | |

Fig. 2 - AC test circuit

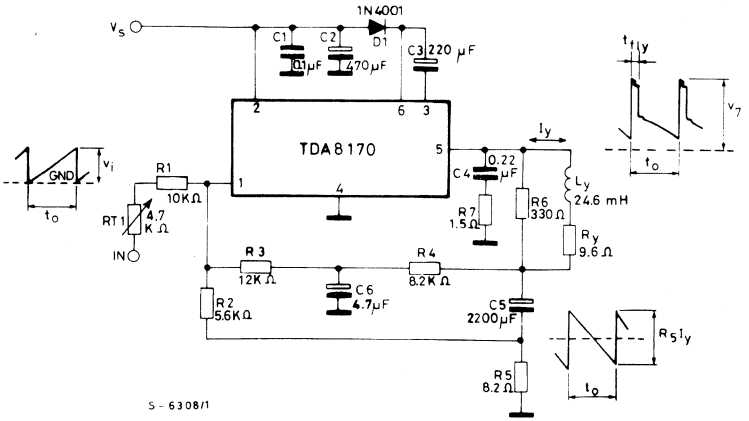
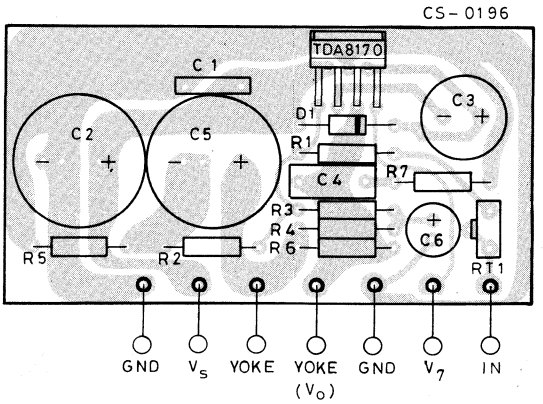



Fig. 3 - PC board and component layout of the circuit of fig. 2 (1:1 scale)



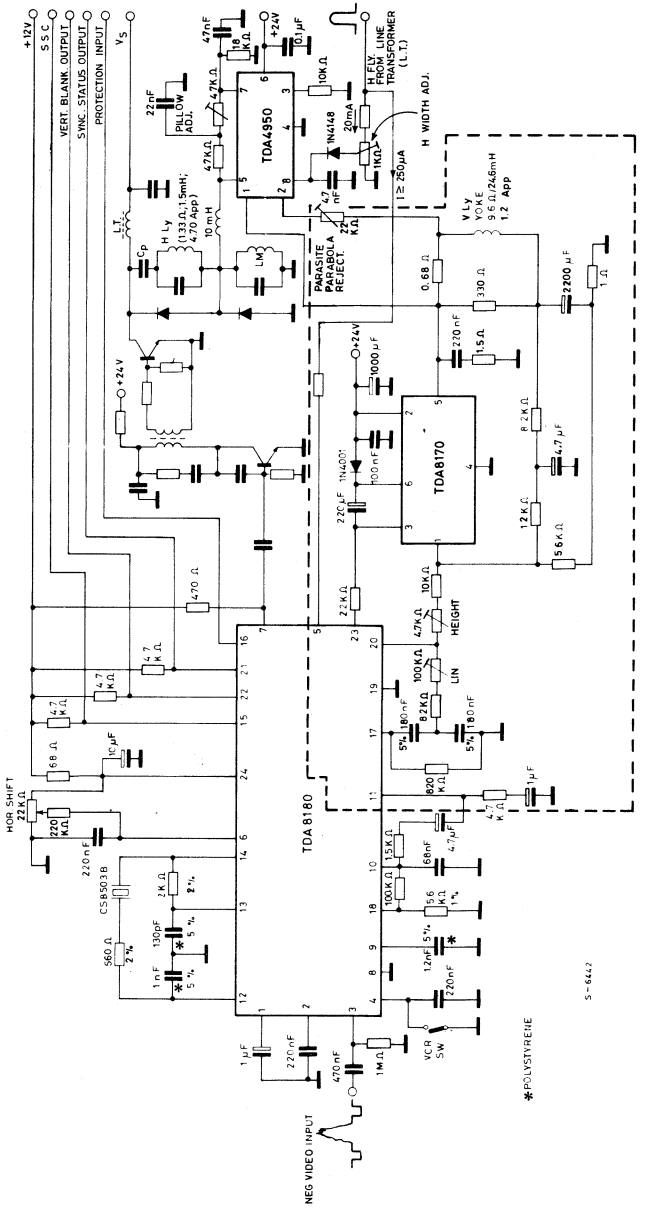
## Components list for typical applications

| Component | 110° TVC 5.9Ω/10 mH 1.95 App | 110° TVC 9.6Ω/24.6 mH 1.2 App | 90° TVC 15Ω/30 mH 0.82 App | Unit |
|---|---|---|---|---|
| RT1 | 10 | 4.7 | 10 | KΩ |
| R1 | 12 | 10 | 12 | KΩ |
| R2 | 10 | 5.6 | 5.6 | KΩ |
| R3 | 27 | 12 | 18 | KΩ |
| R4 | 12 | 8.2 | 5.6 | KΩ |
| R5 | 0.82 | 1 | 1 | Ω |
| R6 | 270 | 330 | 330 | Ω |
| R7 | 1.5 | 1.5 | 1.5 | Ω |
| D1 | 1N 4001 | 1N 4001 | 1N 4001 | — |
| C1 | 0.1 | 0.1 | 0.1 | μF |
| C2 el. | 1000/25V | 470/25V | 470/25V | μF |
| C3 el. | 220/25V | 220/25V | 220/25V | μF |
| C4 | 0.22 | 0.22 | 0.22 | μF |
| C5 el. | 2200/25V | 2200/25V | 1000/16V | μF |
| C6 el. | 4.7/16V | 4.7/16V | 10/16V | μF |

## Typical performances

| Parameter | 110° TVC 5.9Ω/10 mH | 110° TVC 9.6Ω/27 mH | 90° TVC 15Ω/30 mH | Unit |
|---|---|---|---|---|
| $V_s$ — Supply voltage | 24 | 22.5 | 25 | V |
| $I_s$ — Current | 280 | 175 | 125 | mA |
| $t_{fly}$ — Flyback time | 0.6 | 1 | 0.7 | ms |
| $P_{tot}$ — Power dissip. | 4.2 | 2.5 | 2.05 | W |
| $R_{th\ c-a}$ — Heatsink | 7 | 13 | 16 | °C/W |
| $T_{amb}$ | 60 | 60 | 60 | °C |
| $T_{j\ max}$ | 110 | 110 | 110 | °C |
| $t_o$ | 20 | 20 | 20 | ms |
| $v_i$ | 2.5 | 2.5 | 2.5 | Vpp |
| $v_7$ | 2.5 | 2.5 | 2.5 | Vp |

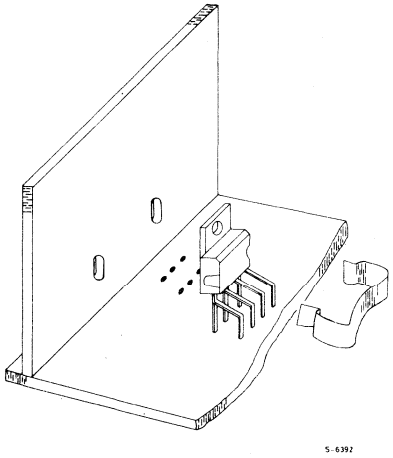
Fig. 4 - Complete deflection circuit

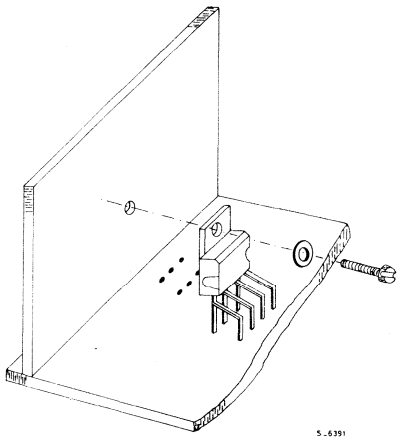


## MOUNTING INSTRUCTIONS

The power dissipated in the circuit must be removed by adding an external heatsink.
Thanks to the HEPTAWATT™ package attaching the heatsink is very simple, a screw a compression spring (clip) being sufficient. Between the heatsink and the package it is better to insert a layer of silicon grease, to optimize the thermal contact; no electrical isolation is needed between the two surfaces.

Fig. 5 - Mounting examples



# TDA8180

# LINEAR INTEGRATED CIRCUITS

**ADVANCE DATA**

## DEFLECTION PROCESSOR

- NO FREQUENCY OR PHASE ADJUSTMENTS
- FEW EXTERNAL COMPONENTS
- COUNTDOWN TIMING LOGIC
- SOPHISTICATED SYNC SEPARATOR
- ADAPTS AUTOMATICALLY TO 625 LINE/50 Hz AND 525 LINE/60 Hz STANDARDS
- PRECISE SUPER-SANDCASTLE & VERTICAL BLANKING OUTPUTS
- 50/60 Hz IDENTIFICATION OUTPUT
- AUTOMATIC VERTICAL AMPLITUDE CORRECTION FOR 50/60 Hz
- CRT PROTECTION CIRCUITS
- 5V SUPPLY; INTERNAL SHUNT REGULATOR FOR HIGHER SUPPLIES
- SPECIALLY DESIGNED FOR VCR OPERATION
- PHASE-CORRECTED HORIZONTAL OUTPUT WITH CONSTANT DUTY CYCLE

The TDA 8180 Deflection Processor integrates the signal processing functions for horizontal and vertical deflection in TVs and monitors. It generates drive waveforms for external deflection power stages plus super-sandcastle and vertical blanking signals for the chroma processor. Additionally it includes CRT protection circuits and an internal voltage regulator. A 5V supply is used and only a series resistor is required for higher supply voltages. A sophisticated sync separator, phase-locked loops and countdown circuitry guarantee high precision and eliminate all frequency and phase adjustments. A low cost 503kHz ceramic resonator defines all circuit timing. The TDA 8180 works with both 625 line/50 Hz and 525 line/60 Hz standards and switches automatically, correcting the vertical sawtooth amplitude. A 50/60 Hz identification output is provided.

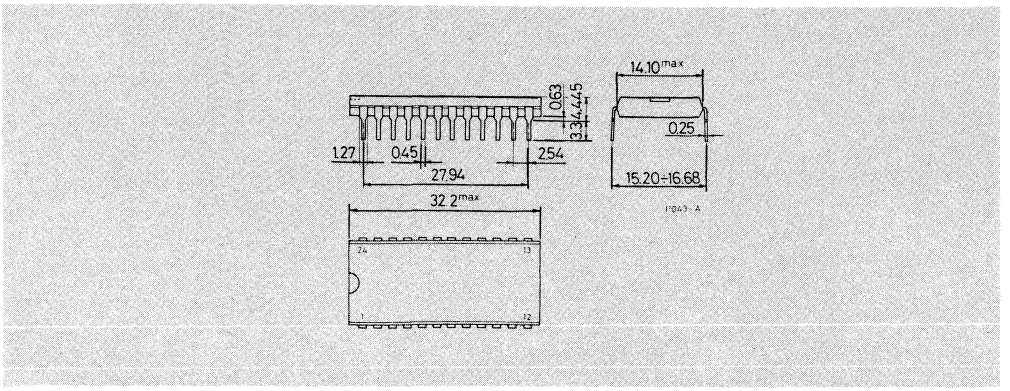
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage at pin 24 (without limiting resistor) | 5.25 | V |
| $V_{cc}$ | Voltage at pins 7, 15, 21, 22 | 20 | V |
| $V_i$ | Input signals | 5 | V |
| $P_{tot}$ | Total power dissipation ($T_{amb}$ = 70°C) | 1 | W |
| $T_{stg}$, $T_j$ | Storage and junction temperature | -40 to + 150 | °C |

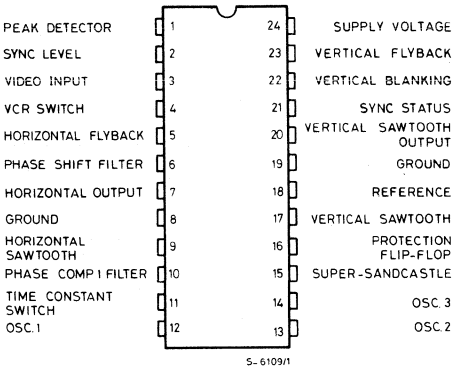
**ORDERING NUMBER:** TDA8180

## MECHANICAL DATA

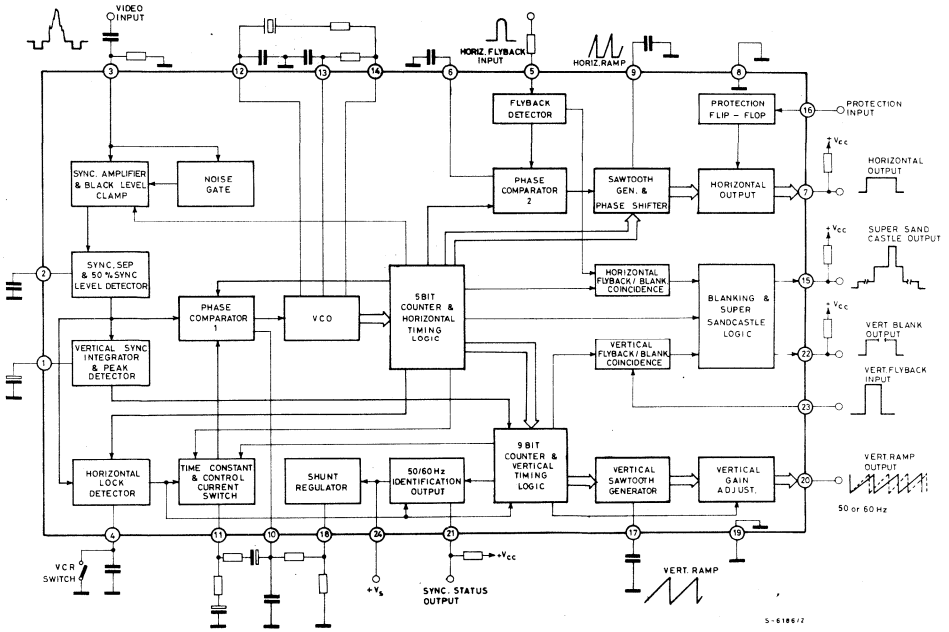
Dimensions in mm



## CONNECTION DIAGRAM




## BLOCK DIAGRAM



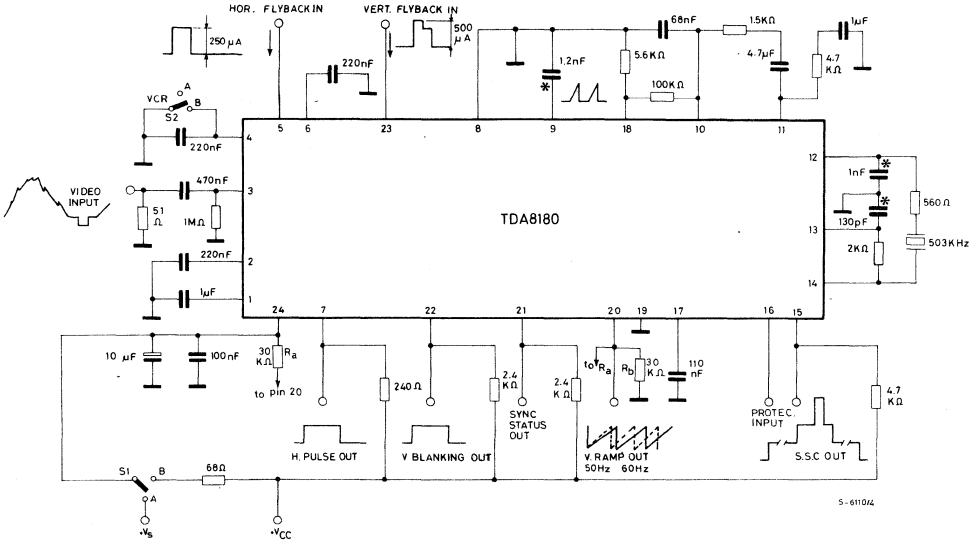
## PIN FUNCTIONS

| N° | NAME | FUNCTION |
|---|---|---|
| 1 | PEAK DETECTOR | A capacitor connected between this pin and ground determines time constant of frame sync. peak detector. |
| 2 | SYNC LEVEL | A capacitor connected to ground sets time constant of 50% sync level detector. |
| 3 | VIDEO INPUT | Input for negative video signal (white level above black level). |
| 4 | VCR SWITCH | A capacitor connected to ground sets time constant of line lock detector. When this pin is grounded the line and frame are held in the "sensitive" state for VCR operation. |
| 5 | HORIZONTAL FLYBACK | Input for horizontal flyback signal. Two thresholds: lower provides horizontal blanking: upper provides coincidence signal for dynamic phase correction of line drive. |
| 6 | PHASE SHIFT FILTER | A capacitor connected to ground sets time constant of horizontal phase correction loop. (A trimmer may be added here for static phase correction). |
| 7 | HORIZONTAL OUTPUT | Open collector output for 29 $\mu$s horizontal drive pulse. Maximum current is 50 mA. |
| 8 | GROUND | Ground connection for horizontal deflection circuitry. |
| 9 | HORIZONTAL SAWTOOTH | Capacitor for horizontal sawtooth generator connected here. The capacitor should be 5% tolerance and stable in temperature. |
| 10 | PHASE COMP 1 FILTER | An RC network connected here determines time constant of line PLL. |
| 11 | TIME CONSTANT SWITCH | This pin switches the time constant of phase comparator 1. It is grounded when the PLL is locked; high impedance when it is unlocked. |

## PIN FUNCTIONS (continued)

| N° | NAME | FUNCTION |
|---|---|---|
| 12<br>13<br>14 | OSCILLATOR<br>(OSC1, OSC2 & OSC3) | Frequency determining network for VCO connected to these pins. A 503 kHz ceramic resonator is used. |
| 15 | SUPER-SANDCASTLE | Output for super-sandcastle signal. Must be connected to supply through a resistor. |
| 16 | PROTECTION INPUT | Input of general-purpose protection flip flop. When grounded flip flop set, disabling horizontal drive. Flip flop is reset by removing supply. |
| 17 | VERTICAL SAWTOOTH | Capacitor for vertical sawtooth generator connected here. |
| 18 | REFERENCE | A resistor connected to this pin sets reference voltage for VCO and reference currents for ramp generators. |
| 19 | GROUND | Ground connection for vertical deflection circuitry. |
| 20 | VERTICAL SAWTOOTH OUTPUT | Output for vertical sawtooth. Amplitude is constant. |
| 21 | SYNC STATUS | Three level open-collector output indicating synchronisation status. The three levels correspond to "out of lock", 50 Hz locked, 60 Hz locked. |
| 22 | VERTICAL BLANKING | Open collector output for vertical blanking. |
| 23 | VERTICAL FLYBACK | Input for vertical flyback signal. |
| 24 | SUPPLY VOLTAGE | Supply voltage input. May be 5V or (with external resistor) above 5V. Internal 5.5V shunt regulator stabilizes higher supplies. |

## TEST CIRCUIT




* POLYSTIRENE CAPACITOR.
Note - Resistors: ± 0.5% metal film type; capacitors: Mylar type.

## THERMAL DATA

| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}pins}$ | Thermal resistance junction-pins | max | 80 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s$ = 5V, $V_{cc}$ = 12V, $S_1$ and $S_2$ in position A, $T_{amb}$ = 25°C, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage (pin 24) | | 4.75 | 5 | 5.25 | V |
| $I_s$ | Supply current (pin 24) | | | 60 | | mA |
| $V_{24}$ | Stabilized voltage at pin 24 | $S_1$ in position B | | 5.5 | | V |
| **SYNC. SEP. AND NOISE GATE** | | | | | | |
| $V_3$ | Peak to peak input signal (negative video signal) | | 0.5 | 2 | 4 | V |
| $t_W$ | Sampling window duration | | | 4 | | µs |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **VIDEO IDENTIFICATION AND VCR SWITCH** | | | | | | |
| $V_4$ | VCR switch voltage | | | | 1.5 | V |
| $V_4$ | Threshold voltage for time constant switching | | | 3.3 | | V |
| $I_4$ | Peak output current | Lock | | 1 | | mA |
| $-I_4$ | Output current | | | 20 | | µA |
| **OSCILLATOR** | | | | | | |
| $F_O$ | Free running frequency | | | 500 | | kHz |
| $S_O$ | Frequency control sensitivity | | | 2.13 | | kHz/V |
| $V_{10}$ | Control voltage range | | | 2.6 to 4 | | V |
| **SYNC-OSCILLATOR PHASE COMPARATOR** | | | | | | |
| $I_{10}$ | Control peak current | | | ± 0.3 | | mA |
| $S_1$ | Phase control sensitivity | | | 0.935 | | V/µs. |
| $\Delta f$ | Catching and holding range | | | ± 700 | | Hz |
| **FLYBACK-OSCILLATOR PHASE COMPARATOR** | | | | | | |
| $V_6$ | Control voltage range | | | 2.8 to 3.7 | | V |
| $I_6$ | Peak control current | | | ± 0.5 | | mA |
| | Static control error | | | 1 | | % |
| $S_2$ | Phase control sensitivity | | | 20.4 | | µs/V |
| $t_d$ | Permissible delay between output pulse and flyback pulse | $t_{flyback}$= 12 µs | | 17 | | µs. |
| **COMPOSITE BLANKING AND KEY PULSE (SUPERSANDCASTLE)** | | | | | | |
| $V_{15K}$ | Key pulse output peak voltage | | | 10 | | V |
| $V_{15L}$ | Line blanking voltage | | 4.25 | 4.5 | 4.75 | V |
| $V_{15F}$ | Frame blanking voltage | | 2.38 | 2.5 | 2.63 | V |
| $I_{15}$ | Input current during line flyback | | | 0.1 | | mA |
| $t_{KS}$ | Phase relationship between leading edge of key pulse and middle of sync. pulse | | | 2.4 | | µs |
| $t_K$ | Key pulse duration | | | 4 | | µs |

## ELECTRICAL CHARACTERISTICS (continued)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **FRAME** | | | | | | |
| $V_{17}$ | Peak to peak | 50 Hz | | 2.95 | | V |
| | Sawtooth voltage | 60 Hz | | 2.45 | | V |
| $V_{17}$ | Regulated voltage | | | 3.3 | | V |
| $V_{20}$ | Output p.p. sawtooth voltage | 50 Hz and 60 Hz | | 2.95 | | V |
| $V_{20}$ | Saturation voltage | | | 0.2 | | V |
| **LINE** | | | | | | |
| $I_7$ | Output current | | | 50 | | mA |
| $V_7$ | Saturation voltage | $I_7$ = 50 mA | | 0.4 | | V |
| $t_L$ | Output pulse duration | | | 29 | | µs |
| **FRAME FREQUENCY SWITCH (50/60 Hz)** | | | | | | |
| $V_{21}$ | Output voltage | 50 Hz | | 11.9 | | V |
| | | 60 Hz | | 7 | | V |
| | | Unlock | | 0.3 | | V |
| **OVERALL PHASE RELATIONSHIP** | | | | | | |
| $t_o$ | Phase difference between middle of flyback and middle of sync pulses | | | 2 | | µs |

## CIRCUIT OPERATION

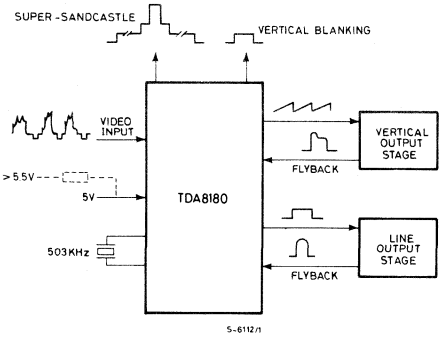
Intended for use in televisions and monitors, the TDA 8180 Deflection Processor separates synchronization pulses from a composite video signal and generates drive waveforms for the horizontal and vertical output stages. It also generates a super-sandcastle signal for the chroma section plus a separate vertical blanking signal.
Frequency and phase adjustments are eliminated completely by the use of digital timing circuitry. PLL synchonization and automatic phase control. A single 503 kHz resonator satisfies all timing requirements.

The TDA 8180 is capable of operating with both the European and US broadcasting standards (USA 15750 lines/sec, 60 fields/sec; EUROPE 15625 lines/sec, 50 fields/sec). It can also be used in monitors or displays using either of these standards and is specially designed to function well with videocassette recorders (VCRs).

The TDA 8180 adapts automatically to the received signal: the line frequency is synchronized by a phaselocked loop, all timing signals are derived by counters from the PLL oscillator and the counter which controls vertical deflection timing is reset by vertical sync pulses. Moreover, the TDA 8180 identifies the field scanning frequency of the input signal (50 or 60 Hz) and automatically adjusts the amplitude of the vertical sawtooth to maintain a constant picture height. An output is provided to indicate when the device is synchronized and whether the input signal has a field frequency of 50 or 60 Hz. This output may be used to control the tuner section and/or to mute the sound channel.

## CIRCUIT OPERATION (continued)

Fig. 1 - The TDA 8180 separates sync pulses from the input signal and controls external deflection power stages.




Also included in the TDA 8180 are CRT protection circuits which generate continuous blanking if either flyback signal is missing, plus a general purpose protection circuit which may be used, for example, to turn off the line output stage when the beam current exceeds a safe value.

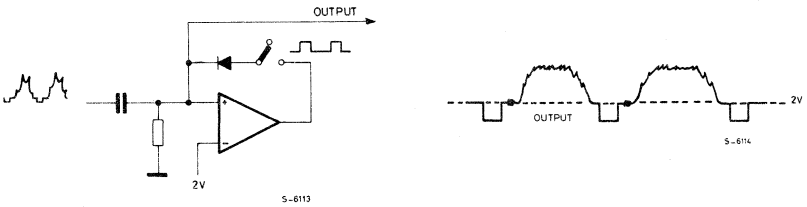
To reduce consumption and the dimensions of the die, the TDA 8180 is realized with a low voltage process and operates directly on a 5V supply. An internal shunt regulator allows operation on higher supply voltages with the addition of a series resistor.

### SYNC SEPARATORS

Sync pulses are separated from the video signal by a circuit which 'slices' the signal at 50% of the sync amplitude, irrespective of the input signal level. This ensures excellent immunity against noise on weak signals. To establish the 50% level, the black level of the video signal is clamped to a constant level by a gated clamping circuit. This circuit is controlled by the 4 $\mu$s brust key pulse and thus samples the black level on the back porch.

Vertical sync pulses are obtained by integrating the separated sync pulses and locating the exact beginning of each field with a peak detector.

Fig. 2 - This gated clamper defines the black level of the TDA 8180's sync separator.

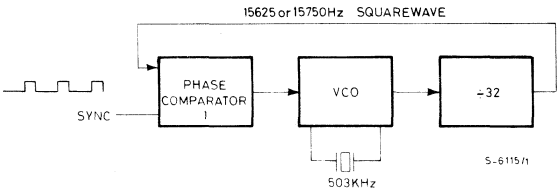


## CIRCUIT OPERATION (continued)

### LINE SYNCHRONIZATION

The TDA 8180's internal oscillator is locked to the incoming sync pulses by a phase-locked loop (PLL) consisting of phase comparator 1, the oscillator (voltage controlled) and a 5-bit counter. When this loop is locked the oscillator runs at exactly 32 times the line frequency (500 kHz for the 15625 Hz European standard; 504 kHz for 15750 Hz US standard). Internal timing signals are obtained by decoding logic on the outputs of the five-bit counter. The high oscillator frequency is chosen to provide high resolution.

Fig. 3 - Line sync phase-locked loop.




When the line sync PLL is locked the line lock detector, which looks for a coincidence between the sync pulses and 15625 Hz (or 15750 Hz) 4 $\mu$s pulses from the counter, reduces the sensitivity of the phase comparator and its time constant. The loop is thus 'sensitive' when out of lock to allow fast locking, yet insensitive to interference when locked. An external capacitor defines the time constant of the line lock detector and thus determines how long the line sync PLL must be locked before the sensitivity is reduced. In addition, horizontal sync pulses are gated when the PLL is in lock and are accepted only when they occur in an 8 $\mu$s window in the horizontal blanking interval.

If the line sync PLL is out of lock the condition is signalled by a low level at the sync status output. Vertical sync pulses are ignored in this condition and the vertical scanning rate obtained directly from the VCO by division.

For VCR operation the action of the line lock detector can be suppressed by a switch which bypasses the time constant capacitor. The device thus remains in the sensitive state and can follow frequency variations of the input signal (caused by tape speed fluctuations) without losing lock. In this condition the sync status output always indicates either "50 Hz" or "60 Hz".

The decoding logic connected to the 5-bit counter provides a 4 $\mu$s colour burst key pulse (used for the super-sandcastle and gated clamper), an 8 $\mu$s pulse for the horizontal ramp discharge and a 4 $\mu$s pulse used for lock and flyback coincidence detection.

The horizontal drive output supplies a 29 $\mu$s pulse derived from a sawtooth, rather than directly from the logic, to allow dynamic phase correction while keeping the duty cycle constant. Phase correction is performed by a phase shifter in the horizontal output circuit. This is controlled by phase comparator 2 which compares the internal drive signal with horizontal flyback, thus compensating for the phase shift introduced by the line output stages. Static phase correction may be added if desired by a voltage applied to the phase shift filter pin (pin 6).

## CIRCUIT OPERATION (continued)

### VERTICAL TIMING

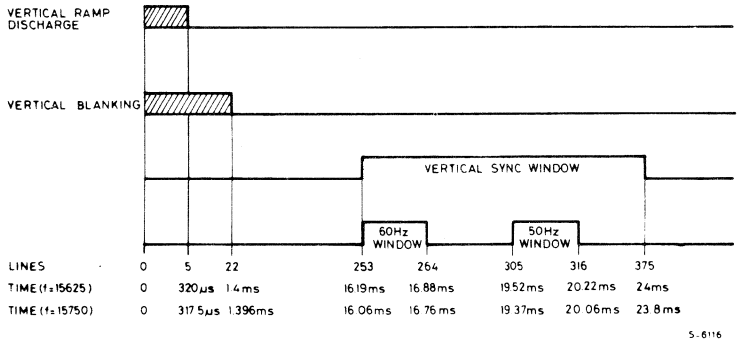
Line frequency squarewave pulses from the line sync PLL are further divided by a nine-bit counter which has four basic functions:

- generation of vertical timing signals (ramp discharge and blanking)
- sync pulse gating to improve noise immunity
- identification of 50 or 60 Hz field frequency
- generation of vertical scanning rate by fixed ratio division from line frequency when sync is too weak.

In normal steady-state operation when the device is fully synchronized each vertical sync pulse resets the counter (after 16.67 ms for 60 Hz, 20 ms for 50 Hz). Decoding logic on the counter generates the vertical ramp discharge and vertical blanking signals at appropriate times.

To enhance noise immunity the sync pulses are gated by the counter so that they are accepted (to reset the counter) only when they occur in a "window". Initially, when the line PLL is locked but vertical synchronization is out of lock the sync pulses are gated by a broad window covering the period 16-24 ms. If a vertical sync pulse occurs within this broad window the counter is reset and the next sync pulse must occur in the window; the vertical scan is synchronized. In contrast, if the sync pulse occurs outside of the window it is ignored. In this condition the counter resets itself after 24 ms, a time chosen to ensure that synchronization will be achieved as soon as possible.

Fig. 4 - Vertical counter timing

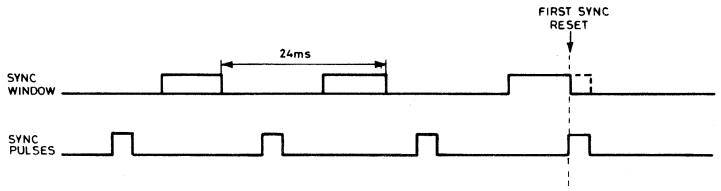



Inside the broad window there are two smaller windows used to identify the field frequency. The first covers the period 16-17 ms (for 60 Hz signals); the second covers the period 19.5-20.2 ms (for 50 Hz signals). After the first sync-generated reset (as opposed to a 24 ms auto reset) the next true sync will occur in one of these windows. If it occurs in the first the counter is reset and a "1" is clocked into a 3-bit shift register; if it occurs in the second the counter is reset and a "1" is clocked into a 2-bit shift register. A majority logic network compares the outputs of these shift registers to determine whether the signal is 50 Hz or 60 Hz. In addition, when all bits of one shift register are set (when two successive 50 or three successive 60 Hz pulses have been accepted) the sync gating window is reduced from the 16-25 ms broad period to the duration of the appropriate short window. Spurious pulses occurring at any other time are thus ignored.

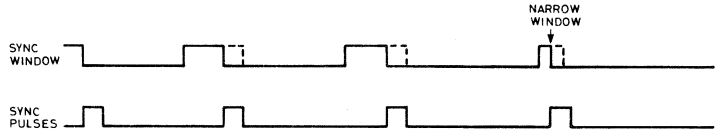
## CIRCUIT OPERATION (continued)

In this fully locked condition, if one vertical sync pulse is missed, the counter generates its own reset at the end of the window (ie. at 16.7 ms in 60 Hz mode; at 20.22 ms in 50 Hz mode). The next sync pulse will therefore be slightly advanced but still within the short window. If two or more sync pulses are missed the vertical timing logic is restored to the initial broad window condition to regain lock rapidly.

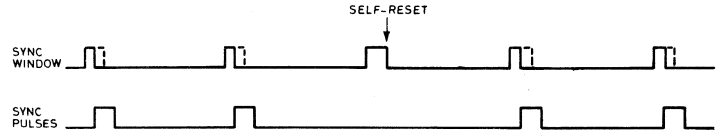
Fig. 5 - Vertical synchronization



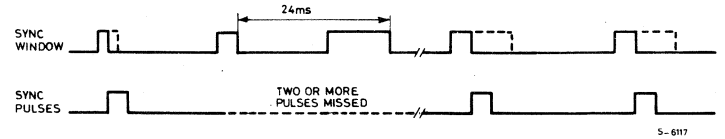

1. 24 ms self-reset for fast lock.




2. After two 20 ms pulses (or three 16.67 ms pulses) the TDA 8180 reduces the width of the sync gating window.




3. Digital "flywheel" effect tolerates loss of one pulse.




4. If two pulses are missed the window is expanded and a self-reset at 24 ms restores lock rapidly.

## CIRCUIT OPERATION (continued)

When the line sync PLL is in the out of lock condition, vertical sync pulses are completely ignored and the counter always resets itself after 20.22 ms. The purpose of this is to obtain a slowly rolling recognisable picture with very weak signals, avoiding irritating frame jumps that would be caused by attempting to lock the signal.

In VCR mode, the vertical timing logic ignores the lock status of the line PLL, assuming that it is locked. The slow rolling function (auto-reset at 20.2 ms) is therefore disabled. In this condition the sync status output always indicates either "50 Hz" or "60 Hz", never that the line PLL is out of sync.

### Table 1 - Vertical synchronization

| | CONDITION | ACTION |
|---|---|---|
| 1 | LINE PLL OUT OF LOCK | Vertical sync pulses ignored. Counter resets itself at 20.22 ms to give rolling picture. |
| 2 | LINE PLL LOCKED, VERTICAL SCANNING OUT OF LOCK | Vertical sync pulse will reset counter if it occurs in 16-24 ms broad window. Otherwise counter resets itself at 24 ms to achieve lock rapidly. |
| 3 | LINE PLL LOCKED, VERTICAL SCANNING IN "COARSE" LOCK | Vertical sync pulses always occur in broad window and reset counter. Occurances of sync pulses in small 60 Hz and 50 Hz windows counted to identify frequency. After two successive 50 Hz or 3 successive 60 Hz pulses the broad window is suppressed and circuit switches to condition 4.* |
| 4 | LINE PLL LOCKED. VERTICAL SCANNING IN "FINE" LOCK | Vertical sync pulses reset counter only if they occur in appropriate short window. If one pulse is missed, counter resets itself at end of short window. If two or more pulses missed, device returns to condition 3 to regain vertical lock. |

* Except in VCR mode.

### PROTECTION CIRCUITS

To protect the CRT against failures of the vertical output stage or deflection coil the TDA 8180 compares the vertical drive signal with the vertical flyback signal. If they do not coincide continuous blanking is generated. Similarly, if the horizontal flyback signal does not coincide with the recreated sync pulses (4 $\mu$s pulses from the line timing logic) continuous blanking is generated.

## CIRCUIT OPERATION (continued)

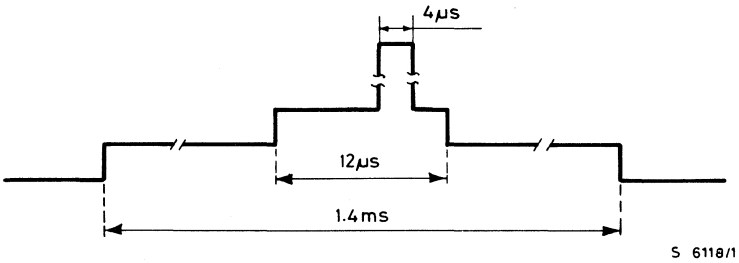
In addition, a general purpose protection flip flop is provided to disable the horizontal output drive. This may be used by the designer for any purpose. When power is applied to the device this flip flop is reset. Grounding the protection input sets the flip flop, turning off horizontal drive. The flip flop is reset by removing the supply. Since the horizontal drive signal is disabled, horizontal flyback will cease, therefore continuous blanking will be generated.

### SUPER-SANDCASTLE & BLANKING

The super-sandcastle signal consists of vertical blanking and key pulse waveforms from the logic circuitry plus a horizontal blanking signal derived from the horizontal flyback signal. The horizontal flyback input has two thresholds, located at about 1.2V and 4.9V. The lower threshold is used for horizontal blanking; the upper threshold is used for the dynamic phase correction loop.

In addition to the super--sandcastle, a separate vertical blanking signal is provided for applications not requiring the super-sandcastle.

Fig. 6 - Super-sandcastle waveform.




### SUPPLY

The TDA 8180 may be operated on a 5V supply directly. A 5.5V shunt regulator is available internally for operation on higher supply voltages. In this case an external limiting resistor is needed. When no resistor is fitted care must be taken to ensure that the supply voltage does not exceed 5.5V or the regulator will intervene, possibly damaging the device.

Fig. 7 - Application circuit

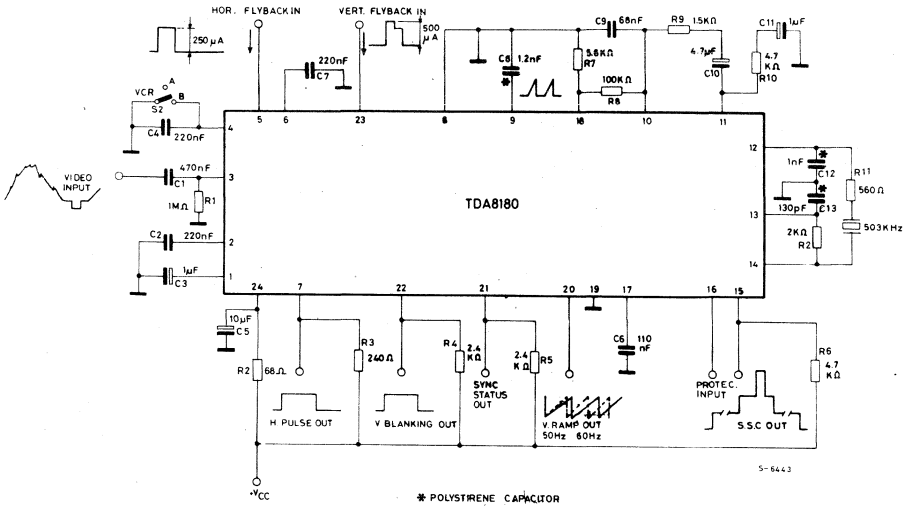
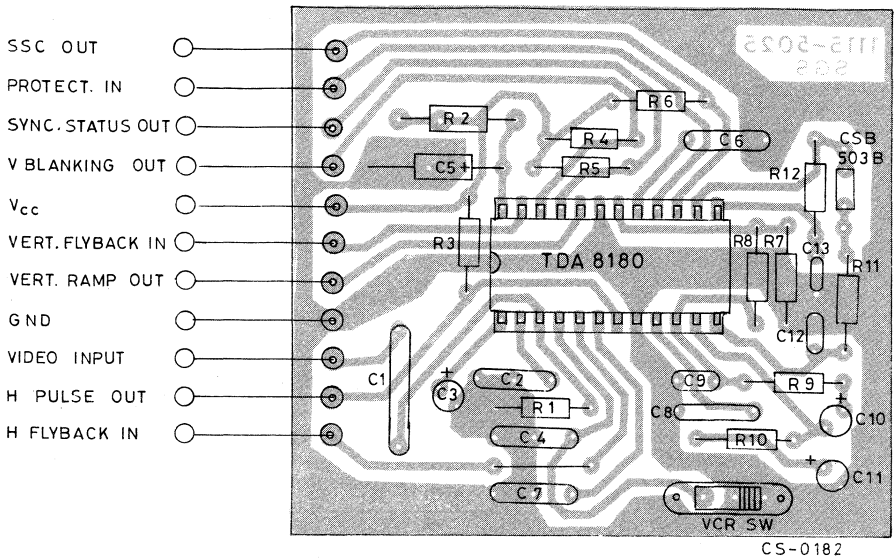



Fig. 8 - P.C. board and component layout of the circuit of fig. 7 (1:1 scale)



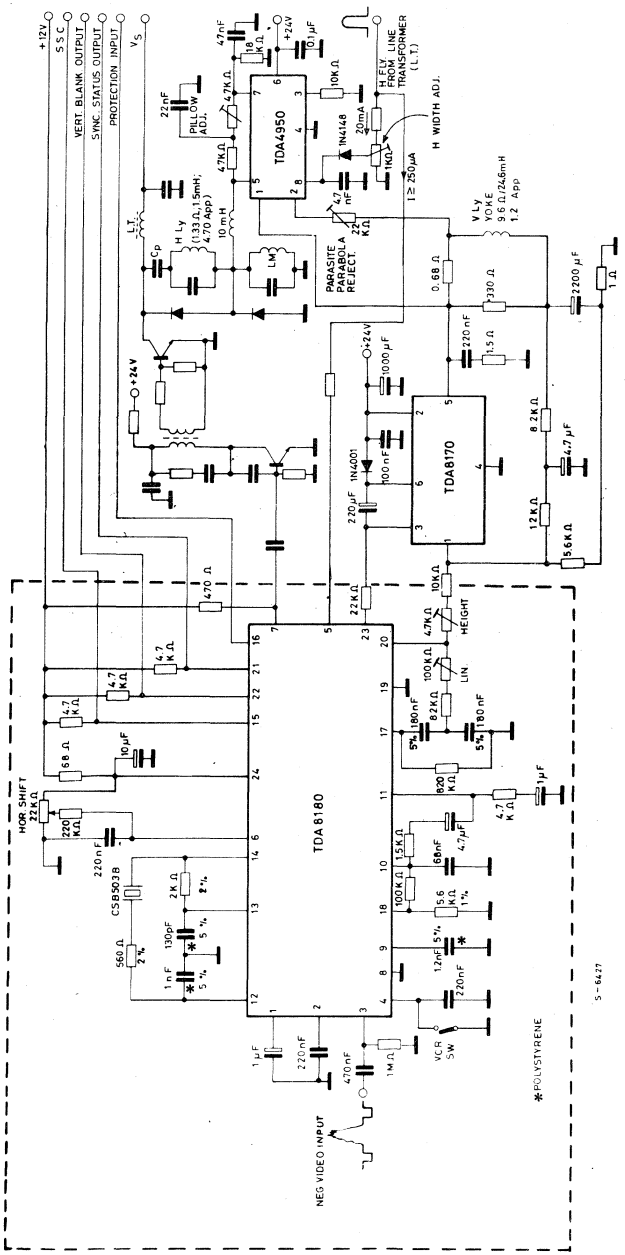



Fig. 9 - Complete deflection circuit

# LINEAR INTEGRATED CIRCUITS

**TDA8190**

## TV SOUND CHANNEL WITH DC CONTROLS

**ADVANCE DATA**

- SEPARATE VCR INPUT AND OUTPUT PINS
- 4W OUTPUT POWER INTO 16Ω
- NO SCREENING REQUIRED
- HIGH SENSITIVITY
- EXCELLENT AM REJECTION
- LOW DISTORTION
- DC TONE/VOLUME CONTROLS
- THERMAL PROTECTION

The TDA8190 is a complete TV sound channel with DC tone and volume controls plus separate VCR input and output connections. Mounted in a Powerdip 16 + 2 + 2 package, the device delivers an output power of 4W into 16Ω (d = 10%, $V_s$ = 24V) or 1.5W into 8Ω (d = 10%, $V_s$ = 12V). Included in the TDA8190 are: IF amplifier limiter, active low-pass filter, AF preamplifier and power amplifier, turnoff muting, mute circuit and thermal protection.

High output, high sensitivity, excellent AM rejection and low distortion make the device suitable for use in TVs of almost every type. Further, no screening is necessary because the device is free of radiation problems.

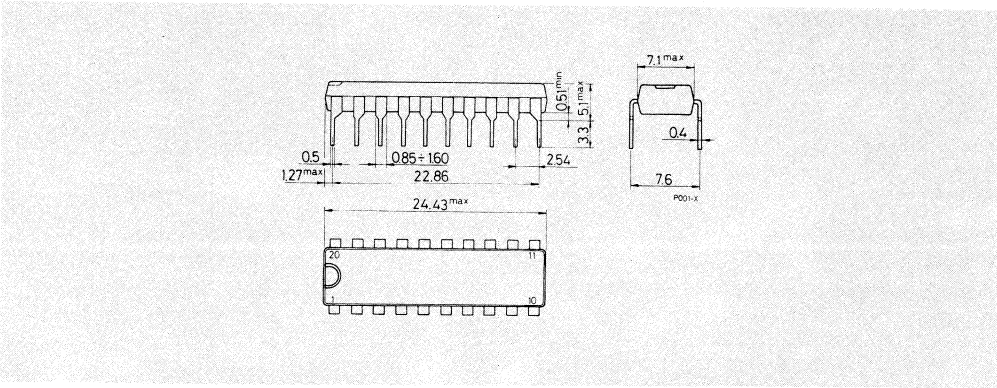
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage (pin 18) | 28 | V |
| $V_l$ | Voltage at pin 1 | $\pm V_s$ | |
| $V_i$ | Input voltage (pin 2) | 1 | Vpp |
| $I_o$ | Output peak current (repetitive) | 1.5 | A |
| $I_o$ | Output peak current (non repetitive) | 2 | A |
| $I_4$ | Current (pin 4) | 10 | mA |
| $P_{tot}$ | Power dissipation at $T_{pins}$ = 90°C | 4.3 | W |
| | at $T_{amb}$ = 70°C | 1 | W |
| $T_{stg}$-$T_j$ | Storage and junction temperature | -40 to 150 | °C |

**ORDERING NUMBER:** TDA8190

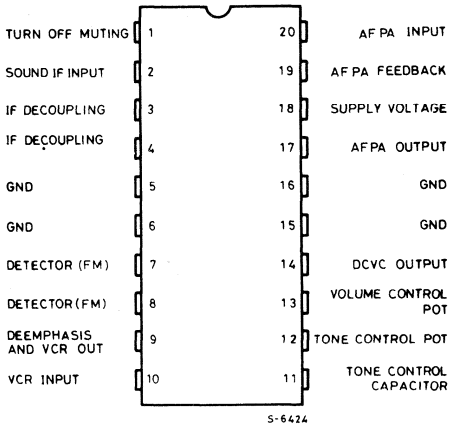
## MECHANICAL DATA

Dimensions in mm

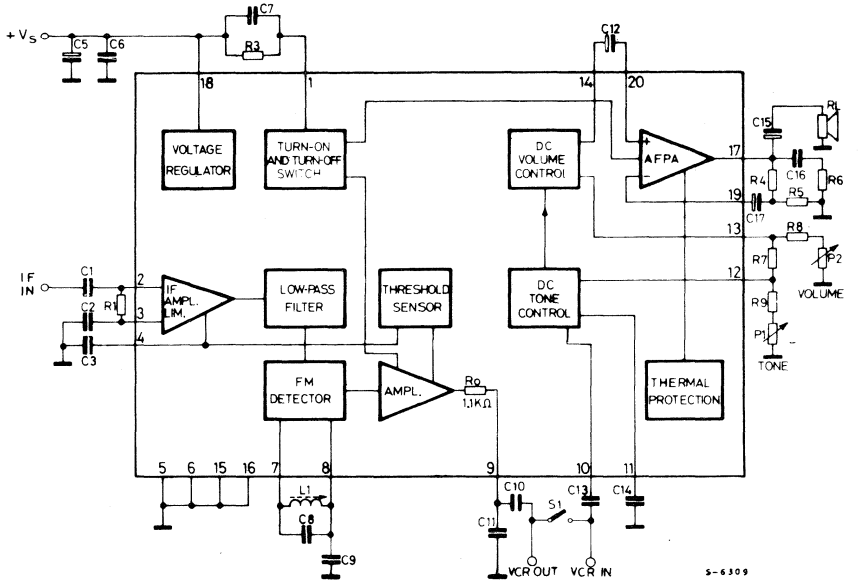


# TDA8190

## CONNECTION DIAGRAM




## BLOCK DIAGRAM




## THERMAL DATA

| | | |
|---|---|---|
| $R_{th\ j\text{-}pins}$ | Thermal resistance junction-pins | max 14 °C/W |
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max 80 °C/W* |

(*) Obtained with GND pins soldered to printed circuit with minimized copper area.

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_s$ = 24V, S1: on, $\Delta f$ = ±25 KHz, $V_i$ = 1mV, $P_1$ = 12 KΩ, $f_o$ = 4.5 MHz, $f_m$ = 400 Hz, $T_{amb}$ = 25°C, unless otherwise specified)

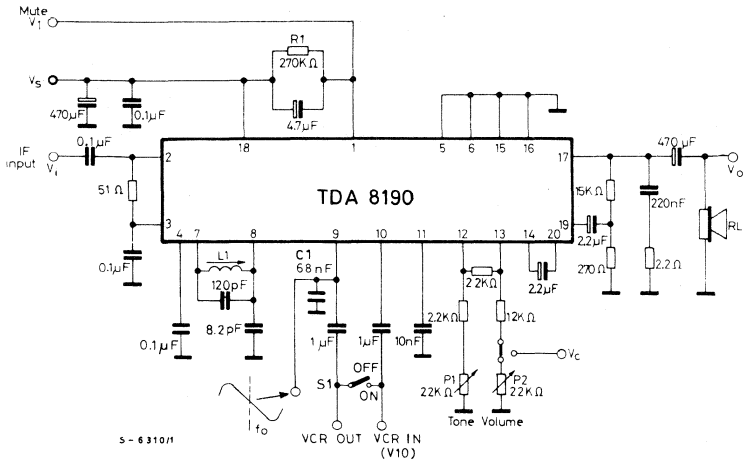
| Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **DC CHARACTERISTICS** | | | | | |
| $V_s$ Supply voltage (pin 18) | $P_2$ = 12 KΩ | 10.8 | | 27 | V |
| $V_o$ Quiescent output voltage (pin 18) | $P_2$ = 12 KΩ | 11 | 12 | 13 | V |
| $V_1$ Pin 1 DC Voltage | $P_2$ = 12 KΩ $R_1$ = 270 KΩ | | 5.3 | | V |
| $V_4$ Pin 4 DC voltage | $P_2$ = 12 KΩ | | 3.2 | | V |
| $I_d$ Quiescent drain current | $P_2$ = 12 KΩ | | 32 | | mA |
| **IF AMPLIFIER AND DETECTOR** | | | | | |
| $V_{i\ (threshold)}$ Input limiting voltage at pin 2 (-3 dB) | $V_o = 4\ V_{rms}$ | | 50 | 100 | μV |
| $V_9$ Recovered audio voltage (pin 9) | $\Delta f$ = ± 7.5 KHz $P_2$ = 12 KΩ | 140 | 200 | 280 | mV |
| AMR Amplitude modulation rejection (*) | m= 0.3; $V_i$ = 1 mV; $V_o = 4V_{rms}$ | | 60 | | dB |
| $R_i$ Input resistance (pin 2) | $\Delta f$ = 0 $P_2$ = 12 KΩ | | 30 | | KΩ |
| $C_i$ Input capacitance (pin 2) | $\Delta f$ = 0 $P_2$ = 12 KΩ | | 6 | | pF |
| $R_9$ Deemphasis resistance | $C_1$ = 68 to 888 nF | 0.75 | 1.1 | 1.5 | KΩ |
| **DC VOLUME CONTROL** | | | | | |
| $K_V$ Volume attenuation (resistance control) | $P_2$ = 0Ω<br>$P_2$ = 4.3 KΩ<br>$P_2$ = 12 KΩ | 20 | 0<br>26<br>88 | 32 | dB<br>dB<br>dB |
| $V_c$ Control voltage | K = 0 dB<br>K = 26 dB<br>K = 88 dB | | 0<br>1.3<br>2.6 | | V<br>V<br>V |
| $\frac{\Delta K_V}{\Delta T_{pins}}$ Volume attenuation thermal drift (resistance control) | $T_{pins}$ 25 to 85°C<br>$P_2$= 4.3 KΩ | | -0.05 | | $\frac{dB}{°C}$ |
| **DC TONE CONTROL** | | | | | |
| $K_T$ Tone cut | S1 : off<br>$V_{10}$ = 200 mV<br>$P_1$ = 12 KΩ to 100 Ω<br>$f_{AF}$= 10 KHz | | 14 | | dB |

## ELECTRICAL CHARACTERISTICS (Continued)

| Parameter | | Test conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **AUDIO FREQUENCY AMPLIFIER** | | | | | | | |
| $P_o$ | Output power (d = 10%) | $V_s$ = 24V<br>$V_s$ = 12V | $R_L$ = 16Ω<br>$R_L$ = 8Ω | 3.5 | 4.1<br>1.5 | | W<br>W |
| B | Frequency response of audio amplifier (-3dB) | $P_o$ = 1W<br>S1 : off<br>$V_{10}$ = 200mV | $R_L$ = 16Ω<br>$V_o$=4Vrms@400Hz | 15 | 50 | | KHz |
| SVR | Supply voltage rejection | $P_2$ = 12KΩ Δf= o $f_{ripple}$ = 120Hz | | | 26 | | dB |
| **V.C.R.** | | | | | | | |
| d | Total harmonic distortion of pin 9 output signal | Δf = ± 7.5 KHz<br>$V_i$ = 1 mV | | | 0.5 | | % |
| SVR | Supply voltage rejection at output pin 9 | Δf = 0;<br>$P_2$= 12 KΩ | $f_{ripple}$= 120 Hz | | 66 | | dB |
| $\frac{S+N}{N}$ | Signal and noise to noise ratio at output pin 9 | Δf = ± 25 KHz<br>$V_i \geq$ 1 mV | | | 70 | | dB |
| $V_{10}$ | Input voltage (playback) | $V_o$= 4 $V_{rms}$ | $P_2$ = 0<br>S1 : off | 50 | 70 | 100 | mV |
| $R_{10}$ | Input resistance (playback) | | S1 : off | 10 | | | KΩ |
| d | Total harmonic distortion for 20 dB overload of $V_{10}$ | $V_{10}$ = 1 $V_{rms}$ | S1 : off<br>$V_o$ = 4 $V_{rms}$ | | 0.5 | 2 | % |
| **OVERALL CIRCUIT** | | | | | | | |
| $\frac{S+N}{N}$ | Signal to noise ratio (*) | $V_i \geq$ 1mV<br>Δf = 0 | $V_o$ = 4$V_{rms}$ | | 70 | | dB |
| d | Distortion (*) | $P_o$ = 50mW<br>$V_s$ = 24V<br>$V_s$ = 12V | Δf = ± 7.5Hz<br>$R_L$ = 16Ω<br>$R_L$ = 8Ω | | 0.5<br>0.5 | | %<br>% |
| M | Muting (*) | $V_o$ = 4$V_{rms}$ @ no $V_1$; $V_1$ = 0 | | 100 | | | dB |
| Δf | Deviation sensitivity | $P_2$ = o | $V_o$ = 4$V_{rms}$ | | 3 | 6 | KHz |

* Test Bandwidth = 20 KHz.

## TEST CIRCUIT




## TEST CONDITIONS (unless otherwise specified)

$V_s$ = 24V; $Q_o$ = 60; $f_o$ = 4.5 MHz;
$V_{in}$ = 1 mV; $f_m$ = 400 Hz; $\Delta f$ = ±25 KHz;
$P_1$ = 12 KΩ; $R_L$ = ∞ ; S1 = on

Fig. 1 - Relative audio output voltage and output noise vs. input signal.

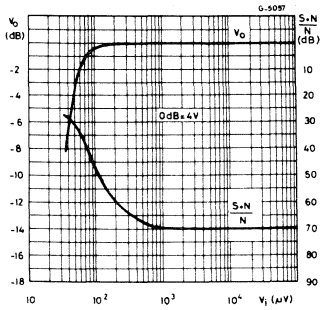



Fig. 2 - Output voltage alternation vs. DC volume control resistance (a) or Vs. DC volume control voltage (b)

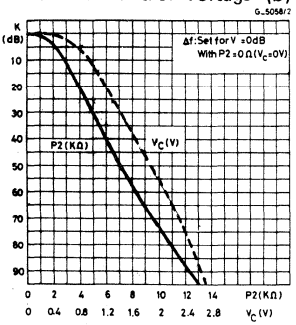



Fig. 3 - DC tone control cut of the high audio frequencies for some values of resistance adjusted by P1.

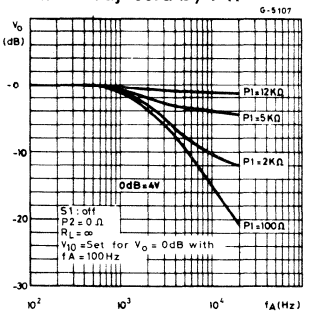


Fig. 4 - Amplitude modulation rejection vs. input signal.

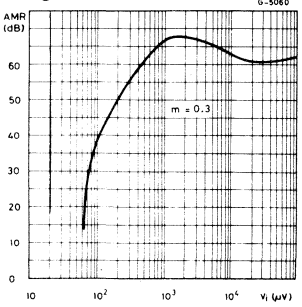



Fig. 5 - ΔAMR vs. timing frequency change

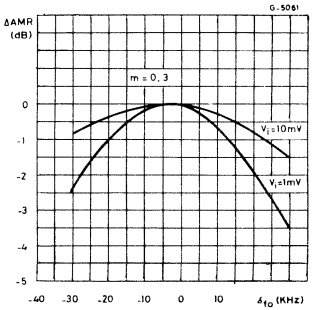



Fig. 6 - Recovered audio voltage vs. unloaded Q-factor of the detector coil

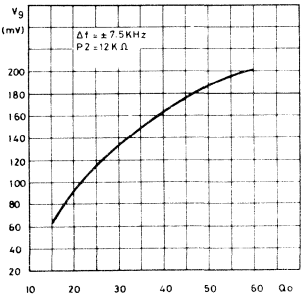



Fig. 7 - Distortion vs. unloaded Q-factor of the detector coil.

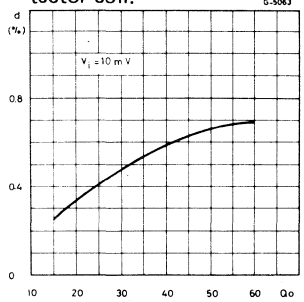



Fig. 8 - Distortion vs. frequency variation

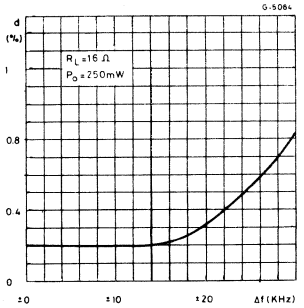



Fig. 9 - Distortion vs. tuning frequency change

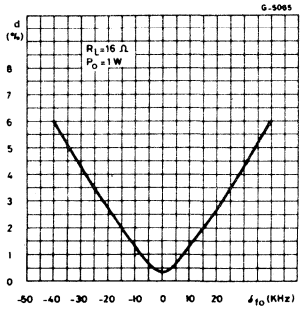



Fig. 10 - Distortion vs. output power

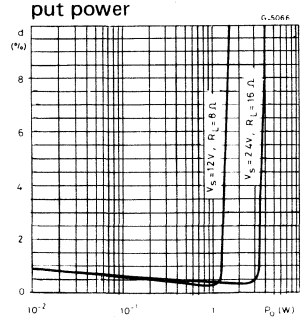



Fig. 11 - Audio amplifier frequency response

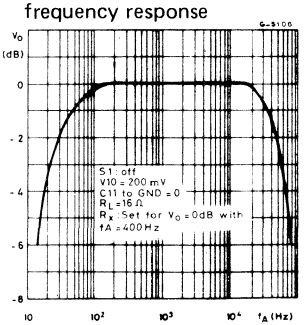



Fig. 12 - Output power vs. supply voltage.

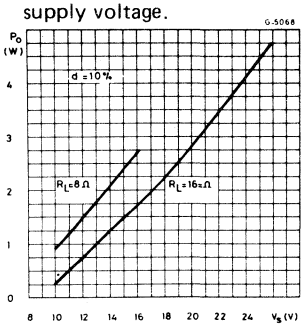


Fig. 13 - Power dissipation vs. supply voltage (sine wave operation).

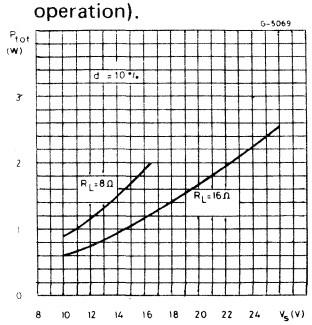



Fig. 14 - Power dissipation and efficiency vs. output power

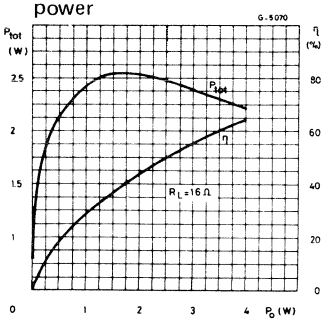
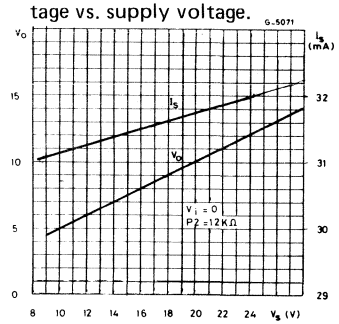



Fig. 15 - Quiescent drain and quiescent output voltage vs. supply voltage.




## APPLICATION INFORMATION (Refer to the block diagram)

### IF Amplifier-limiter

It is made by six differential stages of 15dB gain each so that an open loop gain of 90dB is obtained.

While a unity DC gain is provided, the AC closed loop gain is internally fixed at 70dB that allows a typical input sensitivity of 50 $\mu$V.

The differential output signal is single ended by a 20dB gain amplifier that through a buffer stage, feeds the detector system.

Internal diodes protect the inputs against overloads.

- Pin 2 if the IF non-inverting input
- Pin 3 is decoupled by a capacitor to open the AC loop
- Pin 4 grounded by a capacitor, allows a typical sensitivity of 50 $\mu$V. (See VCR facility too).

### Low-pass filter, FM detector and amplifier

The IF signal is detected by converting the frequency modulation into amplitude modulation and then detecting it.

Since the available modulated signal is a square wave, a 40dB/decade low-pass filter cuts its harmonics so that a sine wave can feed the two-resonances external network L1, C8 and C9.

This network defines the working frequency value, the amplitude of the recovered audio signal and its distortion at the highest frequency deviations.

The two resonances f1 (series resonance) and f2 (parallel resonance) can be computed respectively by:

$$X_{C9} = \frac{X_{L1} \cdot X_{C8}}{X_{L1} + X_{C8}} \quad \text{and} \quad X_{L1} = X_{C8}$$

The ratio of these frequencies defines the peak-to-peak separation of the "S" curve:

$$\frac{f2}{f1} = \sqrt{1 + \frac{C_9}{C_8}}$$

## APPLICATION INFORMATION (continued)

A differential peak detector detects the audio frequency signal that amplified, reaches the deemphasis network R0; C11.

The AF amplifier can be muted (see turn-on and turn-off switch and VCR facility).

- Pin 7 is the output of the low-pass filter and one input of the differential peak detector
- Pin 8 is the other input of the differential peak detector
- Pin 9 is used to provide the required deemphasis time constant by grounding it with C11. At this pin, the internal impedance of which is typically of 1.1 KΩ, is available the recovered audio signal as auxiliary output.

### DC Tone Control

The same signal available or applied to pin 10, after a voltage to current converter, reaches, the DC Tone Control block. It operates, inside the 10 KHz bandwidth, by cutting the high audio frequencies with a variable slope of an RC network, by means of $P_1$.

The maximum slope of the RC network is of 20dB per decade and its pole is defined by:

$X_{C11}$ = 6.8KΩ, tipically.

Pin 11 – At this pin is tied the tone capacitor.

Pin 12 – is the DC Tone Control input.

### DC Volume Control

After tone control regulation, the AF current signal reaches the DC volume control block that controls its intensity. The normal control, for which the block has been designed for a narrow spread, is produced by P2; however, without P2, a voltage control can be operated by forcing a voltage at pin 13 through R8.

- Pin 12, already seen as a DCTC input, is the reference voltage for the DCVC. Because of this, a small interface between tone and volume regulation can be expected.
- Pin 13 is the DC volume control input.
- Pin 14 after a current to voltage converter, the audio frequency signal comes out at this pin.

### Audio Frequency power amplifier and thermal protection

Through C12 the signal reaches the amplifier non-inverting input. The closed loop gain is defined by the feedback at pin 19 (inverting input) or by the ratio:

$$G_v = 20 \text{ Log } \frac{R5 + R4}{R5} \text{ (dB)}$$

The amplifier, thermally protected, can supply 4W of power into a 16Ω load with 24V of supply voltage. The power output stage is a class B type.

- Pin 20 is the non-inverting input
- Pin 19 is the inverting input
- Pin 17 is the output of the AFPA.

## APPLICATION INFORMATION (continued)

### Turn-on and turn-off switch

This block has been mainly designed to avoid, turning on the TV set, that transients, produced by the vision output, can reach the speaker.

Moreover this block, together an optimized rise time and full time of the supply voltage $V_s$, can avoid any pop generally produced during the turn-on and the turn-off transients.

Turning on, pin 1 follows the supply voltage $V_s$ by means of C7; a threshold is reached and the muting of the AFPA output (pin 17) is suddenly produced.

When $V_s$ reaches it stop, C7 charges itself through the input impedance of pin 1 and the muting is removed with a time constant depending on the C7 value.

Turning off, the $V_s$ trend, in series to the voltage $V_s$-$V_1$ and which C7 is charged, drives pin 1 at a low level threshold and a sudden muting is produced again.

Since the turn-off can be operated with high output power, if the muting operates when the current through the inductance of the speaker is different from zero, a flyback is generated and then a small pop can be produced.

The flyback is clipped by integrated diodes.

The thresholds that produce the muting have been chosen in the way that 1Vpp of ripple on the supply voltage does not produce any switching.

By shorting pin 1 to ground through a 10 KΩ resistor the muting can be obtained.

– Pin 1 is the turn-on and turn-off muting input.

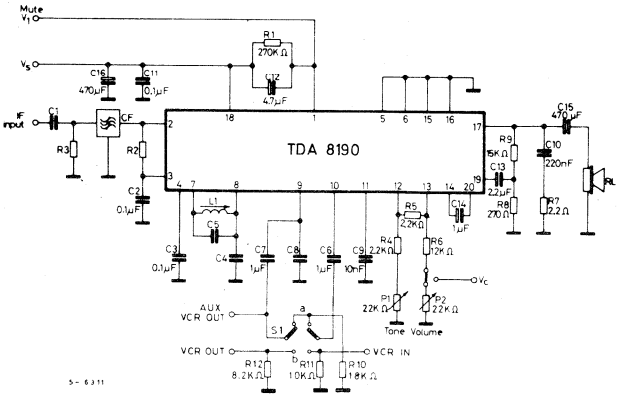
### Supply

An integrated voltage regulator with different output levels, supplies all the blocks operating with small signal.

– Pin 18 is the main supply of the device.

– Pin 5; pin 6; pin 15 and pin 16 are the ground of the supply. These pins are used to drain out from the device the heat produced by the dissipated power.

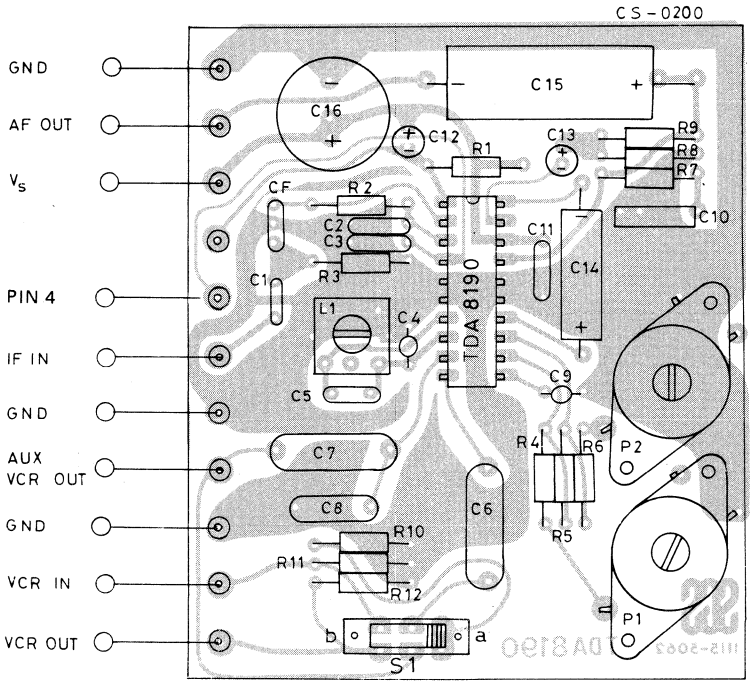
Fig. 16 - Application circuit



## APPLICATION INFORMATION (continued)

| Components | Units | Appl. 4.5 MHz | Appl. 5.5 MHz | Appl. 6 MHz |
|---|---|---|---|---|
| L1 | μH | 10<br>$Q_o$ = 60 | 12<br>$Q_o$ = 80 | 10<br>$Q_o$ = 70 |
| C5 | pF | 120 | 68 | 68 |
| C4 | pF | 9 | 8.2 | 6.8 |
| C8 | nF | 68 | 47 | 47 |
| C.F. | — | Murata SFE 4.5 MA | Murata SFE 5.5 MB | Murata SFE 6.0 MB |
| C1 | pF | 22 | 18 | 18 |
| R2 | Ω | 1000 | 560 | 470 |
| R3 | Ω | 1000 | 560 | 470 |

Fig. 17 - PC board and components layout of the circuit of fig. 16 (1:1 scale)



# LINEAR INTEGRATED CIRCUITS

**TEA1330**

PRELIMINARY DATA

## FM STEREO DECODER

- REQUIRES NO INDUCTORS
- LOW EXTERNAL PART COUNT
- ONLY OSCILLATOR FREQUENCY ADJUSTMENT NECESSARY
- INTEGRAL STEREO/MONAURAL SWITCH WITH HIGH LAMP DRIVING CAPABILITY
- WIDE SUPPLY RANGE: 3V TO 14V
- EXCELLENT CHANNEL SEPARATION MAINTAINED OVER ENTIRE AUDIO FREQUENCY RANGE
- LOW DISTORTION: TYPICALLY 0.3% AT 150 mV (RMS) COMPOSITE INPUT SIGNAL
- EXCELLENT SCA REJECTION (76 dB TYP.)

The TEA 1330 is a monolithic decoder circuit for FM stereo transmissions. Packaged in a 16-pin DIP, it functions with very few external components and requires no inductors.

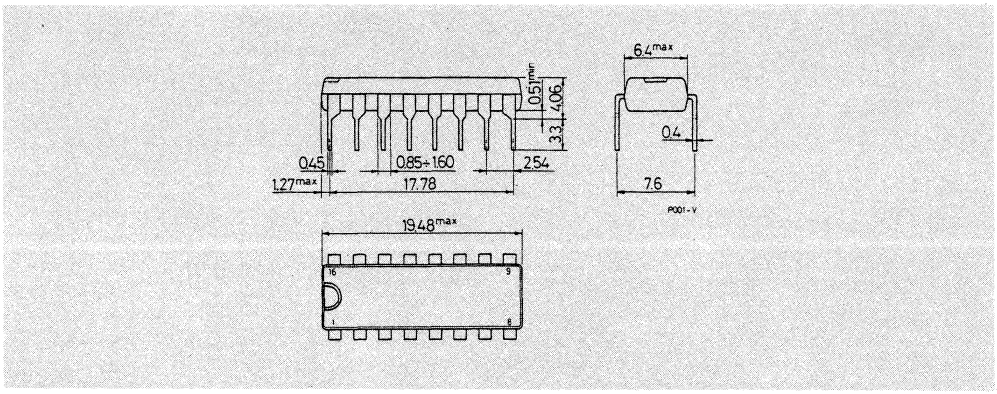
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_s$ | Supply voltage | 16 | V |
| $I_L$ | Lamp current | 75 | mA |
| $P_{tot}$ | Power dissipation $T_{amb}$ = 70°C | 800 | mW |
| $T_{op}$ | Operating temperature | -25 to 75 | °C |
| $T_{stg}$ | Storage temperature | -55 to to 150 | °C |

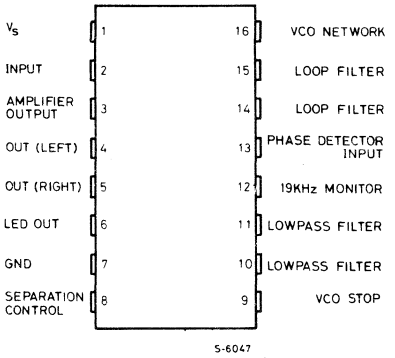
**ORDERING NUMBER:** TEA 1330

## MECHANICAL DATA

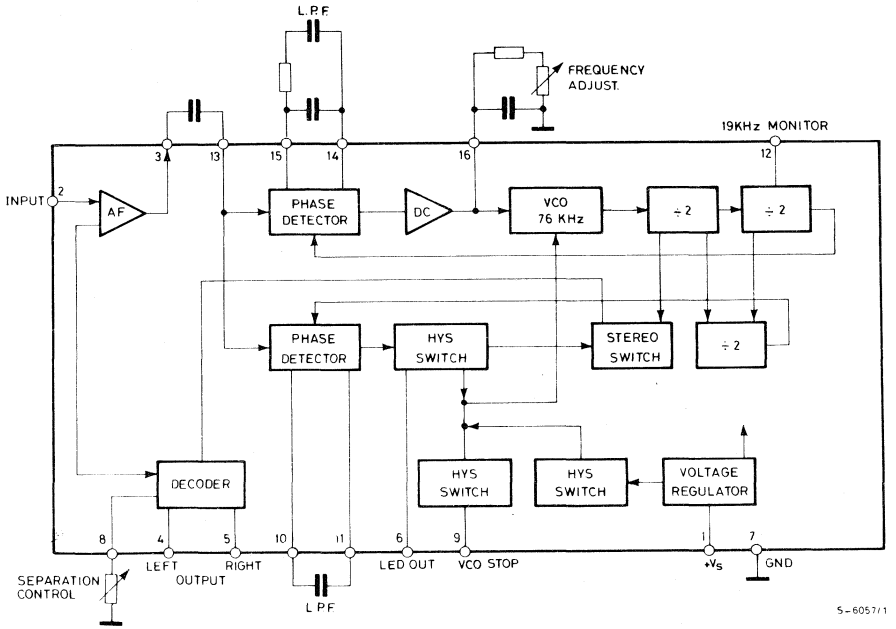
Dimensions in mm



## CONNECTION DIAGRAM
(top view)




## BLOCK DIAGRAM



## THERMAL DATA

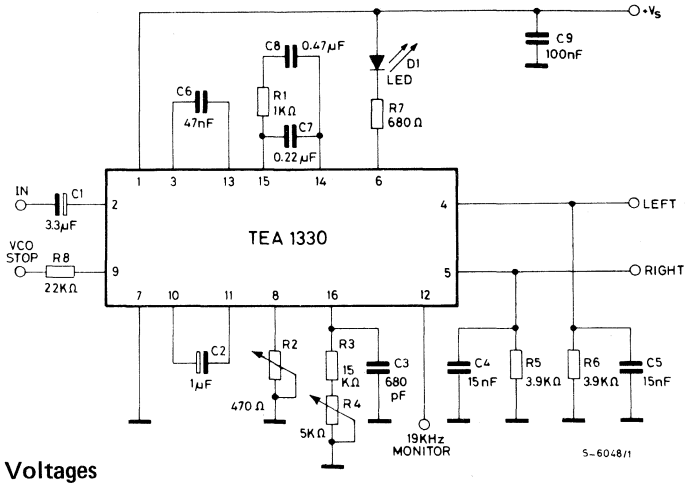
| | | | | |
|---|---|---|---|---|
| $R_{th\ j\text{-}amb}$ | Thermal resistance junction-ambient | max | 100 | °C/W |

## ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $T_{amb}$ = 25°C, $V_s$ = 6V, $V_i$ = 300 mV-RMS (L + R = 90%, Pilot 10%), $f_m$ = 1 KHz, unless otherwise specified)

| Parameter | | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_s$ | Supply voltage range | | 3 | | 14 | V |
| $I_d$ | Current drain | Lamp "OFF" | | 18 | | mA |
| $V_i$ | Max standard composite input signal | d = 1% | 300 | | | mV (RMS) |
| $V_i$ | Max mono input signal | d = 1% | 300 | | | mV (RMS) |
| $R_i$ | Input resistance | | | 40 | | KΩ |
| Sep | Stereo channel separation | R2 = variable (*) | 35 | 50 | | dB |
| | | R2 = 270 Ω | 25 | 40 | | dB |
| $V_o$ | Audio output voltage | | | 265 | | mV |
| CB | Mono channel balance | Pilot tone "OFF" | -2 | 0 | +2 | dB |
| d | Total harmonic distortion | $V_{in}$ = 150 mV (RMS) | | 0.3 | | % |
| UR | Ultrasonic frequency rejection | f = 19 KHz | | 32 | | dB |
| | | f = 38 KHz | | 48 | | dB |
| SCA-R | SCA rejection (**) | f = 67 KHz | | 76 | | dB |
| S/N | Signal to noise ratio | | | 80 | | dB |
| $V_{th}$ | Muting threshold voltage (pin 9) | ON (VCO stop) | | 1 | | V |
| | | OFF | | 0.8 | | V |
| $L_{on}$ | Pilot input level for lamp ON | f = 19 KHz | 4 | 6 | 9 | mV |
| Hys | Pilot input level hysteresis for lamp turn ON-OFF | f = 19 KHz | | 3 | | dB |
| CR | Capture range | | | ± 7 | | % |

(*) R2 has to be adjusted for best figure of channel separation.
(**) SCA = AUX. SUB. CARRIER.

Fig. 1 - Test circuit




## Typical DC Voltages

| Pins | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (V) | 6 | 1.9 | 1.3 | 3 | 3 | | 0 | 0.18 | | 1.4 | 1.4 | 1.2 | 1.4 | 1.4 | 1.4 | 2.2 |

Fig. 2 - P.C. board and components layout of the test circuit of fig. 1 (1:1 scale)

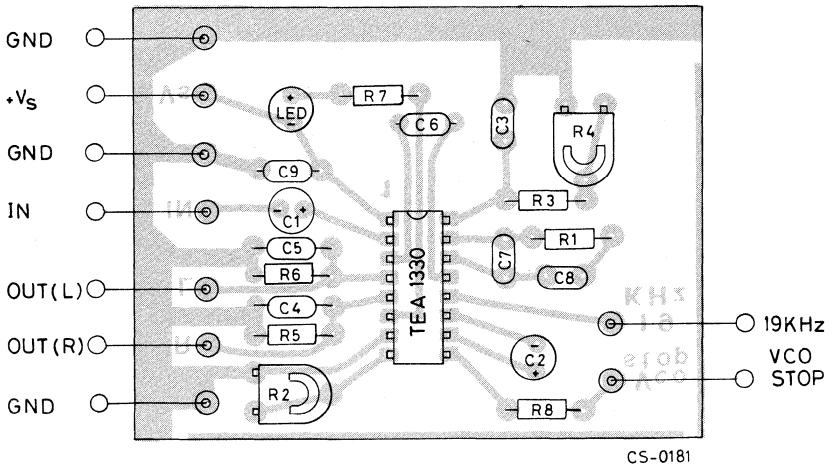


Fig. 3 - Channel separation vs. modulation frequency

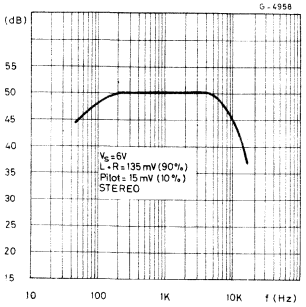



Fig. 4 - Distortion vs. modulation frequency

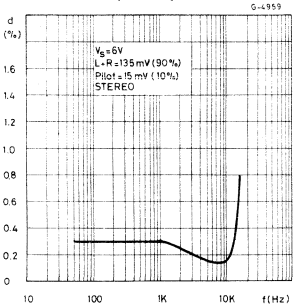



Fig. 5 - Channel separation vs. input level

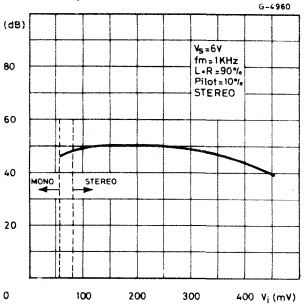



Fig. 6 - Distortion vs. input level

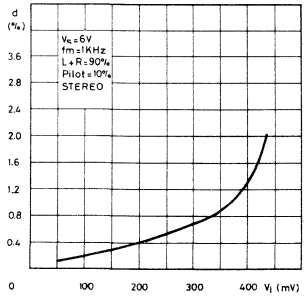



Fig. 7 - Channel separation vs. supply voltage

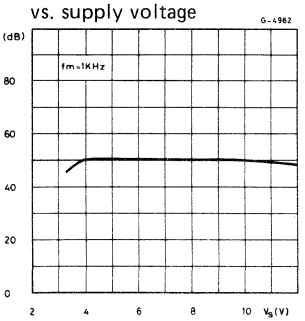
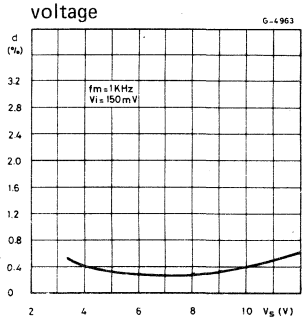



Fig. 8 - Distortion vs. supply voltage




## APPLICATION SUGGESTION (see test circuit of fig. 1)

| Component | Recommended value | Purpose | Smaller than recommended value | Larger than recommended value |
|---|---|---|---|---|
| C1 | 3.3 $\mu$F | Input coupling | Poor low frequency response and separation | |
| C2 | 1 $\mu$F | LPF for stereo switch level detector | Shorter time to switch mono to stereo | Longer time to switch mono to stereo |
| C3 (*)<br>R3<br>R4 | 680 pF<br>15 K$\Omega$<br>5 K$\Omega$ | Set VCO free running frequency | — High VCO jitter<br>— Wide capture range | Narrower capture range |

(*) Polyester ± 5%.

## APPLICATION SUGGESTION (continued)

| Component | Recommended value | Purpose | Smaller than recommended value | Larger than recommended value |
|---|---|---|---|---|
| C4<br>R5 (**) | 15 nF<br>3.9 KΩ | Load and deemphasis right channel | Low output voltage | Higher distortion for low $V_S$ |
| C5<br>R6 (**) | 15 nF<br>3.9 KΩ | Load and deemphasis left channel | Low output voltage | Higher distortion for low $V_S$ |
| C6 | 47 nF | Input PLL coupling | Poor low frequency response and separation | |
| C7<br>C8<br>R1 | 220 nF<br>470 nF<br>1 KΩ | Loop filter | High stereo distortion | Narrower capture range |
| D1 | | Stereo indicator | | |
| R7 | | Sets lamp current | Excess IC dissipation | Dim lamp |
| R2 (***) | 270 Ω | Channel separation | | |

(**) Deemphasis = 50 μs.
(***) Separation can be improved by trimmer adjustement (470 Ω).

Fig. 9 - Application circuit for portable stereo radio receivers

